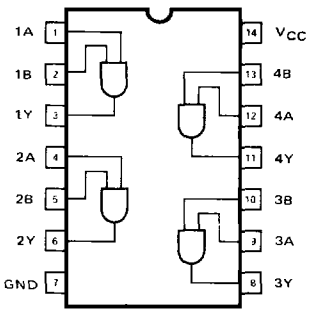
QUAD 2-INPUT AND GATE W/OPEN COLLECTOR OUTPUTS — 54/7409

SPEED/PACKAGE AVAILABILITY

54	F,W	74	A,F
54LS	F,W	74LS	A,F
54S	F,W	74S	A,F

PIN CONFIGURATION

A,F,W PACKAGE



Positive logic: Y = AB

SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

TEST CONDITIONS	54/74 C_L=15pF R_L=400Ω			54/74LS C_L=15pF R_L=2kΩ			54/74S C_L=15pF R_L=280Ω			UNIT
PARAMETER	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	
Propagation delay time t_{PLH} Low-to-high		21	32		20	35		6.5 (C_L=50pF) 9	10	ns
t_{PHL} High-to-low		16	24		20	35		6.5 (C_L=50pF) 9	10	ns

Load circuit and typical waveforms are shown at the front of section.

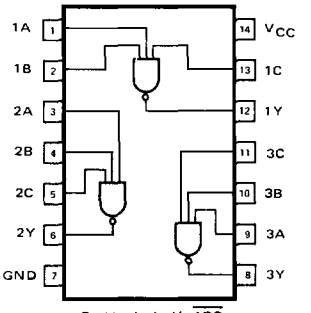
TRIPLE 3-INPUT NAND GATE — 54/7410

SPEED/PACKAGE AVAILABILITY

54	F,W	74	A,F
54H	F,W	74H	A,F
54LS	F,W	74LS	A,F
54S	F,W	74S	A,F

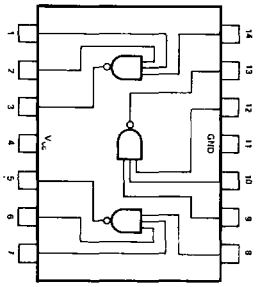
PIN CONFIGURATION

74,74H,54/74LS, 54/74S
A,F,W PACKAGE



Positive logic: $Y = \overline{ABC}$

54,54H
W PACKAGE



SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

TEST CONDITIONS	54/74 C_L=15pF R_L=400Ω			54/74H C_L=25pF R_L=280Ω			54/74LS C_L=15pF R_L=2kΩ			54/74S C_L=15pF R_L=280Ω			UNIT
PARAMETER	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	
Propagation delay time t_{PLH} Low-to-high		11	22		5.9	10		5	15	2	3 (C_L=50pF) 4.5	4.5	ns
t_{PHL} High-to-low		7	15		6.3	10		9	15	2	3 (C_L=50pF) 5	5	ns

Load circuit and typical waveforms are shown at the front of section.