SP2001

100MHz DIRECT DIGITAL FREQUENCY SYNTHESISER

(Supersedes January 1991 Edition)

The SP2001 Direct Frequency Synthesiser (DFS) is an ECL100K compatible 'numerically controlled oscillator' i.e. it directly generates the DAC code required for an output sinewave at any frequency up to 100MHz. The SP2001 has a 16 bit input bus giving a step size and minimum output frequency of 4kHz with a 262.144MHz clock

A full block diagram is shown in Fig 2.

FEATURES

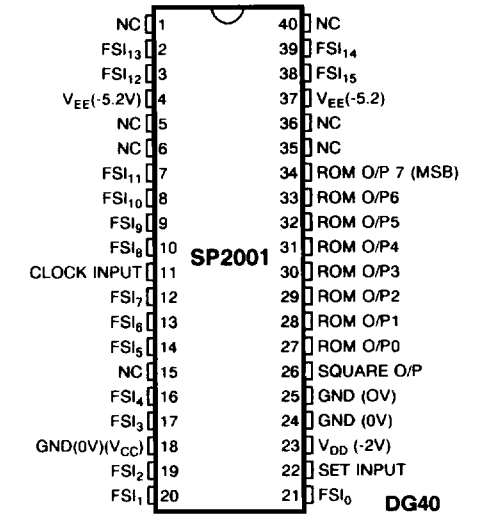
- Maximum clock frequency >300MHz
- 16-Bit Frequency resolution
- 8-Bit Parallel Cosine Output
- ECL 100K Compatible Inputs and Outputs
- Maximum Output Frequency > 100MHz
- Useable with 5, 10, 15 or 25kHz Channel Spacing
- Useable with 3.125, 6.25, 12.5 or 25kHz Channel Spacing
- Asynchronous Data Load for Fast (17ns) Hop Time
- Low Power: 1.85W
- Very Low Close to Carrier Noise.-135dBc/Hz Typ

APPLICATIONS

- LocalOscillator/Transmitter Synthesis in VHF Low Band (30-100MHz)
- LO Synthesis in Frequency Agile Radio/Radar
- Wide Single-Range Sinewave Generator
- ECM/ECCM -e.g. Follower Jammers or Fast Hoppers

ORDERING INFORMATION

SP2001 B DG
SP2001 A DG
SP2001 AA DG
SP2001 B HG
SP2001 A HG
SP2001 AA HG



PIN CONNECTIONS FOR HG PACKAGE

1	NC	16	NC	31	SQUARE O/P
2	FSI_{13}	17	NC	32	ROM O/P0
3	FSI_{12}	18	NC	33	ROM O/P1
4	V_{EE}(-5.2V)	19	FSI_4	34	ROM O/P2
5	NC	20	FSI_3	35	ROM O/P3
6	NC	21	GND(0V)(V_{CC})	36	ROM O/P4
7	NC	22	FSI_2	37	ROM O/P5
8	FSI_{11}	23	FSI_1	38	ROM O/P6
9	FSI_{10}	24	FSI_0	39	ROM O/P7
10	FSI_9	25	SET INPUT	40	NC
11	FSI_8	25	V_{DD}(-2V)	41	NC
12	CLOCK	27	GND(0V)	42	V_{EE}(-5.2V)
13	FSI_7	28	GND(0V)	43	FSI_{15}
14	FSI_6	29	NC	44	FSI_{14}
15	FSI_5	30	NC		

Fig.1 Pin connections - top view

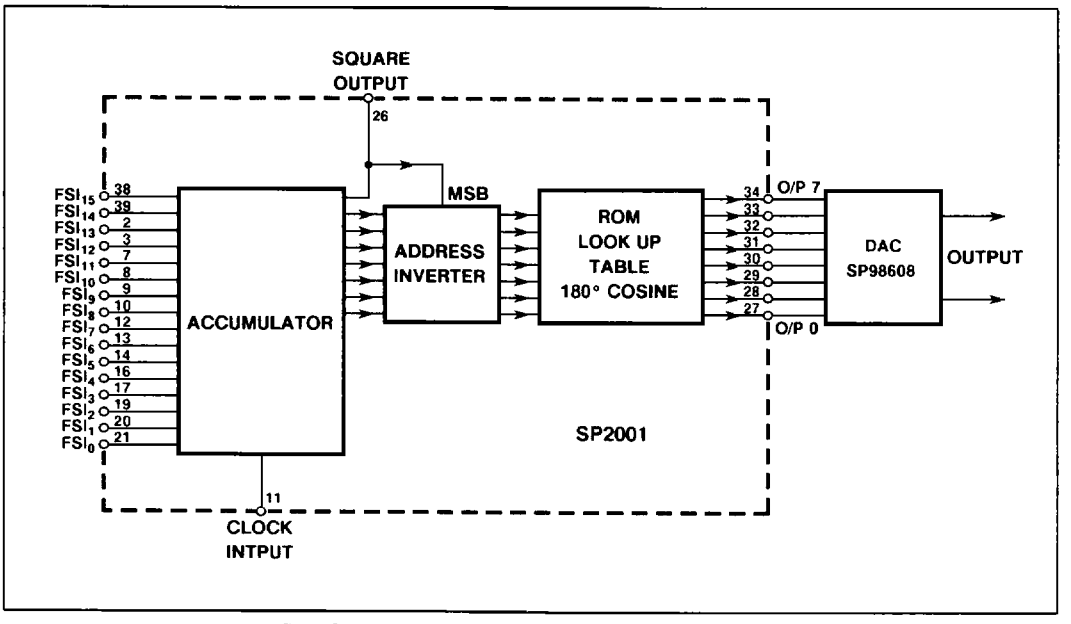


Fig.2 SP2001 Direct Frequency Synthesiser block diagram

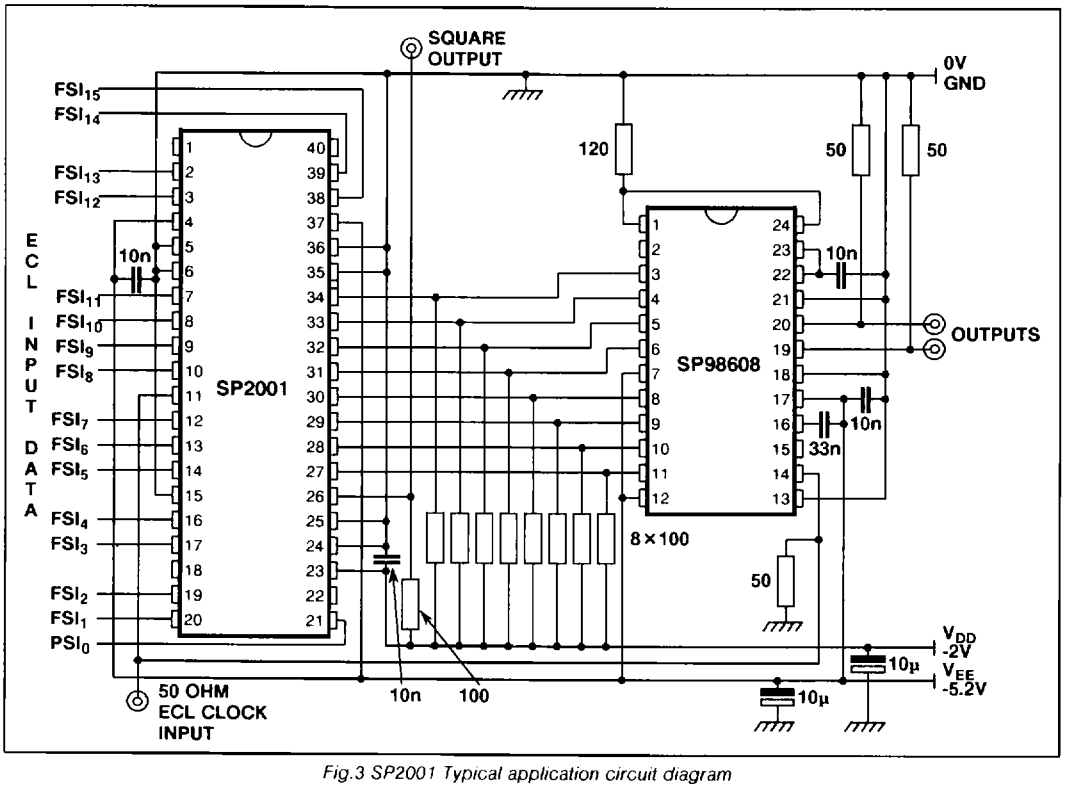


Fig.3 SP2001 Typical application circuit diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated)
V_{EE} = -5.2V ± 0.25V, V_{DD} = -2V ± 0.1V, V_{CC} = GND
A Grade T_{amb} = -55°C to +125°C (see note), B Grade T_{amb} = -40°C to +85°C

Characteristic	Pin	Value			Units	Conditions
		Min	Typ	Max		
Supply current I_{EE}	4,37	220	290	370	mA	All inputs at -1.8V
Supply current I_{DD}	23	40	60	84	mA	Does not include ECL output current
Input HIGH voltage	FSI_{0-15},Clk	-1125		-880	mV	
Input LOW voltage	FSI_{0-15},Clk	-1810		-1520	mV	
Output HIGH voltage	26-34	-1125		-880	mV	Loaded with100Ω to -2V
Output LOW voltage	26-34	-1810		-1520	mV	Loaded with100Ω to -2V

Note: The SP2001 must be used with a suitable heatsink to maintain chip temperature below 175°C when operating at Tamb > 85°Cfor DG package and >70°C for HG package. θ_{JA} DG = 36°C/W. θ_{JA} HG = 50°C/W

ABSOLUTE MAXIMUM RATINGS

Storage temperature	-65°C to 150°C
Max. junction temperature	+125°C
Max voltage between V_{EE} and V_{CC}	-7.0V to + 0.5V
Input voltage (DC)	V_{EE} to (V_{CC} + 0.5)V
Output current at V_O = V_{OH}	20mA

CIRCUIT DESCRIPTION

The SP2001 is a digital frequency synthesiser with an output frequency up to 100MHz. The channel spacing and minimum output frequency depend on the clock frequency, but with the clock set to 262.144 MHz the minimum output frequency and step size are 4kHz. The circuit needs no reactive components except power supply decoupling capacitors and is under full digital control at all times. Frequency accuracy is set by an external oscillator and close to carrier phase noise on the synthesiser output is dominated by the clock performance.

The fully digital system does not contain control loops so 'hop time' between discrete output frequencies is limited in principle only by the digital to analog converter settling time of about 5ns. In practice, to simplify the logic, a further delay of four clock periods has been added: the resultant delay of 20ns worst case is about five orders of magnitude faster than loop synthesisers. The block diagram (Fig. 2) shows the full DFS, including the recommended GPS SP98608 Digital to Analog Converter.

The function of the blocks can be seen from Fig.2. To avoid the need for a full 360 degrees in the ROM, the MSB output of the accumulator is used as a sign inverter, which with the LSBs, forms a digitised triangular number sequence. The MSB of the accumulator provides a square wave output via an ECL buffer which may be used as a variable clock in digital systems. The 1K ROM organised as 128x8 bits contains the data for 180 degrees stored in a cosine sequence which is read twice for each cycle of output data giving 256 words of data in total.

The data passes through retiming latches at each stage including the output in order to provide accurate data at the high clock rate; pipelined delays are unimportant in a non-looped system.

Finally the DAC reconstructs the output waveform, which consists of discrete points on the output sinusoid. Interpolation could be carried out by low pass filtering but in practice no filters are used except the inherent low pass action of the DAC.

Performance of the system is limited by the maximum update rate of the DAC used. The recommended SP98608 will typically update to ±½LSB at over 500MHz. When the clock is running at 327.68MHz, the DAC achieves 5-6 bits accuracy but is otherwise unimpaired in operation. Spur levels are frequency specific and are therefore difficult to measure and specify; also they are dependent on the performance of the output D-A converter. When using the GPS SP98608 450MHz DAC, the spur level remains close to the theoretical limit of -48dBc for an 8 bit system, for all output frequencies up to about 1/8 of the clock. At higher output frequencies around 1/4 of the clock, a spur with a frequency given by f_{CLOCK} -3 X f_{OUT} becomes significant when the clock frequency is greater than 100MHz. This spur has a level of approximately -47dBc at f_{CLOCK} = 100MHz degrading to -36dBc at f_{CLOCK} = 300MHz. When the input code is a whole binary number such as 0001 0000 0000 0000 the output will be free of spurs. Close to carrier noise is very good and is dominated by the clock source; measurements indicate a noise floor of better than -135 dBc/Hz at ±25kHz.

The set input (pin 22) provides a 'start from zero' as a test facility. It sets all the accumulator latches to zero so that the output of the ROM is all ones state.

The frequency equation is:

$$f_{OUT} = \frac{f_{CLOCK}}{2^{16}} \times \textit{Input Data}$$

e.g. For 5kHz increments, f_{CLOCK} = 327.68MHz
For 3.125kHz increments, f_{CLOCK} = 204.8MHz

APPLICATIONS

A typical application circuit diagram is shown in figure 3, using the SP2001 in conjunction with a GPS SP98608 DAC. The eight ECL data outputs from the SP2001 are connected directly to the DAC inputs with 100Ω pull down resistors. The pull down resistors are essential as there are no internal loads for the ECL output transistors.

A square wave output is available from pin 26 which uses an identical output stage to those feeding the DAC. The load resistance can be reduced to 50Ω to allow feeding a terminated 50Ω line. In applications where the square wave output is not required, it may be left open circuit to reduce power consumption. When only the square wave output is required, the DAC drive outputs may be left open circuit.

In the application Fig. 3, the DAC is used in latched mode with the clock input feeding both the SP2001 and the DAC. The DAC may also be used in transparent mode by connecting pin 15 to ground and removing the clock, but performance will be slightly degraded when compared to the latched case.

The clock required in the Fig. 3 application is an ECL square wave. When a high frequency clock is required, a true ECL signal may be difficult to obtain and the arrangement shown in Fig. 4 will be more suitable. In this case, the the clock inputs to the SP2001 and DAC are biased to the centre of the ECL logic swing range (approximately -1.4V) using 68Ω and 180Ω resistors which also provide a 50Ω match to the clock input cable. A sine wave clock signal is AC coupled to the biased clock inputs by C1. The optimum clock input level is +4dBm which equals the nominal 1V p-p standard ECL logic swing.

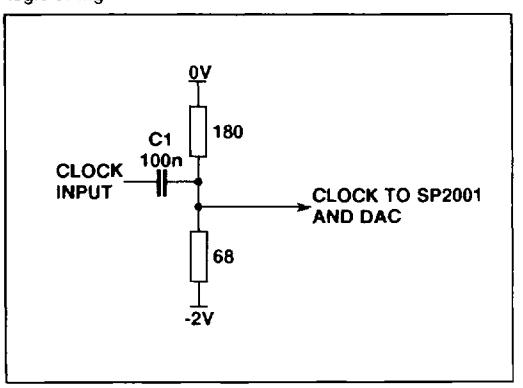


Fig. 4. Connection of high frequency sine wave clock

The Frequency Set data inputs to the SP2001 are ECL compatible with a nominal threshold voltage of about -1.4V and ECL data may be connected directly. Connection to CMOS input data is also straight forward provided the CMOS logic or microprocessor providing the data is operating from the -5.2V supply used by the SP2001. The arrangement is shown in figure 5.

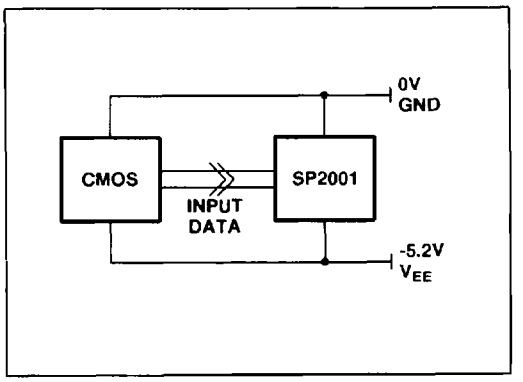


Fig. 5. Interface to CMOS logic

TTL drive logic may also be used in the same way as CMOS provided resistor pull ups are connected to the positive supply are used to ensure a logic high level close to the positive supply.

In order to obtain optimum performance, care should be taken with the layout of printed circuit boards. An earth plane as continuous as possible and common to both the SP2001 and the DAC should be used for the V_{CC} supply. The -5.2V V_{EE} and -2v V_{DD} supplies to both the SP2001 and the DAC should be decoupled close to the device pins preferably using surface mount 10nF capacitors. The eight ECL connections between the SP2001 and the DAC should be of equal length to ensure the input data is presented without time skew.