mosaic

Mosaic
Semiconductor
Inc.

PUMA 2S1000

PUMA 2S1000-85/10/12/15

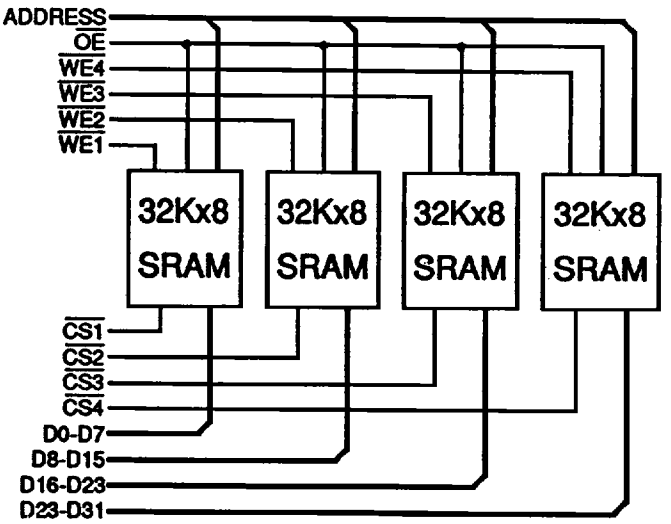
Issue 3.0 : August 1990

1,048,576 bit CMOS High Speed Static RAM

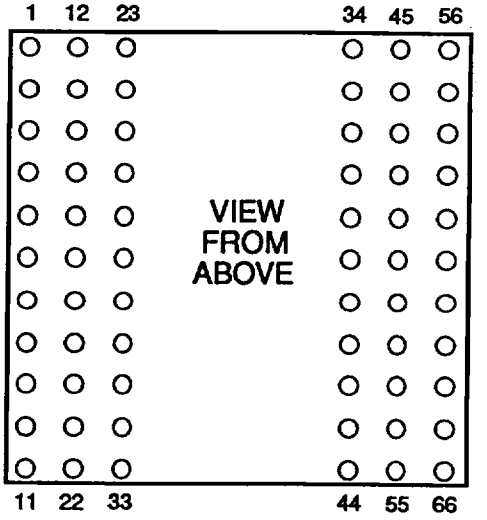
Features

User Configurable as 8,16 or 32 bit wide
Fast access times of 85/100/120/150 ns
Pin grid array gives 2:1 improvement over DIL
Package Suitable for Thermal Ladder Applications
On board decoupling capacitors
Operating Power 160mw (typ) 32 bit mode
90mw (typ) 16 bit mode
48mw (typ) 8 bit mode
Low Power Standby 40µW (typ) -L version
Battery back-up capability
May be screened in accordance with MIL-STD-883C

Block Diagram



Pin Definition

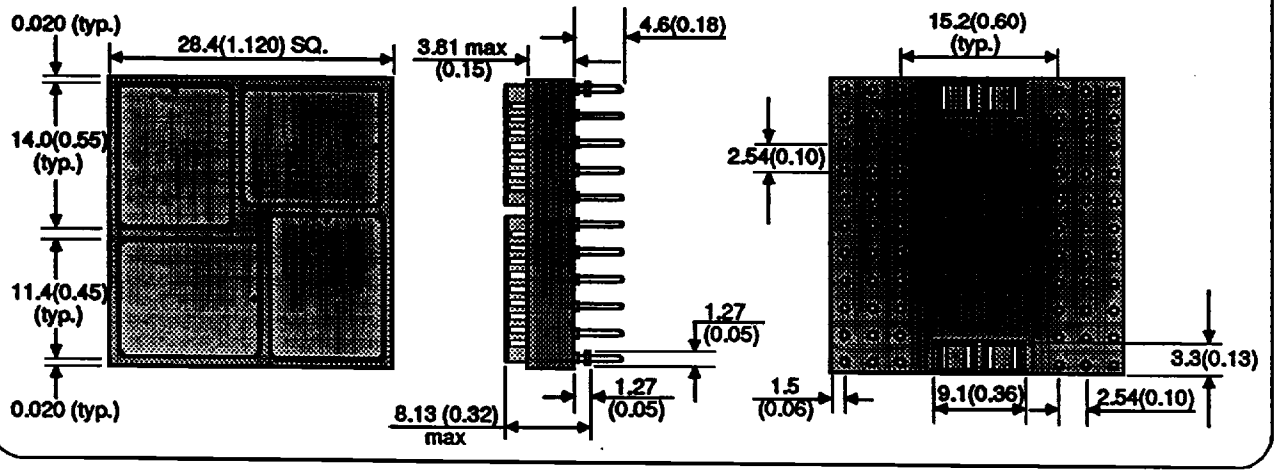


See page 5 for pinout

Pin Functions

A0 -A14	Address Inputs
D0-D31	Data Inputs/Outputs
$\overline{CS1-4}$	Chip Select
$\overline{OE}$	Output Enable
$\overline{WE1-4}$	Write Enable
NC	No Connect
V_{cc}	Power (+5V)
GND	Ground

Package Details Dimensions in mm (inches).



Absolute Maximum Ratings (1)

Voltage on any pin relative to V_{SS} (2)	V_T	-0.5V to +7	V
Power Dissipation	P_T	2	W
Storage Temperature	T_{STG}	-65 to +150	°C

Notes : (1) Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

(2) Pulse width:- 3.0V for less than 30ns.

Recommended Operating Conditions

		min	*typ*	*max*	
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.2	-	V_{CC}+0.3	V
Input Low Voltage	V_{IL}	-0.3	-	0.8	V
Operating Temperature	T_A	0	-	70	°C (2S1000)
	T_{AI}	-40	-	85	°C (2S1000I)
	T_{AM}	-55	-	125	°C (2S1000M, MB)

DC Electrical Characteristics (V_{CC}=5V±10%,T_A=-55°C to +125°C)

Parameter	*Symbol*	*Test Condition*	*min*	*typ*(1)	*max*	*Unit*	*Notes*
Input Leakage Current	I_{LI}	V_{IN}=0V to V_{CC}	-	-	2	µA	
Output Leakage Current	I_{LO}	$\overline{CS}$=V_{IH} or $\overline{OE}$=V_{IH} or $\overline{WE}$=V_{IH},					
		$V_{I/O}$=0V to V_{CC}	-	-	8	µA	(2)
Operating Supply Current	I_{CC}	$\overline{CS}$=V_{IL},$I_{I/O}$=0mA, I/P's static					
		32 BIT MODE	-	32	60	mA	(2)
Average Supply Current	I_{CC1}	Min. cycle, duty=100%,$I_{I/O}$=0mA					
		32 BIT MODE	-	200	280	mA	
		16 BIT MODE	-	101	146	mA	
		8 BIT MODE	-	52	79	mA	
	I_{CC2}	1µs cycle, duty=100%,$I_{I/O}$=0mA					
		32 BIT MODE	-	32	60	mA	
Standby Current	I_{SB}	$\overline{CS}$=V_{IH}	-	2	12	mA	(2)
	I_{SB1}	$\overline{CS}$≥V_{CC}-0.2V, I/P's<0.2V or ≥V_{CC}-0.2V	-	0.16	8	mA	(2)
(L-Part)	I_{SB2}	$\overline{CS}$≥V_{CC}-0.2V, I/P's<0.2V or ≥V_{CC}-0.2V	-	-	800	µA	(2)
Output Voltage Low	V_{OL}	I_{OL}=2.1mA	-	-	0.4	V	
Output Voltage High	V_{OH}	I_{OH}=-1.0mA	2.4	-	-	V	

Notes: (1) Typical values are at V_{CC}=5.0V,T_A=25°C and specified loading.

(2) $\overline{CS}$ above is accessed through $\overline{CS1-4}$ These inputs must be operated simultaneously for 32 bit mode, in pairs for 16 bit mode and singly for 8 bit mode.

Capacitance (V_{CC}=5V±10%,T_A=25°C)

Parameter	*Symbol*	*Test Condition*	*typ*	*max*	*Unit*
Input Capacitance:	C_{IN}	V_{IN}=0V	-	24	pF
I/O Capacitance:	$C_{I/O}$	$V_{I/O}$=0V	-	32	pF

Note: This parameter is calculated and not measured.

AC Test Conditions

*Input pulse levels: 0V to 3.0V
*Input rise and fall times: 5ns
*Input and Output timing reference levels: 1.5V
*Output load: 1 TTL gate + 100pF
*V_{cc}=5V±10%

Operating Modes

The Table below shows the logic inputs required to control the operating modes of each of the SRAMs on the PUMA 2S1000.

Mode	$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	V_{CC} Current	I/O Pin	Reference Cycle
Not Selected	1	X	X	I_{SB1},I_{SB2}	High Z	-
Read	0	0	1	I_{CC}	D_{OUT}	Read Cycle
Write	0	1	0	I_{CC}	D_{IN}	Write Cycle No.1
Write	0	0	0	I_{CC}	D_{IN}	Write Cycle No.2

$1 = V_{IH}$, $0 = V_{IL}$, X = Don't Care

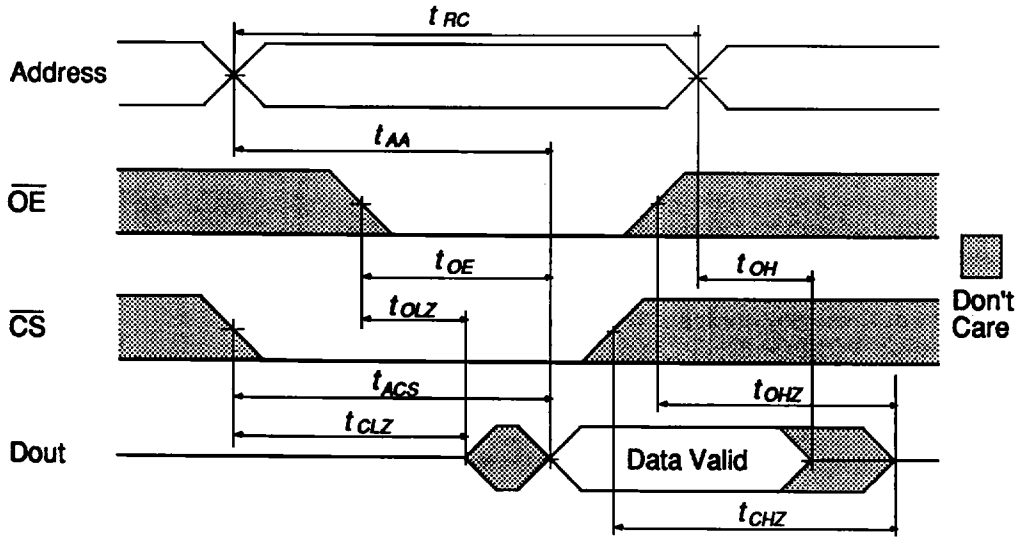
Note: $\overline{CS}$ is accessed through $\overline{CS1\text{-}4}$, and $\overline{WE}$ is accessed through $\overline{WE1\text{-}4}$. For correct operation, $\overline{CS1\text{-}4}$ must operate simultaneously for 32 bit operation, in pairs for 16 bit operation, or singly for 8 bit operation. $\overline{WE1\text{-}4}$ must also be operated in the same manner.

Electrical Characteristics & Recommended AC Operating Conditions

Read Cycle

		-85		-10		-12		-15		
Parameter	*Symbol*	*min*	*max*	*min*	*max*	*min*	*max*	*min*	*max*	*Unit*
Read Cycle Time	t_{RC}	85	-	100	-	120	-	150	-	ns
Address Access Time	t_{AA}	-	85	-	100	-	120	-	150	ns
Chip Select Access Time	t_{ACS}	-	85	-	100	-	120	-	150	ns
Output Enable to Output Valid	t_{OE}	-	45	-	50	-	60	-	70	ns
Output Hold from Address Change	t_{OH}	5	-	10	-	10	-	10	-	ns
Chip Selection to Output in Low Z[2]	t_{CLZ}	10	-	10	-	10	-	10	-	ns
Output Enable to Output in Low Z[2]	t_{OLZ}	5	-	5	-	5	-	5	-	ns
Chip Deselection to Output in High Z[2]	t_{CHZ}	0	30	0	35	0	40	0	50	ns
Output Disable to Output in High Z[2]	t_{OHZ}	0	30	0	35	0	40	0	50	ns

Read Cycle Timing Waveform (1)



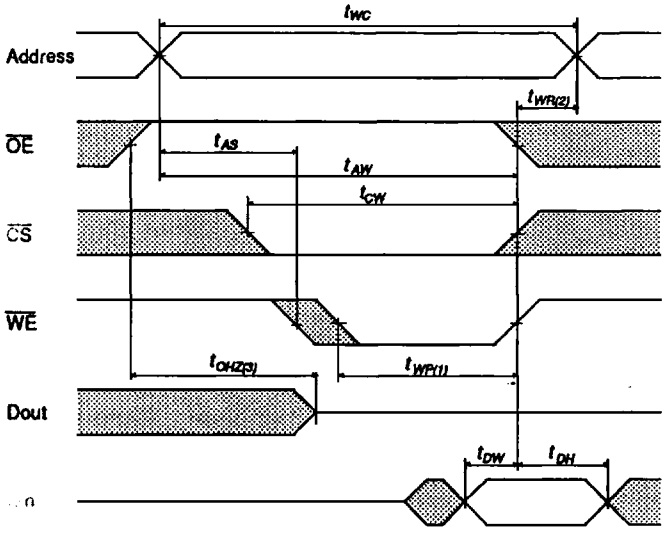
Notes: (1) $\overline{WE1\text{-}4}$ are High throughout a Read Cycle.

(2) t_{CHZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels. These parametere are sampled and not 100% tested.

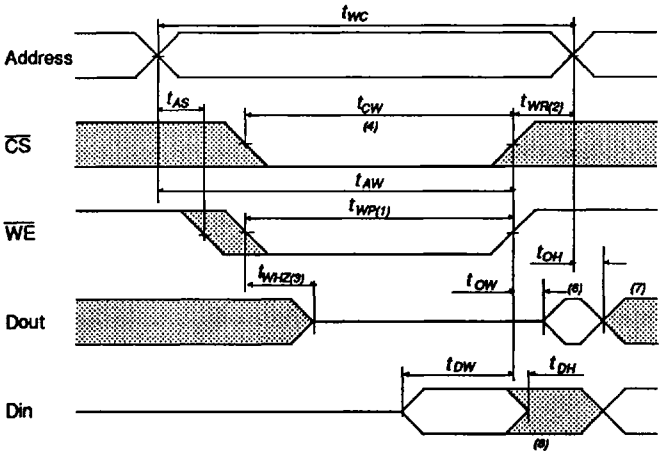
Write Cycle

Parameter	Symbol	-85 min	-85 max	-10 min	-10 max	-12 min	-12 max	-15 min	-15 max	Unit
Write Cycle Time	t_{WC}	85	-	100	-	120	-	150	-	ns
Chip Selection to End of Write	t_{CW}	75	-	80	-	85	-	100	-	ns
Address Valid to End of Write	t_{AW}	75	-	80	-	85	-	100	-	ns
Address Setup Time	t_{AS}	0	-	0	-	0	-	0	-	ns
Write Pulse Width	t_{WP}	60	-	60	-	70	-	90	-	ns
Write Recovery Time	t_{WR}	10	-	0	-	0	-	0	-	ns
Write to Output in High Z[9]	t_{WHZ}	0	30	0	35	0	40	0	50	ns
Data to Write Time Overlap	t_{DW}	40	-	40	-	50	-	60	-	ns
Data Hold from Write Time	t_{DH}	0	-	0	-	0	-	0	-	ns
Output Disable to Output in High Z[9]	t_{OHZ}	0	30	0	35	0	40	0	50	ns
Output Active from End of Write	t_{OW}	5	-	5	-	5	-	5	-	ns

Write Cycle No.1 Timing Waveform



Write Cycle No.2 Timing Waveform (11)



AC Characteristics Notes

(1) A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and a low $\overline{WE}$.
(2) t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
(3) During this period, I/O pins are in the output state. Input signals out of phase must not be applied.
(4) If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transition or after the $\overline{WE}$ low transition, outputs remain in a high impedance state.
(5) $\overline{OE}$ is continuously low. ($\overline{OE}$=V_{IL})
(6) Dout is in the same phase as written data of this write cycle.
(7) Dout is the read data of next address.
(8) If $\overline{CS}$ is low during this period, I/O pins are in the output state. Input signals out of phase must not be applied to I/O pins.
(9) t_{WHZ} and is defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels. This parameter is sampled and not 100% tested.

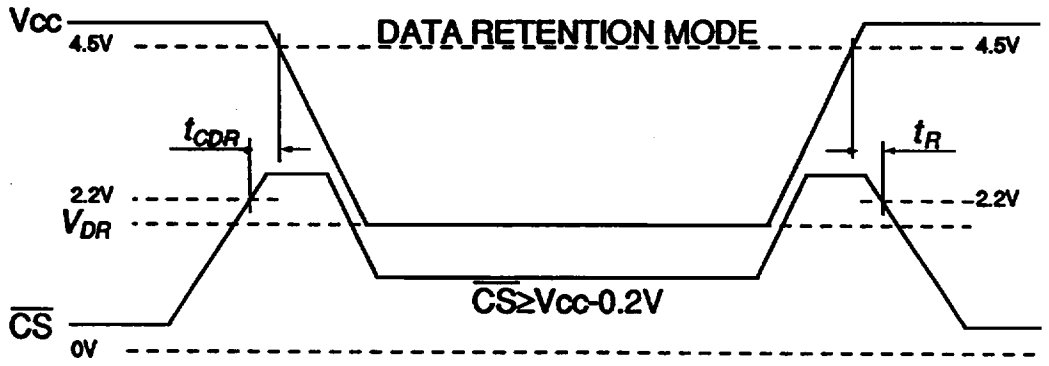
Connection Table

PGA Pin No.	Signal Name	PGA Pin No.	Signal Name	PGA Pin No.	Signal Name	PGA Pin No.	Signal Name	PGA Pin No.	Signal Name
1	D8	2	D9	3	D10	4	A13	5	A14
6	NC	7	NC	8	NC	9	D0	10	D1
11	D2	12	$\overline{WE2}$	13	$\overline{CS2}$	14	GND	15	D11
16	A10	17	A11	18	A12	19	V_{CC}	20	$\overline{CS1}$
21	NC	22	D3	23	D15	24	D14	25	D13
26	D12	27	$\overline{OE}$	28	NC	29	$\overline{WE1}$	30	D7
31	D6	32	D5	33	D4	34	D24	35	D25
36	D26	37	A6	38	A7	39	NC	40	A8
41	A9	42	D16	43	D17	44	D18	45	V_{CC}
46	$\overline{CS4}$	47	$\overline{WE4}$	48	D27	49	A3	50	A4
51	A5	52	$\overline{WE3}$	53	$\overline{CS3}$	54	GND	55	D19
56	D31	57	D30	58	D29	59	D28	60	A0
61	A1	62	A2	63	D23	64	D22	65	D21
66	D20								

Low V_{cc} Data Retention Characteristics - L Version Only

Parameter	Symbol	Test Condition	min	typ	max	Unit
V_{CC} for Data Retention	V_{DR}	$\overline{CS} \geq V_{CC}$-0.2V. $V_{IN} \geq 0V$	2.0	-	-	V
Data Retention Current		V_{CC}=3.0V,$V_{IN} \geq 0V$, $\overline{CS} \geq V_{CC}$-0.2V.				
	I_{CCDR1}	$T_{OP}=T_A$	-	32	120	mA
	I_{CCDR1}	$T_{OP}=T_{AI}$	-	-	200	µA
	I_{CCDR1}	$T_{OP}=T_{AM}$	-	-	600	µA
Chip Deselect to Data Retention Time	t_{CDR}	See Retention Waveform	0	-	-	ns
Operation Recovery Time	t_R	See Retention Waveform	5	-	-	ms

Low V_{cc} Data Retention Timing Waveform



Military Screening Procedure

Module Screening Flow for high reliability product is in accordance with MIL-STD-883C method 5004 Level B and is detailed below:

MB MODULE SCREENING FLOW		
SCREEN	*TEST METHOD*	*LEVEL*
Visual and Mechanical		
External visual	2017 Condition B (or manufacturers equivalent)	100%
Temperature cycle	1010 Condition C (10 Cycles,-65°C to +150°C)	100%
Burn-In		
Pre Burn-in Electrical	Per Applicable device Specifications at T_A = +25°C (optional)	100%
Burn-In	Method 1015, Condition D, T_A = +125°C	100%
Final Electrical Tests	Per applicable Device Specification	
Static (dc)	a) @ T_A=+25°C and power supply extremes	100%
	b) @ temperature and power supply extremes	100%
Functional	a) @ T_A=+25°C and power supply extremes	100%
	b) @ temperature and power supply extremes	100%
Switching (ac)	a) @ T_A=+25°C and power supply extremes	100%
	b) @ temperature and power supply extremes	100%
Percent Defective Allowable (PDA)	Calculated at Post Burn-in at T_A=+25°C	10%
Quality Conformance	Per applicable Device Specification	Sample
External Visual	2009 Per Vendor or customer specification	

Ordering Information

PUMA 2S1000LMB-10

Speed	85	= 85 ns
	10	= 100 ns
	12	= 120 ns
	15	= 150 ns
Temp. range/screening	Blank	= Commercial Temp.
	I	= Industrial Temp.
	M	= Military Temp.
	MB	= Screened in accordance with MIL STD 883C
Power Consumption	Blank	= Standard Power Part
	L	= Low Power Part
Memory Organisation	S1000	= 32K x 32 SRAM (Configurable)

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