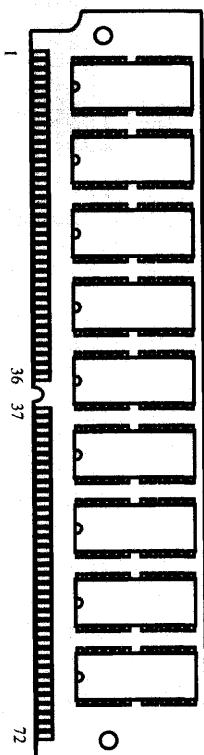




## Description

The GMM7374110CNS/SG is a 4M x 36 bits Dynamic RAM MODULE which is assembled 9 pieces of 4M x 4bit EDO DRAMs in 24 (26) pin SOJ package on the printed circuit board with decoupling capacitors. The GMM7374110CNS/SG is optimized for application to the systems which are required high density and large capacity such as main memory of the computers and an image memory systems, and to the others which are requested compact size. The GMM7374110CNS/SG provides common data inputs and Extended Data outputs.

- GMM7374110CNS/SG (Single Side)



## Features

- 72 pins Single In-Line Package
  - GMM7374110CNS : Solder plating
  - GMM7374110CNSG : Gold plating
- Extended Data Out (EDO) Mode Capability
- Single Power Supply
- Fast Access Time & Cycle Time

(Unit: ns)

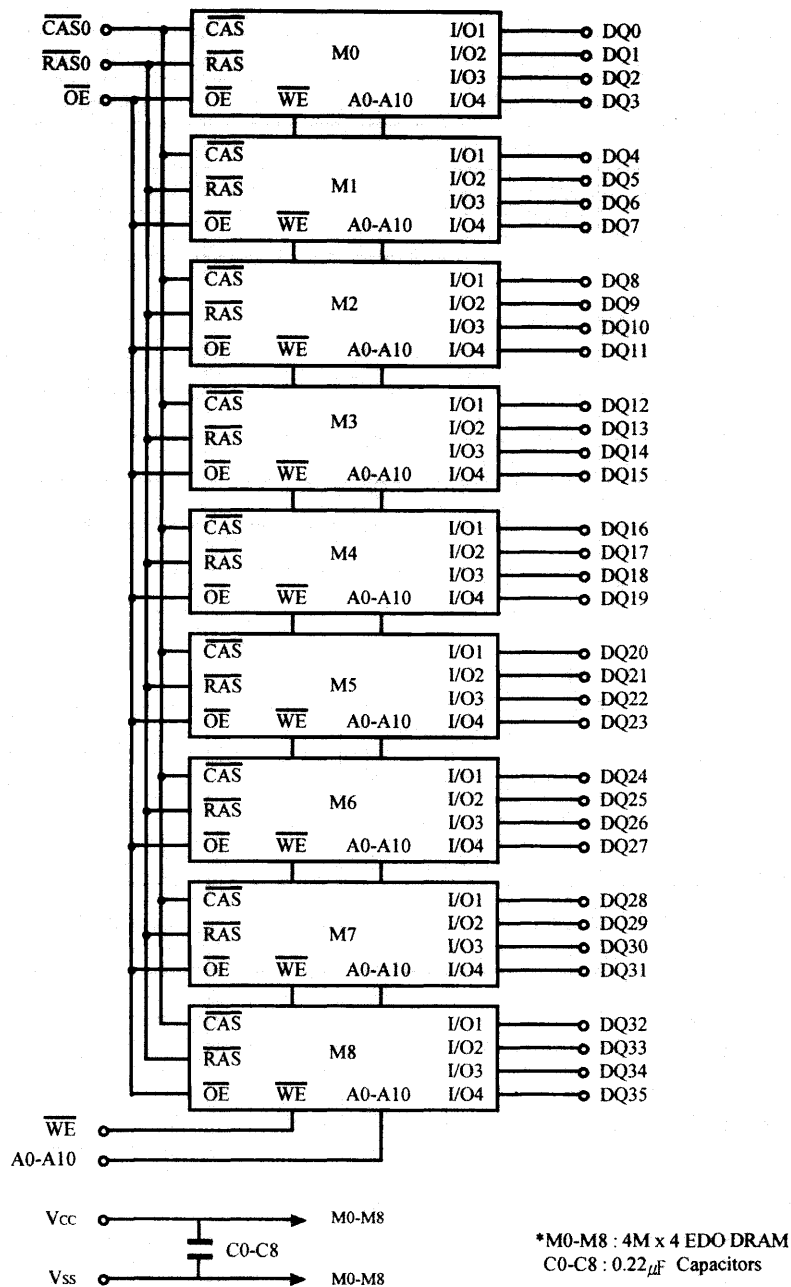
|                    | t <sub>TRAC</sub> | t <sub>CAC</sub> | t <sub>RC</sub> | t <sub>PC</sub> |
|--------------------|-------------------|------------------|-----------------|-----------------|
| GMM7374110CNS/SG-6 | 60                | 15               | 104             | 25              |
| GMM7374110CNS/SG-7 | 70                | 18               | 124             | 30              |
| GMM7374110CNS/SG-8 | 80                | 20               | 144             | 35              |

- Low Power
  - Active : 5,445/4,950/4,455mW (MAX)
  - Standby : 49.5mW (CMOS level : MAX)
- RAS Only Refresh, CAS before RAS Refresh, Hidden Refresh Capability
- All inputs and outputs TTL Compatible
- 2048 Refresh Cycles/32ms

## Pin Configuration (Top View)

| Pin | Symbol          | Pin | Symbol           | Pin | Symbol                 | Pin | Symbol           |
|-----|-----------------|-----|------------------|-----|------------------------|-----|------------------|
| 1   | V <sub>SS</sub> | 19  | <u>OE</u>        | 37  | DQ <sub>19</sub>       | 55  | DQ <sub>28</sub> |
| 2   | DQ <sub>0</sub> | 20  | DQ <sub>8</sub>  | 38  | DQ <sub>20</sub>       | 56  | DQ <sub>29</sub> |
| 3   | DQ <sub>1</sub> | 21  | DQ <sub>9</sub>  | 39  | <u>V<sub>SS</sub></u>  | 57  | DQ <sub>30</sub> |
| 4   | DQ <sub>2</sub> | 22  | DQ <sub>10</sub> | 40  | <u>CAS<sub>0</sub></u> | 58  | DQ <sub>31</sub> |
| 5   | DQ <sub>3</sub> | 23  | DQ <sub>11</sub> | 41  | A <sub>10</sub>        | 59  | V <sub>CC</sub>  |
| 6   | DQ <sub>4</sub> | 24  | DQ <sub>12</sub> | 42  | NC                     | 60  | DQ <sub>32</sub> |
| 7   | DQ <sub>5</sub> | 25  | DQ <sub>13</sub> | 43  | <u>NC</u>              | 61  | DQ <sub>33</sub> |
| 8   | DQ <sub>6</sub> | 26  | DQ <sub>14</sub> | 44  | <u>RAS<sub>0</sub></u> | 62  | DQ <sub>34</sub> |
| 9   | DQ <sub>7</sub> | 27  | DQ <sub>15</sub> | 45  | NC                     | 63  | DQ <sub>35</sub> |
| 10  | V <sub>CC</sub> | 28  | A <sub>7</sub>   | 46  | DQ <sub>21</sub>       | 64  | NC               |
| 11  | PD <sub>5</sub> | 29  | DQ <sub>16</sub> | 47  | <u>WE</u>              | 65  | NC               |
| 12  | A <sub>0</sub>  | 30  | V <sub>CC</sub>  | 48  | V <sub>SS</sub>        | 66  | NC               |
| 13  | A <sub>1</sub>  | 31  | A <sub>8</sub>   | 49  | DQ <sub>22</sub>       | 67  | PD <sub>1</sub>  |
| 14  | A <sub>2</sub>  | 32  | A <sub>9</sub>   | 50  | DQ <sub>23</sub>       | 68  | PD <sub>2</sub>  |
| 15  | A <sub>3</sub>  | 33  | NC               | 51  | DQ <sub>24</sub>       | 69  | PD <sub>3</sub>  |
| 16  | A <sub>4</sub>  | 34  | NC               | 52  | DQ <sub>25</sub>       | 70  | PD <sub>4</sub>  |
| 17  | A <sub>5</sub>  | 35  | DQ <sub>17</sub> | 53  | DQ <sub>26</sub>       | 71  | NC               |
| 18  | A <sub>6</sub>  | 36  | DQ <sub>18</sub> | 54  | DQ <sub>27</sub>       | 72  | V <sub>SS</sub>  |

# Block Diagram



**Pin Description**

| Pin               | Function              | Pin             | Function        |
|-------------------|-----------------------|-----------------|-----------------|
| A0-A10            | Address Inputs        | PD1-PD5         | Presence Detect |
| DQ0-DQ35          | Data Input/Output     | $\overline{OE}$ | Output Enable   |
| $\overline{RAS0}$ | Row Address Strobe    | V <sub>CC</sub> | Power (+5V)     |
| $\overline{CAS0}$ | Column Address Strobe | V <sub>SS</sub> | Ground          |
| $\overline{WE}$   | Read/Write Enable     | NC              | No Connection   |

**Presence Detect Pins (Optional)**

| Pin | 60ns            | 70ns            | 80ns            |
|-----|-----------------|-----------------|-----------------|
| PD1 | V <sub>SS</sub> | V <sub>SS</sub> | V <sub>SS</sub> |
| PD2 | NC              | NC              | NC              |
| PD3 | NC              | V <sub>SS</sub> | NC              |
| PD4 | NC              | NC              | V <sub>SS</sub> |
| PD5 | V <sub>SS</sub> | V <sub>SS</sub> | V <sub>SS</sub> |

**Absolute Maximum Ratings\***

| Symbol                            | Parameter                                      | Rating     | Unit |
|-----------------------------------|------------------------------------------------|------------|------|
| T <sub>A</sub>                    | Ambient Temperature under Bias                 | 0 ~ 70     | ℃    |
| T <sub>STG</sub>                  | Storage Temperature (Plastic)                  | -55 ~ 125  | ℃    |
| V <sub>IN</sub> /V <sub>OUT</sub> | Voltage on any Pin Relative to V <sub>SS</sub> | -1.0 ~ 7.0 | V    |
| V <sub>CC</sub>                   | Power Supply Voltage                           | -1.0 ~ 7.0 | V    |
| I <sub>OUT</sub>                  | Short Circuit Output Current                   | 50         | mA   |
| P <sub>D</sub>                    | Power Dissipation                              | 9.0        | W    |

\*Note: Stress greater than above g)bsolute Maximum Ratings may cause permanent damage to the device.

**Recommended DC Operating Conditions (T<sub>A</sub> = 0 ~ 70℃)**

| Symbol          | Parameter          | Min  | Typ | Max | Unit |
|-----------------|--------------------|------|-----|-----|------|
| V <sub>CC</sub> | Supply Voltage     | 4.5  | 5.0 | 5.5 | V    |
| V <sub>IH</sub> | Input High Voltage | 2.4  | -   | 6.5 | V    |
| V <sub>IL</sub> | Input Low Voltage  | -1.0 | -   | 0.8 | V    |

DC Electrical Characteristics ( $V_{CC} = 5V \pm 10\%$ ,  $T_A = 0 \sim 70^\circ\text{C}$ )

| Symbol              | Parameter                                                                                                                                                                                                                                           | Min  | Max             | Unit | Note |      |
|---------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------|-----------------|------|------|------|
| V <sub>OH</sub>     | Output Level<br>Output $\overline{\text{M}}\overline{\text{A}}\overline{\text{S}}$ Level Voltage (I <sub>OUT</sub> = -5mA)                                                                                                                          | 2.0  | V <sub>CC</sub> | V    |      |      |
| V <sub>OL</sub>     | Output Level<br>Output $\overline{\text{M}}\overline{\text{A}}\overline{\text{S}}$ Level Voltage (I <sub>OUT</sub> = 4.2mA)                                                                                                                         | 0    | 0.4             | V    |      |      |
| I <sub>CC1</sub>    | Operating Current<br>Average Power Supply Operating Current<br>( $\overline{\text{RAS}}$ , $\overline{\text{CAS}}$ , Address Cycling: t <sub>RC</sub> = t <sub>RC min</sub> )                                                                       | 60ns | -               | 990  | mA   | 1, 2 |
|                     |                                                                                                                                                                                                                                                     | 70ns | -               | 900  |      |      |
|                     |                                                                                                                                                                                                                                                     | 80ns | -               | 810  |      |      |
| I <sub>CC2</sub>    | Standby Current (TTL)<br>Power Supply Standby Current<br>( $\overline{\text{RAS}}$ , $\overline{\text{CAS}}$ = V <sub>IH</sub> )                                                                                                                    | -    | 18              | mA   |      |      |
| I <sub>CC3</sub>    | $\overline{\text{RAS}}$ Only Refresh Current<br>Average Power Supply Current<br>$\overline{\text{RAS}}$ Only Refresh Mode<br>( $\overline{\text{RAS}}$ Cycling, $\overline{\text{CAS}}$ = V <sub>IH</sub> , t <sub>RC</sub> = t <sub>RC min</sub> ) | 60ns | -               | 990  | mA   | 2    |
|                     |                                                                                                                                                                                                                                                     | 70ns | -               | 900  |      |      |
|                     |                                                                                                                                                                                                                                                     | 80ns | -               | 810  |      |      |
| I <sub>CC4</sub>    | Extended Data Out Mode Current<br>Average Power Supply Current<br>EDO Page Mode<br>( $\overline{\text{RAS}}$ = V <sub>IL</sub> , $\overline{\text{CAS}}$ , Address Cycling: t <sub>HPC</sub> = t <sub>HPC min</sub> )                               | 60ns | -               | 990  | mA   | 1, 3 |
|                     |                                                                                                                                                                                                                                                     | 70ns | -               | 900  |      |      |
|                     |                                                                                                                                                                                                                                                     | 80ns | -               | 810  |      |      |
| I <sub>CC5</sub>    | Standby Current (CMOS)<br>Power Supply Standby Current<br>( $\overline{\text{RAS}}$ , $\overline{\text{CAS}}$ ≥ V <sub>CC</sub> -0.2V)                                                                                                              | -    | 9               | mA   |      |      |
| I <sub>CC6</sub>    | $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Refresh Current<br>(t <sub>RC</sub> = t <sub>RC min</sub> )                                                                                                                                  | 60ns | -               | 990  | mA   |      |
|                     |                                                                                                                                                                                                                                                     | 70ns | -               | 900  |      |      |
|                     |                                                                                                                                                                                                                                                     | 80ns | -               | 810  |      |      |
| I <sub>CC7</sub>    | Standby Current $\overline{\text{RAS}}$ = V <sub>IH</sub><br>$\overline{\text{CAS}}$ = V <sub>IL</sub><br>D <sub>OUT</sub> = Enable                                                                                                                 | -    | 45              | mA   | 1    |      |
| I <sub>IL</sub> (L) | Input Leakage Current<br>Any Input (0V ≤ V <sub>IN</sub> ≤ 7V)<br>All Other Pins Not Under Test = 0V                                                                                                                                                | -90  | 90              | μA   |      |      |
| I <sub>OL</sub> (L) | Output Leakage Current<br>(D <sub>OUT</sub> is Disabled, 0V ≤ V <sub>OUT</sub> ≤ 7V)                                                                                                                                                                | -10  | 10              | μA   |      |      |

Note: 1.  $I_{CC}$  depends on output load condition when the device is selected.  $I_{CC}(\text{max})$  is specified at the output open condition.

2. Address can be changed once or less while  $\overline{\text{RAS}} = V_{IL}$ .

3. Address can be changed once or less while  $\overline{\text{CAS}} = V_{IH}$ .

**Capacitance** ( $V_{CC} = 5V \pm 10\%$ ,  $T_A = 25^\circ C$ )

| Symbol    | Parameter                  | Min | Max | Unit | Note |
|-----------|----------------------------|-----|-----|------|------|
| $C_{II}$  | Input Capacitance (A0-A10) | -   | 70  | pF   | 1    |
| $C_{I2}$  | Input Capacitance (Clocks) | -   | 80  | pF   | 1    |
| $C_{I/O}$ | I/O Capacitance (DQ0-DQ35) | -   | 17  | pF   | 1, 2 |

Note: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.

2.  $\overline{CAS} = V_{IH}$  to disable DOUT.

**AC Electrical Characteristics** ( $V_{CC} = 5V \pm 10\%$ ,  $T_A = 0 \sim 70^\circ C$ , Notes 1, 15)

The GMM7374110CNS/SG writes data only in early write cycle ( $t_{wcs} \geq t_{wcs(min)}$ ).

Delayed write cycle is not available because of I/O common.

**Read, Write and Refresh Cycle** (Common Parameters)

| Symbol    | Parameter                                           | GMM7374110<br>CNS/SG-6 |        | GMM7374110<br>CNS/SG-70 |        | GMM7374110<br>CNS/SG-80 |        | Unit | Note |
|-----------|-----------------------------------------------------|------------------------|--------|-------------------------|--------|-------------------------|--------|------|------|
|           |                                                     | Min                    | Max    | Min                     | Max    | Min                     | Max    |      |      |
| $t_{RC}$  | Random Read or Write Cycle Time                     | 104                    | -      | 124                     | -      | 144                     | -      | ns   |      |
| $t_{RP}$  | $\overline{RAS}$ Precharge Time                     | 40                     | -      | 50                      | -      | 60                      | -      | ns   |      |
| $t_{CP}$  | $\overline{CAS}$ Precharge Time                     | 10                     | -      | 13                      | -      | 15                      | -      | ns   |      |
| $t_{RAS}$ | $\overline{RAS}$ Pulse Width                        | 60                     | 10,000 | 70                      | 10,000 | 80                      | 10,000 | ns   |      |
| $t_{CAS}$ | $\overline{CAS}$ Pulse Width                        | 10                     | 10,000 | 13                      | 10,000 | 15                      | 10,000 | ns   |      |
| $t_{ASR}$ | Row Address Setup Time                              | 0                      | -      | 0                       | -      | 0                       | -      | ns   |      |
| $t_{RAH}$ | Row Address Hold Time                               | 10                     | -      | 10                      | -      | 10                      | -      | ns   |      |
| $t_{ASC}$ | Column Address Setup Time                           | 0                      | -      | 0                       | -      | 0                       | -      | ns   |      |
| $t_{CAH}$ | Column Address Hold Time                            | 10                     | -      | 13                      | -      | 15                      | -      | ns   |      |
| $t_{RCD}$ | $\overline{RAS}$ to $\overline{CAS}$ Delay Time     | 20                     | 45     | 20                      | 52     | 20                      | 60     | ns   | 9    |
| $t_{RAD}$ | $\overline{RAS}$ to Column Address Delay Time       | 15                     | 30     | 15                      | 35     | 15                      | 40     | ns   | 10   |
| $t_{RSH}$ | $\overline{RAS}$ Hold Time                          | 15                     | -      | 18                      | -      | 20                      | -      | ns   |      |
| $t_{CSH}$ | $\overline{CAS}$ Hold Time                          | 48                     | -      | 58                      | -      | 68                      | -      | ns   |      |
| $t_{CRP}$ | $\overline{CAS}$ to $\overline{RAS}$ Precharge Time | 5                      | -      | 5                       | -      | 5                       | -      | ns   |      |
| $t_{ODD}$ | $\overline{OE}$ to $D_{IN}$ Delay Time              | 15                     | -      | 18                      | -      | 20                      | -      | ns   |      |
| $t_{DZO}$ | $\overline{OE}$ Delay Time from $D_{IN}$            | 0                      | -      | 0                       | -      | 0                       | -      | ns   |      |
| $t_{DZC}$ | $\overline{CAS}$ Setup Time from $D_{IN}$           | 0                      | -      | 0                       | -      | 0                       | -      | ns   |      |
| $t_T$     | Transition Time (Rise and Fall)                     | 2                      | 50     | 2                       | 50     | 2                       | 50     | ns   | 8    |
| $t_{REF}$ | Refresh Period                                      | -                      | 64     | -                       | 64     | -                       | 64     | ms   |      |

## Read Cycle

| Symbol           | Parameter                                                     | GMM7374110<br>CNS/SG-6 |     | GMM7374110<br>CNS/SG-70 |     | GMM7374110<br>CNS/SG-80 |     | Unit | Note  |
|------------------|---------------------------------------------------------------|------------------------|-----|-------------------------|-----|-------------------------|-----|------|-------|
|                  |                                                               | Min                    | Max | Min                     | Max | Min                     | Max |      |       |
| t <sub>RAC</sub> | Access Time from $\overline{\text{RAS}}$                      | -                      | 60  | -                       | 70  | -                       | 80  | ns   | 2, 3  |
| t <sub>CAC</sub> | Access Time from $\overline{\text{CAS}}$                      | -                      | 15  | -                       | 18  | -                       | 20  | ns   | 3, 4  |
| t <sub>AA</sub>  | Access Time from Column Address                               | -                      | 30  | -                       | 35  | -                       | 40  | ns   | 3, 5  |
| t <sub>OAC</sub> | Access Time from $\overline{\text{OE}}$                       | -                      | 15  | -                       | 18  | -                       | 20  | ns   | 3     |
| t <sub>RCS</sub> | Read Command Setup Time                                       | 0                      | -   | 0                       | -   | 0                       | -   | ns   |       |
| t <sub>RCH</sub> | Read Command Hold Time to $\overline{\text{CAS}}$             | 0                      | -   | 0                       | -   | 0                       | -   | ns   | 6     |
| t <sub>RRH</sub> | Read Command Hold Time to $\overline{\text{RAS}}$             | 0                      | -   | 0                       | -   | 0                       | -   | ns   | 6     |
| t <sub>RAL</sub> | Column Address to $\overline{\text{RAS}}$ Lead Time           | 30                     | -   | 35                      | -   | 40                      | -   | ns   |       |
| t <sub>CLZ</sub> | $\overline{\text{CAS}}$ to Output in low-Z                    | 0                      | -   | 0                       | -   | 0                       | -   | ns   |       |
| t <sub>OH</sub>  | Output Data Hold Time                                         | 3                      | -   | 3                       | -   | 3                       | -   | ns   |       |
| t <sub>OH0</sub> | Output Data Hold Time from $\overline{\text{OE}}$             | 3                      | -   | 3                       | -   | 3                       | -   | ns   |       |
| t <sub>OEZ</sub> | Output Buffer Turn-off Time to $\overline{\text{OE}}$         | -                      | 15  | -                       | 15  | -                       | 15  | ns   | 7     |
| t <sub>OFF</sub> | Output Buffer Turn-off Time                                   | -                      | 15  | -                       | 15  | -                       | 15  | ns   | 7     |
| t <sub>CDD</sub> | $\overline{\text{CAS}}$ to $\overline{\text{DIN}}$ Delay Time | 15                     | -   | 18                      | -   | 20                      | -   | ns   |       |
| t <sub>CAL</sub> | Column Address to $\overline{\text{CAS}}$ Lead Time           | 18                     | -   | 23                      | -   | 28                      | -   | ns   |       |
| t <sub>OFB</sub> | Output Buffer Turn-off Time to $\overline{\text{RAS}}$        | -                      | 15  | -                       | 15  | -                       | 15  | ns   | 7, 16 |

## Write Cycle

| Symbol           | Parameter                                          | GMM7374110<br>CNS/SG-6 |     | GMM7374110<br>CNS/SG-70 |     | GMM7374110<br>CNS/SG-80 |     | Unit | Note |
|------------------|----------------------------------------------------|------------------------|-----|-------------------------|-----|-------------------------|-----|------|------|
|                  |                                                    | Min                    | Max | Min                     | Max | Min                     | Max |      |      |
| t <sub>WCS</sub> | Write Command Setup Time                           | 0                      | -   | 0                       | -   | 0                       | -   | ns   | 11   |
| t <sub>WCH</sub> | Write Command Hold Time                            | 10                     | -   | 13                      | -   | 15                      | -   | ns   |      |
| t <sub>WP</sub>  | Write Command Pulse Width                          | 10                     | -   | 10                      | -   | 10                      | -   | ns   |      |
| t <sub>RWL</sub> | Write Command to $\overline{\text{RAS}}$ Lead Time | 10                     | -   | 13                      | -   | 15                      | -   | ns   |      |
| t <sub>CWL</sub> | Write Command to $\overline{\text{CAS}}$ Lead Time | 10                     | -   | 13                      | -   | 15                      | -   | ns   |      |
| t <sub>DS</sub>  | Data-in Setup Time                                 | 0                      | -   | 0                       | -   | 0                       | -   | ns   | 12   |
| t <sub>DH</sub>  | Data-in Hold Time                                  | 10                     | -   | 13                      | -   | 15                      | -   | ns   | 12   |

## Refresh Cycle

| Symbol           | Parameter                                                                                                        | GMM7374110<br>CNS/SG-6 |     | GMM7374110<br>CNS/SG-70 |     | GMM7374110<br>CNS/SG-80 |     | Unit | Note |
|------------------|------------------------------------------------------------------------------------------------------------------|------------------------|-----|-------------------------|-----|-------------------------|-----|------|------|
|                  |                                                                                                                  | Min                    | Max | Min                     | Max | Min                     | Max |      |      |
| t <sub>CSR</sub> | $\overline{\text{CAS}}$ Set-up Time<br>( $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ Refresh Cycle) | 5                      | -   | 5                       | -   | 5                       | -   | ns   |      |
| t <sub>CHR</sub> | $\overline{\text{CAS}}$ Hold Time<br>( $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ Refresh Cycle)   | 10                     | -   | 10                      | -   | 10                      | -   | ns   |      |
| t <sub>RPC</sub> | $\overline{\text{RAS}}$ Precharge to $\overline{\text{CAS}}$ Hold Time                                           | 0                      | -   | 0                       | -   | 0                       | -   | ns   |      |
| t <sub>WRP</sub> | $\overline{\text{WE}}$ Set-up Time<br>( $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ Refresh Cycle)  | 0                      | -   | 0                       | -   | 0                       | -   | ns   |      |
| t <sub>WRH</sub> | $\overline{\text{WE}}$ Hold Time<br>( $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ Refresh Cycle)    | 10                     | -   | 10                      | -   | 10                      | -   | ns   |      |

## Extended Data Out (EDO) Mode Cycle

| Symbol            | Parameter                                                                | GMM7374110<br>CNS/SG-6 |         | GMM7374110<br>CNS/SG-70 |         | GMM7374110<br>CNS/SG-80 |         | Unit | Note |
|-------------------|--------------------------------------------------------------------------|------------------------|---------|-------------------------|---------|-------------------------|---------|------|------|
|                   |                                                                          | Min                    | Max     | Min                     | Max     | Min                     | Max     |      |      |
| t <sub>HPC</sub>  | EDO Mode Cycle Time                                                      | 25                     | -       | 30                      | -       | 35                      | -       | ns   |      |
| t <sub>CP</sub>   | EDO Mode $\overline{\text{CAS}}$ Precharge Time                          | 10                     | -       | 13                      | -       | 15                      | -       | ns   |      |
| t <sub>RASP</sub> | EDO Mode $\overline{\text{RAS}}$ Pulse Width                             | -                      | 100,000 | -                       | 100,000 | -                       | 100,000 | ns   | 13   |
| t <sub>ACP</sub>  | Access Time from $\overline{\text{CAS}}$ Precharge                       | -                      | 35      | -                       | 40      | -                       | 45      | ns   | 3,14 |
| t <sub>RHCP</sub> | $\overline{\text{RAS}}$ Hold Time from $\overline{\text{CAS}}$ Precharge | 35                     | -       | 40                      | -       | 45                      | -       | ns   |      |
| t <sub>RCHP</sub> | Read Command Hold Time from<br>$\overline{\text{CAS}}$ Precharge         | 35                     | -       | 40                      | -       | 45                      | -       | ns   |      |
| t <sub>DOH</sub>  | Output Data Hold Time from $\overline{\text{CAS}}$ Low                   | 3                      | -       | 3                       | -       | 3                       | -       | ns   |      |

**Notes:**

1. AC measurements assume  $t_r = 2\text{ns}$ .
2. Assumes that  $t_{\text{rCD}} \leq t_{\text{rCD}}(\text{max})$  and  $t_{\text{rAD}} \leq t_{\text{rAD}}(\text{max})$ . If  $t_{\text{rCD}}$  or  $t_{\text{rAD}}$  is greater than the maximum recommended value shown in this table,  $t_{\text{rAC}}$  exceeds the value shown.
3. Measured with a load circuit equivalent to 1TTL loads and 100pF.
4. Assumes that  $t_{\text{rCD}} \geq t_{\text{rCD}}(\text{max})$  and  $t_{\text{rAD}} \leq t_{\text{rAD}}(\text{max})$ .
5. Assumes that  $t_{\text{rCD}} \leq t_{\text{rCD}}(\text{max})$  and  $t_{\text{rAD}} \geq t_{\text{rAD}}(\text{max})$ .
6. Either  $t_{\text{rCD}}$  or  $t_{\text{rRH}}$  must be satisfied for a read cycles.
7.  $t_{\text{OFF}}(\text{max})$  defines the time at which the outputs achieve the open circuit condition and is not referenced to output voltage levels.
8.  $V_{\text{IH}}(\text{min})$  and  $V_{\text{IL}}(\text{max})$  are reference levels for measuring timing of input signals. Also, transition times are measured between  $V_{\text{IH}}$  and  $V_{\text{IL}}$ .
9. Operation with the  $t_{\text{rCD}}(\text{max})$  limit insures that  $t_{\text{rAC}}(\text{max})$  can be met,  $t_{\text{rCD}}(\text{max})$  is specified as a reference point only, if  $t_{\text{rCD}}$  is greater than the specified  $t_{\text{rCD}}(\text{max})$  limit, then access time is controlled exclusively by  $t_{\text{CAC}}$ .
10. Operation with the  $t_{\text{rAD}}(\text{max})$  limit insures that  $t_{\text{rAC}}(\text{max})$  can be met,  $t_{\text{rAD}}(\text{max})$  is specified as a reference point only, if  $t_{\text{rAD}}$  is greater than the specified  $t_{\text{rAD}}(\text{max})$  limit, then access time is controlled exclusively by  $t_{\text{AA}}$ .
11.  $t_{\text{WCS}}$  is not restrictive operating parameter. It is included in the data sheet as electrical characteristics only; If  $t_{\text{WCS}} \geq t_{\text{WCS}}(\text{min})$ , the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle.
12. These parameters are referenced to  $\overline{\text{CAS}}$  leading edge in early write cycles.
13.  $t_{\text{RASP}}$  is defines  $\overline{\text{RAS}}$  pulse width in Fast Page Mode cycles.
14. Access time is determined by the longer of  $t_{\text{AA}}$  or  $t_{\text{CAC}}$  or  $t_{\text{ACP}}$ .
15. An initial pause of  $200\mu\text{s}$  is required after power up followed by a minimum of eight initialization cycles (any combination of cycles containing  $\overline{\text{RAS}}$  clock such as  $\overline{\text{RAS}}$  only refresh). If the internal refresh counter is used, a minimum of eight  $\overline{\text{CAS}}$  before  $\overline{\text{RAS}}$  refresh cycles are required.
16.  $t_{\text{OFF}}$  and  $t_{\text{OFR}}$  are determined by the later rising edge of  $\overline{\text{RAS}}$  or  $\overline{\text{CAS}}$ .

**Timing Waveforms : Please refer to attached Timing Waveform-8**

Unit: mil (mm)  
\* (1mil = 1/1000 inches)

