HARRIS
SEMICONDUCTOR

CD74FCT151T, CD74FCT251T, CD74FCT2151T

Fast CMOS 8-Input Multiplexers

Features

- **Advanced 0.8 micron CMOS Technology**

- **These Devices are Pin Compatible with Bipolar FAST™ Series at a Higher Speed and Lower Power Consumption**

- **25Ω Series Resistor On All Outputs (FCT2151T Only)**

- **TTL Input and Output Levels**

- **Extremely Low Static Power**

- **Hysteresis on All Inputs**

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CD74FCT151TM	-40 to 85	16 Ld SOIC	M16.3-P
CD74FCT151ATM	-40 to 85	16 Ld SOIC	M16.3-P
CD74FCT151CTM	-40 to 85	16 Ld SOIC	M16.3-P
CD74FCT151TNM	-40 to 85	16 Ld SOIC	M16.15-P
CD74FCT151ATNM	-40 to 85	16 Ld SOIC	M16.15-P
CD74FCT151CTNM	-40 to 85	16 Ld SOIC	M16.15-P
CD74FCT151TQM	-40 to 85	16 Ld QSOP	M16.15A-P
CD74FCT151ATQM	-40 to 85	16 Ld QSOP	M16.15A-P
CD74FCT151CTQM	-40 to 85	16 Ld QSOP	M16.15A-P
CD74FCT251TM	-40 to 85	16 Ld SOIC	M16.3-P
CD74FCT251ATM	-40 to 85	16 Ld SOIC	M16.3-P
CD74FCT251CTM	-40 to 85	16 Ld SOIC	M16.3-P
CD74FCT251TNM	-40 to 85	16 Ld SOIC	M16.15-P
CD74FCT251ATNM	-40 to 85	16 Ld SOIC	M16.15-P
CD74FCT251CTNM	-40 to 85	16 Ld SOIC	M16.15-P
CD74FCT251TQM	-40 to 85	16 Ld QSOP	M16.15A-P
CD74FCT251ATQM	-40 to 85	16 Ld QSOP	M16.15A-P
CD74FCT251CTQM	-40 to 85	16 Ld QSOP	M16.15A-P
CD74FCT2151TM	-40 to 85	16 Ld SOIC	M16.3-P
CD74FCT2151ATM	-40 to 85	16 Ld SOIC	M16.3-P
CD74FCT2151CTM	-40 to 85	16 Ld SOIC	M16.3-P
CD74FCT2151TNM	-40 to 85	16 Ld SOIC	M16.15-P
CD74FCT2151ATNM	-40 to 85	16 Ld SOIC	M16.15-P
CD74FCT2151CTNM	-40 to 85	16 Ld SOIC	M16.15-P
CD74FCT2151TQM	-40 to 85	16 Ld QSOP	M16.15A-P
CD74FCT2151ATQM	-40 to 85	16 Ld QSOP	M16.15A-P
CD74FCT2151CTQM	-40 to 85	16 Ld QSOP	M16.15A-P

NOTE: QSOP is commonly known as SSOP.

When ordering, use the entire part number. Add the suffix 96 to obtain the variant in the tape and reel.

Description

The CD74FCT151T, CD74FCT251T, and CD74FCT2151T are high-speed 8-input multiplexers. They select one bit from a source of eight under the control of three select inputs. Both assertion and negation outputs are provided.
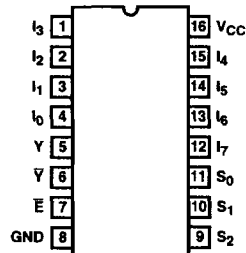
The CD74FCT151T, CD74FCT2151T have a common, active-LOW, Enable input ($\overline{E}$). When $\overline{E}$ is LOW, data from one of eight inputs is directed to the complementary outputs based on the 3-bit code applied to the Select (S_0-S_2) inputs. The CD74FCT151T, CD74FCT2151T can be used as a data routing device from one of eight sources.

The CD74FCT251T has a common Active-LOW Output Enable ($\overline{OE}$) input. When $\overline{OE}$ is LOW, data from one of eight inputs is directed to the complementary outputs. When $\overline{OE}$ is HIGH, both outputs are switched to a high-impedance state allowing multiplexer expansion by tying several outputs together.
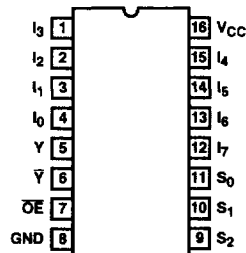
The CD74FCT2151T device has a built-in 25Ω series resistor on all outputs to reduce noise due to reflections, thus eliminating the need for an external terminating resistor.

Pinouts

CD74FCT151, CD74FCT2151T
(QSOP, SOIC)
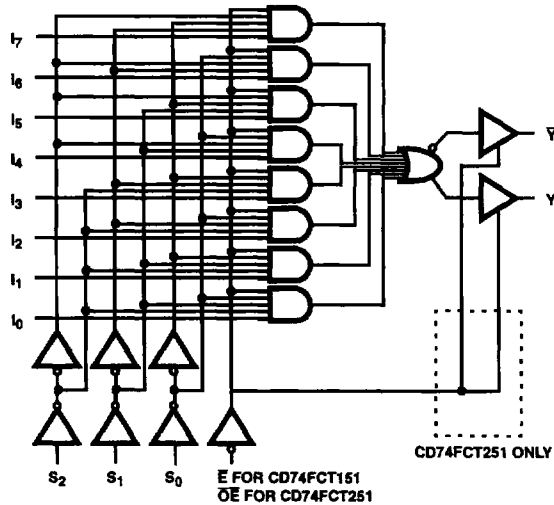**TOP VIEW**

I_3	1	16 V_{CC}
I_2	2	15 I_4
I_1	3	14 I_5
I_0	4	13 I_6
Y	5	12 I_7
$\overline{Y}$	6	11 S_0
$\overline{E}$	7	10 S_1
GND	8	9 S_2

CD74FCT251
(QSOP, SOIC)
TOP VIEW

I_3	1	16 V_{CC}
I_2	2	15 I_4
I_1	3	14 I_5
I_0	4	13 I_6
Y	5	12 I_7
$\overline{Y}$	6	11 S_0
$\overline{OE}$	7	10 S_1
GND	8	9 S_2

4

OCTAL 5V FCT
5V FCT 25Ω

FAST™ is a trademark of Fairchild Semiconductor.

File Number **4160.2**

Functional Block Diagram

TRUTH TABLE (NOTE 1)

INPUTS				OUTPUTS	
S_2	S_1	S_0	(NOTE 2) E/OE	Y	$\bar{Y}$
X	X	X	H	L (Note 3)	H (Note 3)
X	X	X	H	Z (Note 4)	Z (Note 4)
L	L	L	L	I0	$\bar{I0}$
L	L	H	L	I1	$\bar{I1}$
L	H	L	L	I2	$\bar{I2}$
L	H	H	L	I3	$\bar{I3}$
H	L	L	L	I4	$\bar{I4}$
H	L	H	L	I5	$\bar{I5}$
H	H	L	L	I6	$\bar{I6}$
H	H	H	L	I7	$\bar{I7}$

NOTES:
1. H = High Voltage Level, L = Low Voltage Level, X = Don't Care
   Z = High Impedance.
2. $\bar{E}$ for 151/2151, $\overline{OE}$ for 251.
3. 151/2151 ONLY.
4. 251 ONLY.

Pin Descriptions

PIN NAME	DESCRIPTION
I_0-I_7	Data Inputs
S_0-S_2	Select Inputs
$\bar{E}$	Enable Input (Active LOW) FCT151/2151T
$\overline{OE}$	Output Enable (Active LOW) FCT251T
Y	Data Output
$\bar{Y}$	Inverted Data Output
GND	Ground
V_{CC}	Power

Absolute Maximum Ratings

DC Input Voltage . . . . -0.5V to 7.0V
DC Output Current 120mA

Operating Conditions

Operating Temperature Range . . . . -40°C to 85°C
Supply Voltage to Ground Potential
   Inputs and V_{CC} Only . . . . -0.5V to 7.0V
Supply Voltage to Ground Potential
   Outputs and D/O Only . . . . -0.5V to 7.0V

Thermal Information

Thermal Resistance (Typical, Note 5)	θ_{JA} (°C/W)
16 Lead SOIC (150 mil) Package	110
16 Lead SOIC (300 mil) Package	97
16 Lead QSOP Package	140

Maximum Junction Temperature . . . . 150°C
Maximum Storage Temperature Range . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . 300°C
   (Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

5. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

PARAMETER	SYMBOL	(NOTE 6) TEST CONDITIONS		MIN	(NOTE 7) TYP	MAX	UNITS
DC ELECTRICAL SPECIFICATIONS Over the Operating Range, T_A = -40°C to 85°C, V_{CC} = 5.0V ±5%							
Output HIGH Voltage	V_{OH}	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	I_{OH} = -15.0mA	2.4	3.0	-	V
Output LOW Voltage	V_{OL}	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	I_{OL} = 48mA	-	0.3	0.50	V
Output LOW Voltage	V_{OL}	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	I_{OL} = 12mA (25Ω series)	-	0.3	0.50	V
Input HIGH Voltage	V_{IH}	Guaranteed Logic HIGH Level		2.0	-	-	V
Input LOW Voltage	V_{IL}	Guaranteed Logic LOW Level		-	-	0.8	V
Input HIGH Current	I_{IH}	V_{CC} = Max	V_{IN} = V_{CC}	-	-	1	µA
Input LOW Current	I_{IL}	V_{CC} = Max	V_{IN} = GND	-	-	-1	µA
High Impedance Output Current	I_{OZH}, I_{OZL}	V_{CC} = Max	V_{OUT} = 2.7V			1	µA
			V_{OUT} = 0.5V			-1	µA
Clamp Diode Voltage	V_{IK}	V_{CC} = Min, I_{IN} = -18mA		-	-0.7	-1.2	V
Short Circuit Current	I_{OS}	V_{CC} = Max (Note 8), V_{OUT} = GND		-60	-120	-	mA
Power Down Disable	I_{OFF}	V_{CC} = GND, V_{OUT} = 4.5V		-	-	100	µA
Input Hysteresis	V_H			-	200	-	mV
CAPACITANCE T_A = 25°C, f = 1MHz							
Input Capacitance (Note 9)	C_{IN}	V_{IN} = 0V		-	6	10	pF
Output Capacitance (Note 9)	C_{OUT}	V_{OUT} = 0V		-	8	12	pF
POWER SUPPLY SPECIFICATIONS							
Quiescent Power Supply Current	I_{CC}	V_{CC} = Max	V_{IN} = GND or V_{CC}	-	0.1	500	µA
Supply Current per Input at TTL HIGH	ΔI_{CC}	V_{CC} = Max	V_{IN} = 3.4V (Note 10)	-	0.5	2.0	mA
Supply Current per Input per MHz (Note 11)	I_{CCD}	V_{CC} = Max, Outputs Open $\overline{E}$ or $\overline{OE}$ = GND One Bit Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	-	0.15	0.25	mA/ MHz
Total Power Supply Current (Note 13)	I_C	V_{CC} = Max, Outputs Open f_I = 10MHz, 50% Duty Cycle $\overline{E}$ or $\overline{OE}$ = GND One Bit Toggling	V_{IN} = V_{CC} V_{IN} = GND	-	3.2	6.5 (Note 12)	mA
			V_{IN} = 3.4V V_{IN} = GND	-	3.5	7.5 (Note 12)	

4

OCTAL 5V FCT
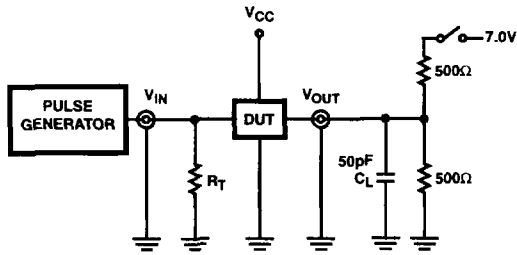5V FCT 25Ω

CD74FCT151T, CD74FCT251T, CD74FCT2151T

Switching Specifications Over Operating Range

PARAMETER	SYMBOL	(NOTE 14) TEST CONDITIONS	T (NOTE 15) MIN	T MAX	AT (NOTE 15) MIN	AT MAX	CT (NOTE 15) MIN	CT MAX	UNIT
CD74FCT151T, CD74FCT2151T									
Propagation Delay Sn to $\overline{Y}$	t_{PLH}, t_{PHL}	$C_L = 50pF$ $R_L = 500\Omega$	1.5	9.0	1.5	6.6	1.5	5.6	ns
Propagation Delay Sn to Y	t_{PLH}, t_{PHL}		1.5	10.5	1.5	6.8	1.5	5.8	ns
Propagation Delay $\overline{E}$ to $\overline{Y}$	t_{PLH}, t_{PHL}		1.5	7.0	1.5	5.6	1.5	4.8	ns
Propagation Delay $\overline{E}$ to Y	t_{PLH}, t_{PHL}		1.5	9.5	1.5	5.8	1.5	5.0	ns
Propagation Delay In to $\overline{Y}$	t_{PLH}, t_{PHL}		1.5	6.5	1.5	5.2	1.5	4.4	ns
Propagation Delay In to Y	t_{PLH}, t_{PHL}		1.5	7.5	1.5	5.5	1.5	4.7	ns
CD74FCT251T									
Propagation Delay Sn to $\overline{Y}$	t_{PLH}, t_{PHL}	$C_L = 50pF$ $R_L = 500\Omega$	1.5	9.0	1.5	6.6	1.5	5.6	ns
Propagation Delay Sn to Y	t_{PLH}, t_{PHL}		1.5	11.0	1.5	6.8	1.5	5.8	ns
Propagation Delay In to $\overline{Y}$	t_{PLH}, t_{PHL}		1.5	7.0	1.5	5.2	1.5	4.4	ns
Propagation Delay In to Y	t_{PLH}, t_{PHL}		1.5	7.0	1.5	5.5	1.5	4.7	ns
Output Enable Time $\overline{OE}$ to $\overline{Y}$	t_{PZH}, t_{PZL}		1.5	9.0	1.5	6.7	1.5	5.7	ns
Output Disable Time (Note 16) $\overline{OE}$ to $\overline{Y}$	t_{PHZ}, t_{PLZ}		1.5	7.5	1.5	6.0	1.5	5.0	ns
Output Enable Time $\overline{OE}$ to Y	t_{PZH}, t_{PZL}		1.5	9.0	1.5	6.7	1.5	5.7	ns
Output Disable Time (Note 16) $\overline{OE}$ to Y	t_{PHZ}, t_{PLZ}		1.5	7.0	1.5	6.0	1.5	5.0	ns

NOTES:

6. For conditions show as Max or Min, use appropriate value specified under Electrical Specifications for the applicable device type.

7. Typical values are at $V_{CC} = 5.0V$, 25°C ambient and maximum loading.

8. Not more than one output should be shorted at one time. Duration of the test should not exceed one second

9. This parameter is determined by device characterization but is not production tested.

10. Per TTL driven input ($V_{IN} = 3.4V$); all other inputs at V_{CC} or GND.

11. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.

12. Values for these conditions are examples of the Icc formula. These limits are guaranteed but not tested.

13. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
$I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_I N_I)$
I_{CC} = Quiescent Current
ΔI_{CC} = Power Supply Current for a TTL High Input (Vin = 3.4V)
D_H = Duty Cycle for TTL Inputs High
N_T = Number of TTL Inputs at D_H
I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
f_I = Input Frequency
N_I = Number of Inputs at f_I
All currents are in milliamps and all frequencies are in megahertz.

14. See test circuit and wave forms.

15. Minimum limits are guaranteed but not tested on Propagation Delays.

16. This parameter is guaranteed but not production tested.

Test Circuits and Waveforms

SWITCH POSITION

TEST	SWITCH
t_{PLZ}, t_{PZL}	Closed
t_{PHZ}, t_{PZH}, t_{PLH}, t_{PHL}	Open

DEFINITIONS:

C_L = Load capacitance, includes jig and probe capacitance.

R_T = Termination resistance, should be equal to Z_{OUT} of the Pulse Generator.

NOTE:

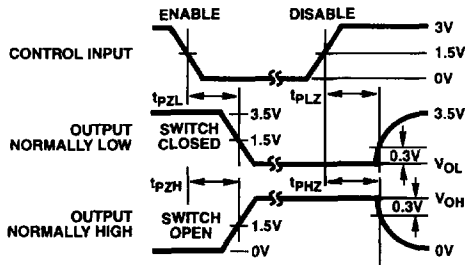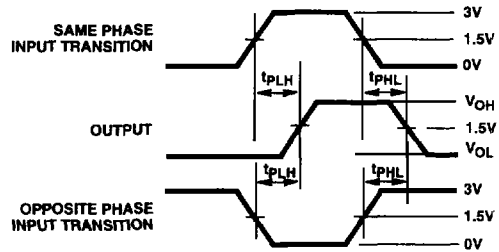17. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; Z_{OUT} ≤ 50Ω; t_f, t_r ≤ 2.5ns.

FIGURE 1. TEST CIRCUIT

FIGURE 2. ENABLE AND DISABLE TIMING

FIGURE 3. PROPAGATION DELAY

4

OCTAL 5V FCT
5V FCT 25Ω