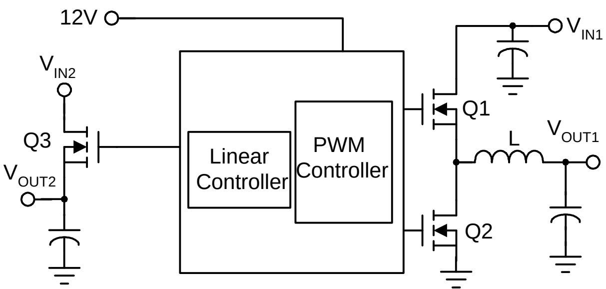
Synchronous Buck PWM and Linear Controller with 0.8V Reference Out Voltage

Features

- **Two Regulated Voltages and REF_OUT**
  - **Synchronous Buck Converter**
  - **Linear Regulator**
  - **REF_OUT = 0.8V±1% with 3mA source current**
- **Single 12V Power Supply Required**
- **Excellent Both Output Voltage Regulation**
  - **0.8V Internal Reference**
  - **±1% Over Line Voltage and Temperature**
- **Integrated Soft-Start for PWM and Linear Outputs**
- **300KHz Fixed Switching Frequency**
- **Voltage Mode PWM Control Design and Up to 89% (Typ.) Duty Cycle**
- **Under-Voltage Protection Monitoring Linear Output**
- **Over-Voltage Protection Monitoring PWM Output**
- **Over-Current Protection for PWM Output**
  - **Sense Low-side MOSFET's $R_{DS(ON)}$**
- **SOP-14, QSOP-16 and Compact QFN4x4-16 packages**
- **Lead Free and Green Devices Available (RoHS Compliant)**

Simplified Application Circuit



General Description

The APW7068 integrates synchronous buck PWM, linear controller, and 0.8V Reference Out Voltage, as well as the monitoring and protection functions into a single package. The fixed 300kHz switching frequency synchronous PWM controller drives dual N-channel MOSFETs, which provides one controlled power output with over-voltage and over-current protections. Linear controller drives an external N-channel MOSFET with under-voltage protection.

The APW7068 provides excellent regulation for output load variation. An internal 0.8V temperature-compensated reference voltage is designed to meet the requirement of low output voltage applications.

The APW7068 with excellent protection functions: POR, OCP, OVP and UVP. The Power-On-Reset (POR) circuit can monitor V_{CC12} supply voltage exceeds its threshold voltage while the controller is running, and a built-in digital soft-start provides both outputs with controlled rising voltage. The Over-Current Protection (OCP) monitors the output current by using the voltage drop across the lower MOSFET's $R_{DS(ON)}$, comparing with the voltage of OCSET pin, $V_{OCSET.}$ The maximum V_{OCSET} voltage is limited to the internal default value 0.25V. In addition, when OCSET pin is floating (no R_{OCSET} resistor), the over current threshold will also be internal default value, 0.25V. When the output current reaches the trip point, the controller will shutdown the IC directly, and latch the converter's output. The Under-Voltage Protection (UVP) monitors the voltage of FBL pin for short-circuit protection. When the V_{FBL} is less than 50% of V_{REF}, the controller will shutdown the IC directly. The Over-Voltage Protection (OVP) monitors the voltage of FB. When the V_{FB} is over 135% of V_{REF}, the controller will make Low-side gate signal fully turn on until the fault events are removed.

Applications

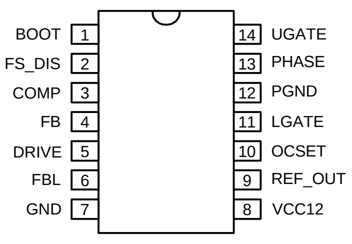
- **Graphic Cards**

Ordering and Marking Information

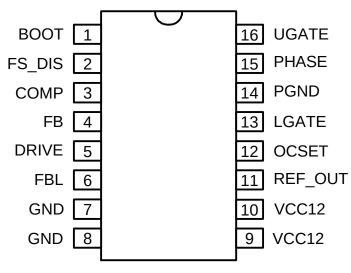
APW7068 □□□-□□□ (Assembly Material; Handling Code; Temp. Range; Package Code)	Package Code K : SOP-14 M : QSOP - 16 QA : QFN 4x4-16 Temp. Range E : -20 to 70 °C Handling Code TR : Tape & Reel Assembly Material L : Lead Free Device G : Halogen and Lead Free Device
APW7068 K : APW7068 XXXXX	XXXXX - Date Code
APW7068 M : APW7068 XXXXX	XXXXX - Date Code
APW7068 QA : APW7068 XXXXX	XXXXX - Date Code

Note: ANPEC lead-free products contain molding compounds/die attach materials and 100% matte tin plate termination finish; which are fully compliant with RoHS. ANPEC lead-free products meet or exceed the lead-free requirements of IPC/JEDEC J-STD-020C for MSL classification at lead-free peak reflow temperature. ANPEC defines “Green” to mean lead-free (RoHS compliant) and halogen free (Br or Cl does not exceed 900ppm by weight in homogeneous material and total of Br and Cl does not exceed 1500ppm by weight).

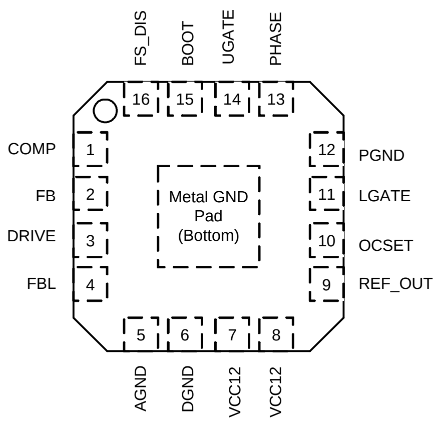
Pin Configuration



SOP-14
TOP VIEW



QSOP-16
TOP VIEW



QFN 4x4-16
TOP VIEW

Absolute Maximum Ratings (Note 1)

Symbol	Parameter	Rating	Unit
V_{CC12}	VCC12 to GND	-0.3 to +16	V
V_{BOOT}	BOOT to PHASE	-0.3 to +16	V
V_{UGATE}	UGATE to PHASE <400ns pulse width >400ns pulse width	-5 to V_{BOOT} +5 -0.3 to V_{BOOT} +0.3	V
V_{LGATE}	LGATE to PGND <400ns pulse width >400ns pulse width	-5 to V_{CC12}+5 -0.3 to V_{CC12}+0.3	V
V_{PHASE}	PHASE to GND <200ns pulse width >200ns pulse width	-10 to +30 -0.3 to 16	V
V_{DRIVE}	DRIVE to GND	12	V
V_{FB}, V_{FBL}, V_{COMP}, V_{FS_DIS}	FB, FBL, COMP, FS_DIS to GND	-0.3 to 7	V

Absolute Maximum Ratings (Cont.)

Symbol	Parameter	Rating	Unit
V_{PGND}	PGND to GND	-0.3 to +0.3	V
T_J	Junction Temperature Range	-20 to +150	°C
T_{STG}	Storage Temperature	-65 ~ 150	°C
T_{SDR}	Maximum Lead Soldering Temperature, 10 Seconds	260	°C

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Symbol	Parameter	Rating	Unit
V_{CC12}	IC Supply Voltage	10.8 to 13.2	V
V_{IN1}	Converter Input Voltage	2.9 to 13.2	V
V_{OUT1}	Converter Output Voltage	0.9 to 5	V
I_{OUT1}	Converter Output Current	0 to 30	A
I_{OUT2}	Linear Output Current	0 to 3	A
T_A	Ambient Temperature Range	-20 to 70	°C
T_J	Junction Temperature Range	-20 to 125	°C

Electrical Characteristics

Unless otherwise specified, these specifications apply over V_{CC12} = 12V, and T_A =-20 ~ 70°C. Typical values are at T_A = 25°C.

Symbol	Parameter	Test Conditions	APW7068			Unit
			Min	Typ	Max	
INPUT SUPPLY CURRENT						
I_{CC12}	VCC12 Supply Current (Shutdown mode)	UGATE, LGATE and DRIVE open; FS_DIS = GND		4	6	mA
	VCC12 Supply Current	UGATE, LGATE and DRIVE open		8	12	mA
POWER-ON-RESET						
	Rising VCC12 Threshold		7.7	7.9	8.1	V
	Falling VCC12 Threshold		7.2	7.4	7.6	V
OSCILLATOR						
	Accuracy		-15		+15	%
F_{OSC}	Oscillator Frequency		255	300	345	kHz
V_{OSC}	Ramp Amplitude	(nominal 1.2V to 2.7V) (Note 2)		1.5		V
Duty	Maximum Duty Cycle			89		%
REFERENCE						
V_{REF}	Reference Voltage	for Error Amp1 and Amp2	0.792	0.80	0.808	V
	Reference Voltage Tolerance		-1		+1	%
	PWM Load Regulation	I_{OUT1} = 0 to 10A			1	%
	Linear Load Regulation	I_{OUT2} = 0 to 3A			1	%
PWM ERROR AMPLIFIER						
Gain	Open Loop Gain	R_L = 10k, C_L = 10pF (Note 2)		93		dB
GBWP	Open Loop Bandwidth	R_L = 10k, C_L = 10pF (Note 2)		20		MHz

Electrical Characteristics (Cont.)

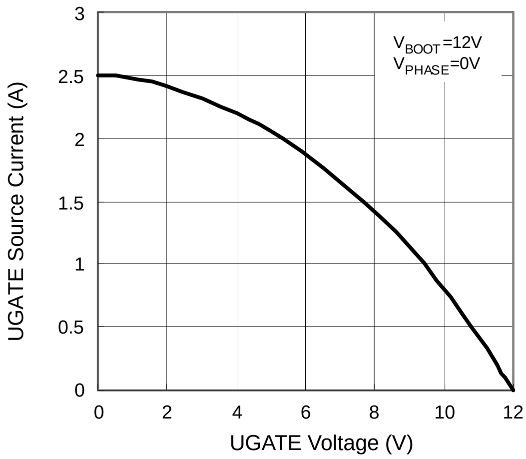
Unless otherwise specified, these specifications apply over V_{CC12} = 12V, and T_A =-20 ~ 70°C. Typical values are at T_A = 25°C.

Symbol	Parameter	Test Conditions	APW7068			Unit
			Min	Typ	Max	
PWM ERROR AMPLIFIER (Cont.)						
SR	Slew Rate	R_L = 10k, C_L = 10pF (Note 2)		8		V/µs
	FB Input Current	V_{FB} = 0.8V		0.1	1	µA
V_{COMP}	COMP High Voltage			5		V
V_{COMP}	COMP Low Voltage			0		V
I_{COMP}	COMP Source Current	V_{COMP} = 2V		12		mA
I_{COMP}	COMP Sink Current	V_{COMP} = 2V		12		mA
GATE DRIVERS						
I_{UGATE}	Upper Gate Source Current	V_{BOOT} = 12V, V_{UGATE} - V_{PHASE} = 2V		2.5		A
I_{UGATE}	Upper Gate Sink Current			2		A
I_{LGATE}	Lower Gate Source Current	V_{CC12} = 12V, V_{LGATE} = 2V		2.5		A
I_{LGATE}	Lower Gate Sink Current			3.5		A
R_{UGATE}	Upper Gate Source Impedance	V_{BOOT} = 12V, I_{UGATE} = 0.1A		2.25	3.375	Ω
R_{UGATE}	Upper Gate Sink Impedance	V_{BOOT} = 12V, I_{UGATE} = 0.1A		0.7	1.05	Ω
R_{LGATE}	Lower Gate Source Impedance	V_{CC12} = 12V, I_{LGATE} = 0.1A		2.25	3.375	Ω
R_{LGATE}	Lower Gate Sink Impedance	V_{CC12} = 12V, I_{LGATE} = 0.1A		0.4	0.6	Ω
T_D	Dead Time			20		ns
LINEAR REGULATOR						
Gain	Open Loop Gain	R_L = 10k, C_L = 10pF (Note 2)		70		dB
GBWP	Open Loop Bandwidth	R_L = 10k, C_L = 10pF (Note 2)		19		MHz
SR	Slew Rate	R_L = 10k, C_L = 10pF (Note 2)		6		V/µs
	FBL Input Current	V_{FBL}= 0.8V		0.1	1	µA
V_{DRIVE}	DRIVE High Voltage			10		V
V_{DRIVE}	DRIVE Low Voltage			0		V
I_{DRIVE}	DRIVE Source Current	V_{DRIVE} = 5V		4		mA
I_{DRIVE}	DRIVE Sink Current	V_{DRIVE} = 5V		3		mA
PROTECTION						
V_{FB-OV}	FB Over Voltage Protection Trip Point	Percent of V_{REF}		135		%
V_{FBL-UV}	FBL Under Voltage Protection Trip Point	Percent of V_{REF}		50		%
I_{OCSET}	OCSET Current Source		36	40	44	µA
SOFT START						
T_{SS}	Internal Soft-Start Interval (NOTE3)	F_{OSC}=300kHz		8.5		ms
REF_OUT						
V_{REF_OUT}	Output Voltage		0.792	0.800	0.808	V
	Offset Voltage		-8		+8	mV
I_{REF_OUT}	Source Current		1.5	3		mA
	Sink Current		0.25	0.5		mA
	Output Capacitance		0.4	1	2.2	µF

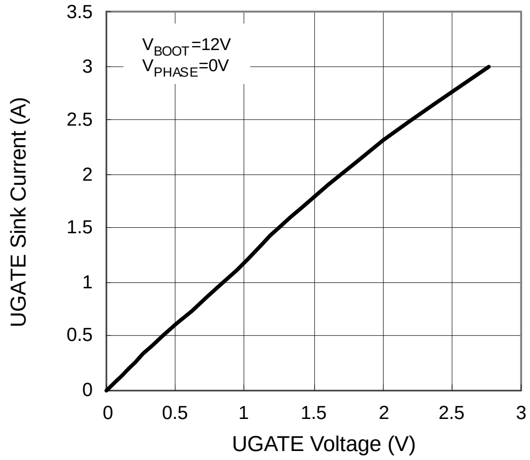
Note 2: Guaranteed by design.

Typical Operating Characteristics

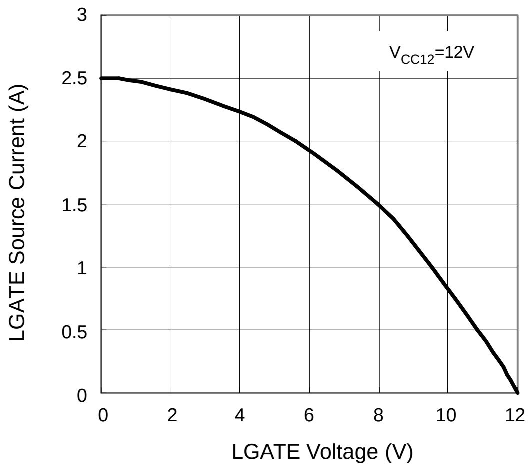
UGATE Source Current vs. UGATE Voltage



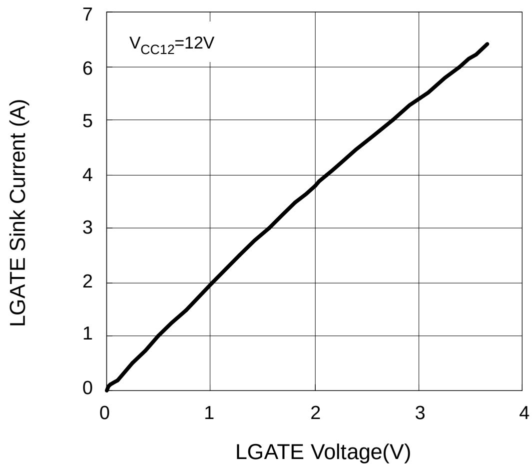
UGATE Sink Current vs. UGATE Voltage



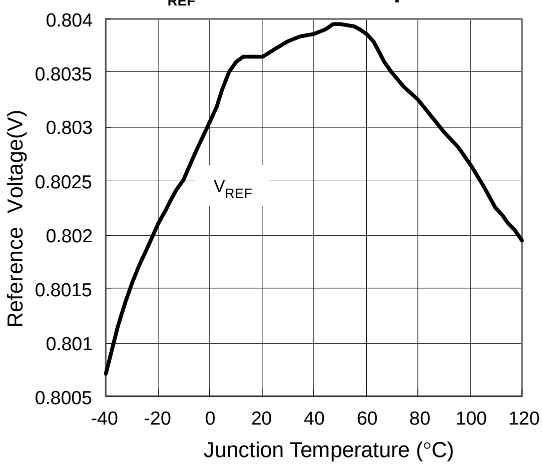
LGATE Source Current vs. LGATE Voltage



LGATE Sink Current vs. LGATE Voltage

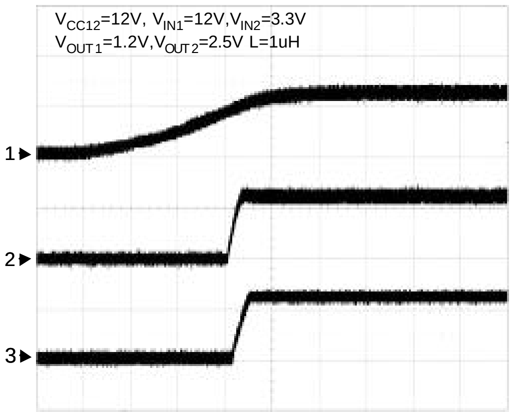


V_{REF} vs. Junction Temperature



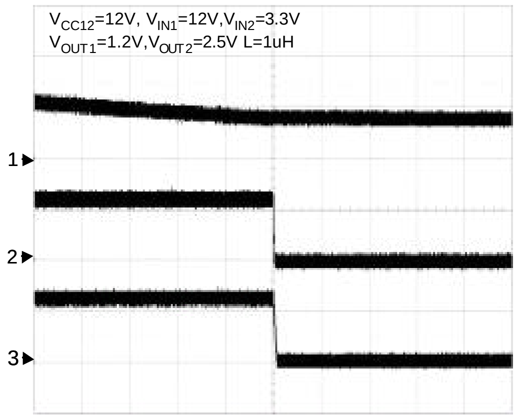
Operating Waveforms

Power On



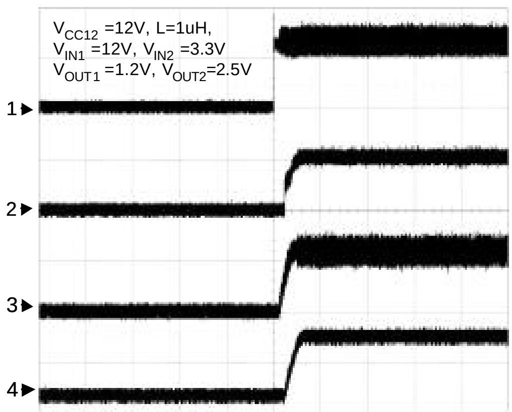
CH1: V_{CC12} (10V/div)
CH2: V_{OUT1} (1V/div)
CH3: V_{OUT2} (2V/div)
Time: 10ms/div

Power Off



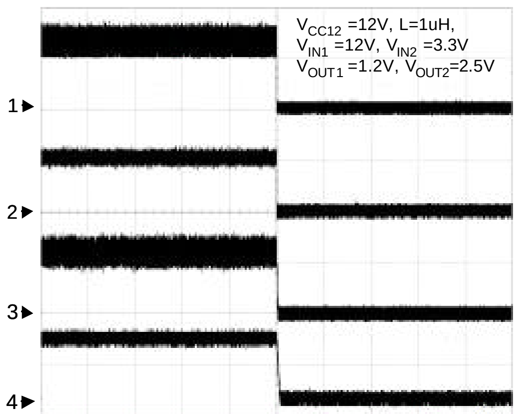
CH1: V_{CC12} (10V/div)
CH2: V_{OUT1} (1V/div)
CH3: V_{OUT2} (2V/div)
Time: 10ms/div

EN



CH1: V_{FS_DIS} (1V/div)
CH2: V_{DRIVE} (5V/div)
CH3: V_{OUT1} (1V/div)
CH4: V_{OUT2} (2V/div)
Time: 10ms/div

Shutdown



CH1: V_{FS_DIS} (1V/div)
CH2: V_{DRIVE} (5V/div)
CH3: V_{OUT1} (1V/div)
CH4: V_{OUT2} (2V/div)
Time: 10ms/div

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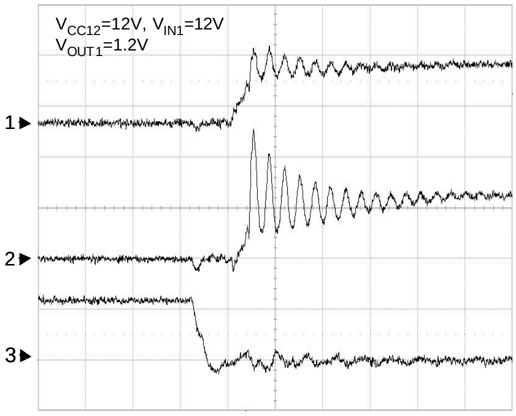
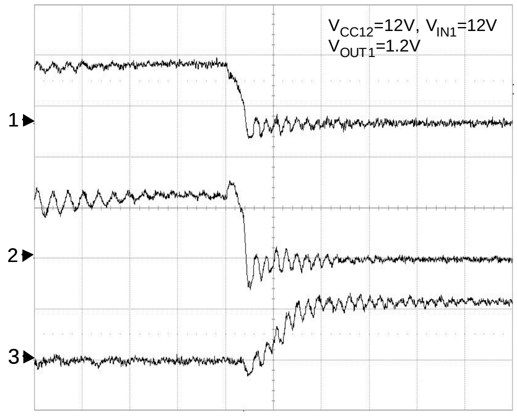
Operating Waveforms (Cont.)

UGATE Rising



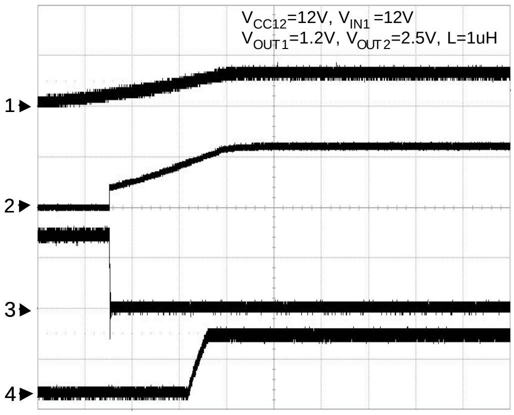
CH1: V_{UGATE} (20V/div)
CH2: V_{PHASE} (10V/div)
CH3: V_{LGATE} (10V/div)
Time: 50ns/div

UGATE Falling



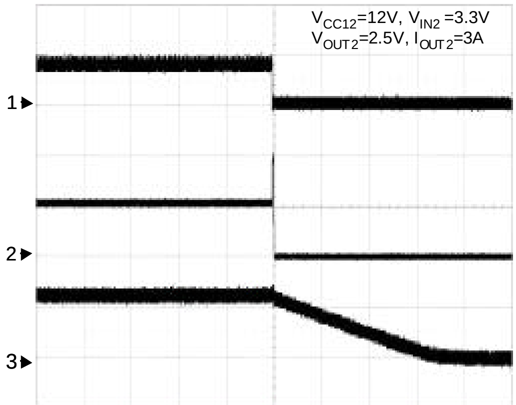
CH1: V_{UGATE} (20V/div)
CH2: V_{PHASE} (10V/div)
CH3: V_{LGATE} (10V/div)
Time: 50ns/div

OVP_PWM Controller (V_{FB} > 135% V_{REF})



CH1: V_{CC12} (1V/div)
CH2: V_{LGATE} (1V/div)
CH3: V_{OUT1} (500mV/div)
CH4: V_{OUT2} (2V/div)
Time: 10ms/div

UVP_Linear Regulator (V_{FBL}< 50% V_{REF})



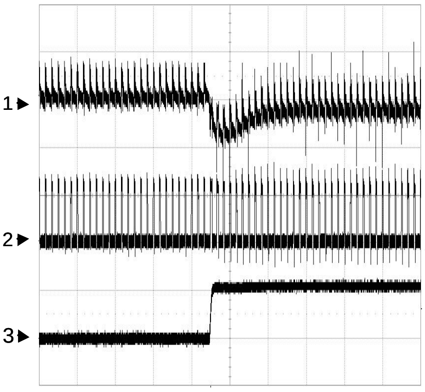
CH1: V_{FBL} (1V/div)
CH2: V_{DRIVE} (5V/div)
CH3: V_{OUT2} (2V/div)
Time: 100μs/div

Operating Waveforms (Cont.)

Load Transient Response (PWM Controller)

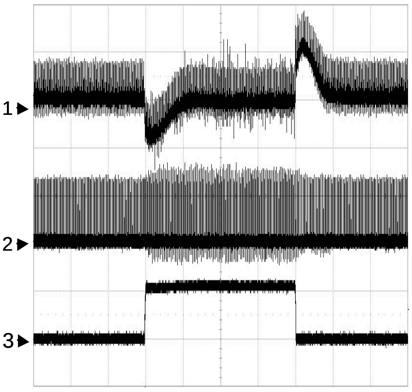
- V_{CC12}=12V, V_{IN1}=12V, V_{OUT1}=2V, F_{OSC}=300kHz
- I_{OUT1} slew rate=±10 A/μs

I_{OUT1}=0A→10A



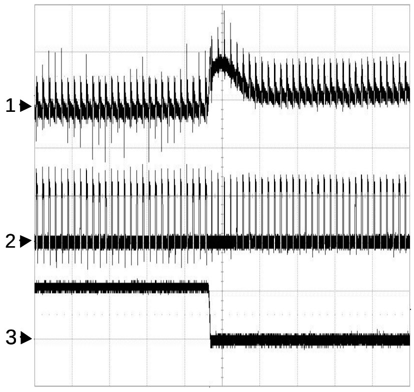
CH1: V_{OUT1} (100mV/div,AC)
CH2: V_{UGATE} (20V/div)
CH3: I_{OUT1} (10A/div)
Time: 20μs/div

I_{OUT1}=0A→10A→0A



CH1: V_{OUT1} (100mV/div,AC)
CH2: V_{UGATE} (20V/div)
CH3: I_{OUT1} (10A/div)
Time: 50μs/div

I_{OUT1}=10A→0A

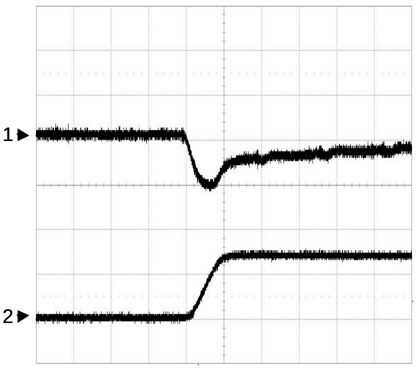


CH1: V_{OUT1} (100mV/div,AC)
CH2: V_{UGATE} (20V/div)
CH3: I_{OUT1} (10A/div)
Time: 20μs/div

Load Transient Response (Linear Regulator)

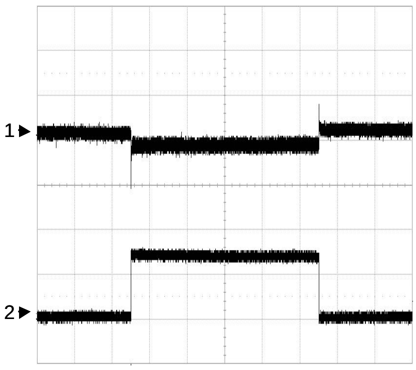
- V_{CC12}=12V, V_{IN2}=3.3V, V_{OUT2}=2.5V
- I_{OUT2} slew rate=±3A/μs

I_{OUT2}=0A→3A



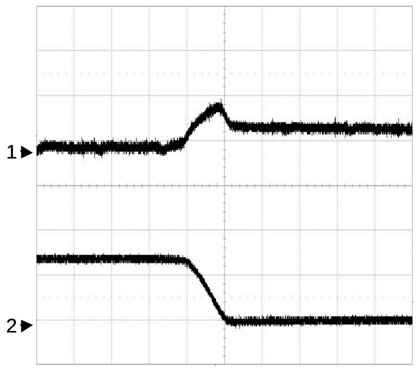
CH1: V_{OUT2} (100mV/div,AC)
CH2: I_{OUT2} (2A/div)
Time: 1μs/div

I_{OUT2}=0A→3A→0A



CH1: V_{OUT2} (100mV/div,AC)
CH2: I_{OUT2} (2A/div)
Time: 10μs/div

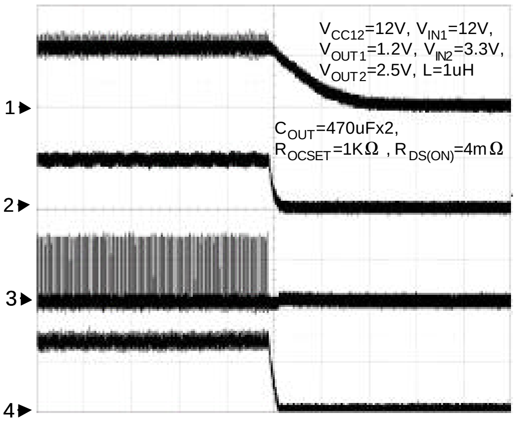
I_{OUT2}=3A→0A



CH1: V_{OUT2} (100mV/div,AC)
CH2: I_{OUT2} (2A/div)
Time: 1μs/div

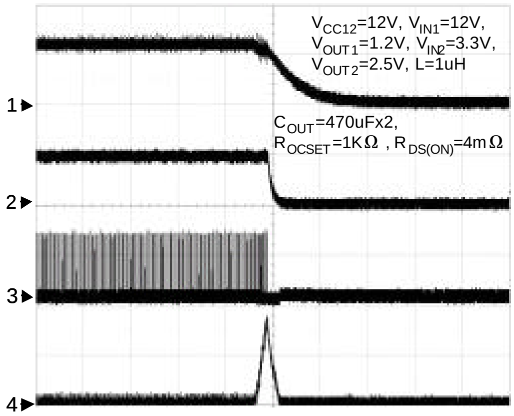
Operating Waveforms (Cont.)

Over Current Protection



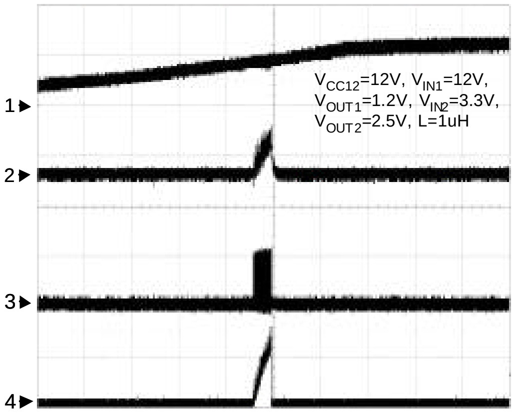
CH1: V_{OUT1} (1V/div)
CH2: V_{DRIVE} (5V/div)
CH3: V_{UGATE} (20V/div)
CH4: IL (10A/div)
Time: 50μs/div

Short Test after Power Ready



CH1: V_{OUT1} (1V/div)
CH2: V_{DRIVE} (5V/div)
CH3: V_{UGATE} (20V/div)
CH4: IL (10A/div)
Time: 50μs/div

Short Test before Power On



CH1: V_{CC12} (10V/div)
CH2: V_{OUT1} (1V/div)
CH3: V_{UGATE} (20V/div)
CH4: IL (10A/div)
Time: 2ms/div

Function Pin Description

VCC12

Power supply input pin. Connect a nominal 12V power supply to this pin. The power-on reset function monitors the input voltage at this pin. It is recommended that a decoupling capacitor (1 to 10µF) be connected to GND for noise decoupling.

BOOT

This pin provides the bootstrap voltage to the upper gate driver for driving the N-channel MOSFET. An external capacitor from PHASE to BOOT, an internal diode, and the power supply valtage V_{CC12}, generates the bootstrap voltage for the upper gate diver (UGATE).

PHASE

This pin is the return path for the upper gate driver. Connect this pin to the upper MOSFET source, and connect a capacitor to BOOT for the bootstrap voltage. This pin is also used to monitor the voltage drop across the lower MOSFET for over-current protection.

GND

This pin is the signal ground pin. Connect the GND pin to a good ground plane.

PGND

This pin is the power ground pin for the lower gate driver. It should be tied to GND pin on the board.

COMP

This pin is the output of PWM error amplifier. It is used to set the compensation components.

FB

This pin is the inverting input of the PWM error amplifier. It is used to set the output voltage and the compensation components. This pin is also monitored for under-voltage protection, when the FB voltage is under 50% of reference voltage (0.4V), both outputs will be shutdowned immediately.

UGATE

This pin is the gate driver for the upper MOSFET of PWM output.

LGATE

This pin is the gate driver for the lower MOSFET of PWM output.

DRIVE

This pin drives the gate of an external N-channel MOSFET for linear regulator. It is also used to set the compensation for some specific applications, for example, with low values of output capacitance and ESR.

FBL

This pin is the inverting input of the linear regulator error amplifier. It is used to set the output voltage. This pin is also monitored for under-voltage protection, when the FBL voltage is under 50% of reference voltage (0.4V), both outputs will be shutdown immediately.

OCSET

Connect a resistor (R_{OCSET}) from this pin to GND, an internal 40µA current source will flow through this resistor and create a voltage drop. When V_{CC12} reaches the POR rising threshold voltage, the voltage drop of R_{OCSET} will be memoried and compared with the voltage across the lower MOSFET. The threshold of the over current limit is therefore given by:

$$I_{LIMIT} = \frac{I_{OCSET} \times R_{OCSET}}{R_{DS(ON)}(Low-Side)}$$

The APW7068 has a internal OCP voltage source, and the value is around 0.25V. When the R_{OCSET} x I_{OCSET} is bigger than 0.25V or the OCSET PIN is floating (no R_{OCSET} resistor), the over current threshold will be the internal default value 0.25V.

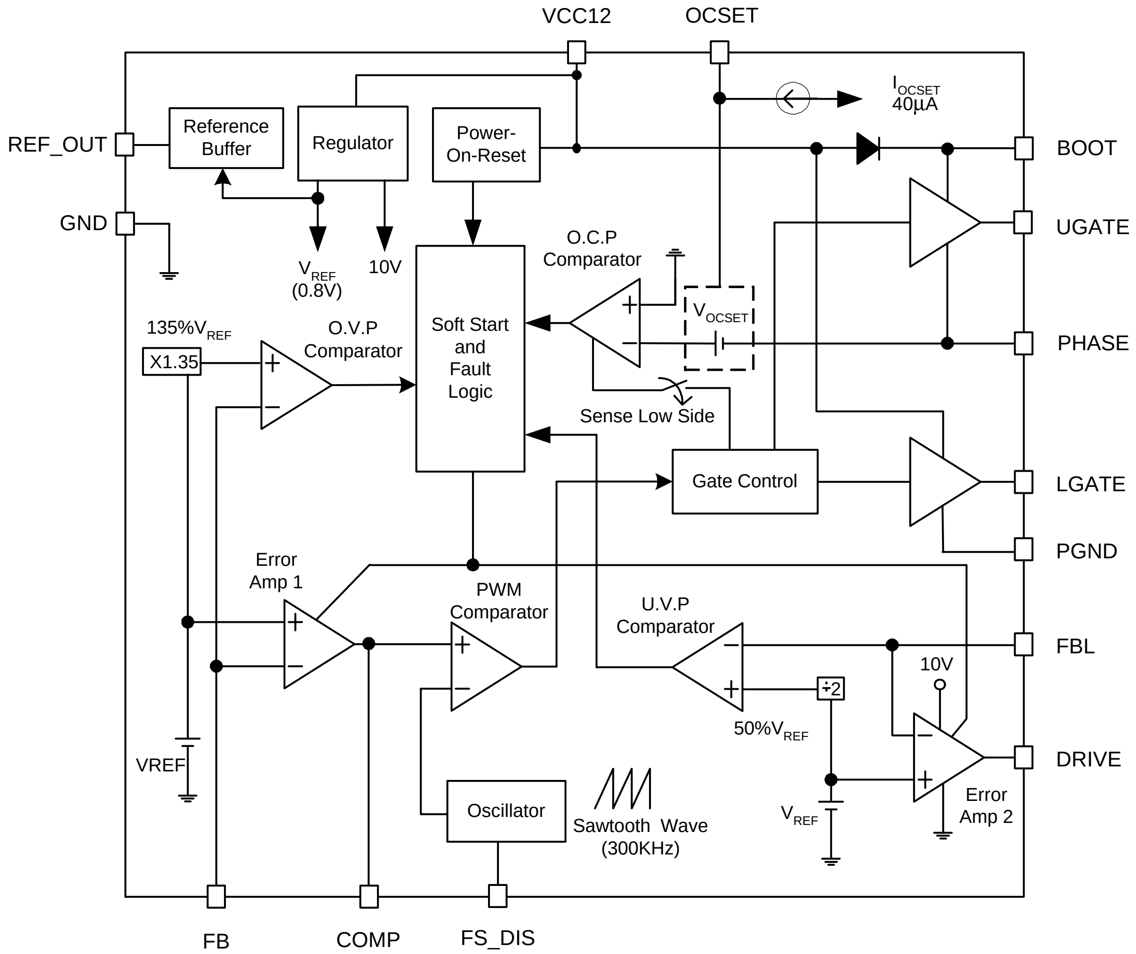
REF_OUT

This pin provides a buffed voltage, which is from internal reference voltage. It is recommended that a 1µF capacitor is connected to ground for stability. When V_{OCSET} is above 1V, the REF_OUT buffer will be closed, the V_{REF_OUT} is 0V.

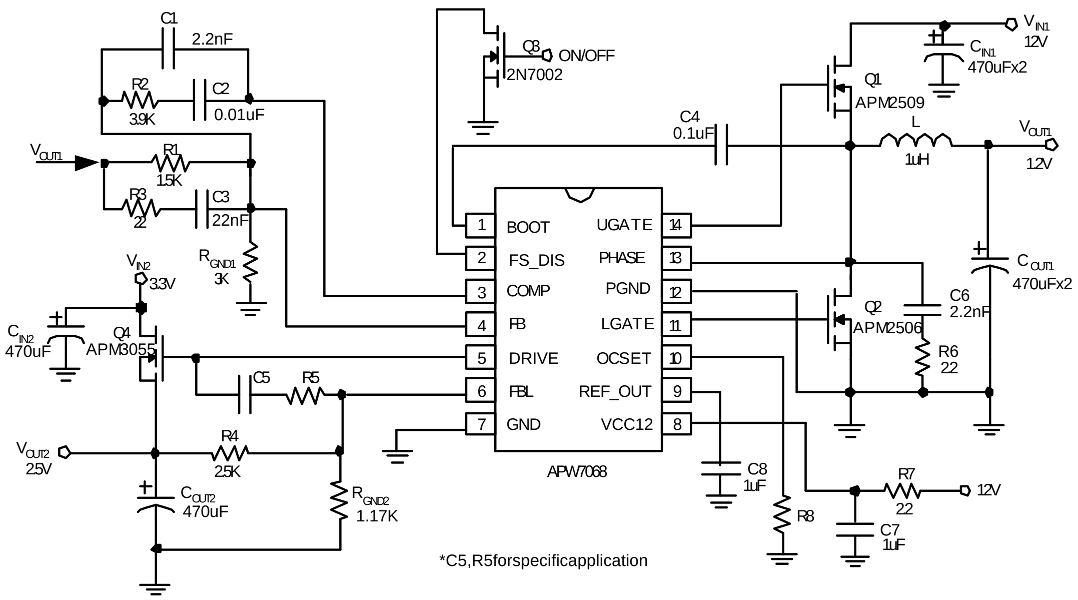
FS_DIS

This pin provides shutdown function. When pulling low the FS_DIS pin near GND will shutdown both regulators; almost any NFET or other pull-down device (< 1k. impedance) should work. Upon release of the FS_DIS pin, it will enable both outputs back into regulation.

Block Diagram



Typical Application Circuits



*C5,R5forspecificapplication

Function Description

Power-On-Reset (POR)

The Power-On-Reset (POR) function of APW7068 continually monitors the input supply voltage (V_{CC12}), ensures the supply voltage exceed its rising POR threshold voltage. The POR function initiates soft-start interval operation while VCC12 voltage exceeds its POR threshold and inhibits operation under disabled status.

Soft-Start

Figure 1. shows the soft-start interval. When V_{CC12} reaches the rising POR threshold voltage, the internal reference voltage is controlled to follow a voltage proportional to the soft-start voltage. The soft-start interval is variable by the oscillator frequency. The formulation is given by:

$$T_{SS} = \Delta(t_2 - t_1) = \frac{1}{F_{OSC}} \times 2560$$

Figure 2. shows more detail of the FB and FBL voltage ramps. The FB and FBL voltage soft-start ramps are formed with many small steps of voltage. The voltage of one step is about 20mV in V_{FB} and V_{FBL}, and the period of one step is about 32/FOSC. This method provides a controlled voltage rise and prevents the large peak current to charge the output capacitors. The FB voltage compares the FBL voltage to shift to an earlier time the establishment as Figure2. The voltage estabilishment time difference for V_{FB} and V_{FBL} is variable by the oscillator. The formulation is given by:

$$\Delta(t_4 - t_3) = \frac{1}{F_{OSC}} \times 640 = \frac{1}{4} \times T_{SS}$$

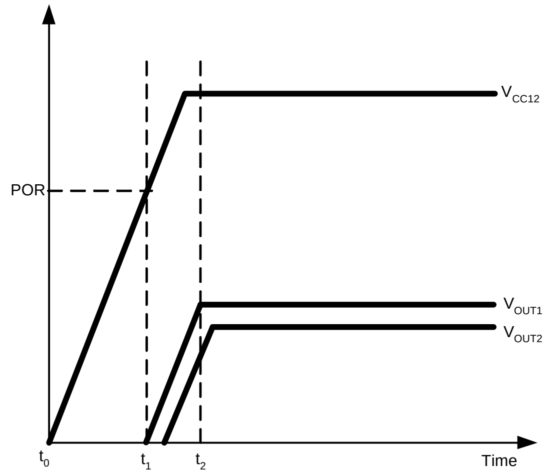


Figure 1. Soft-Start Interval

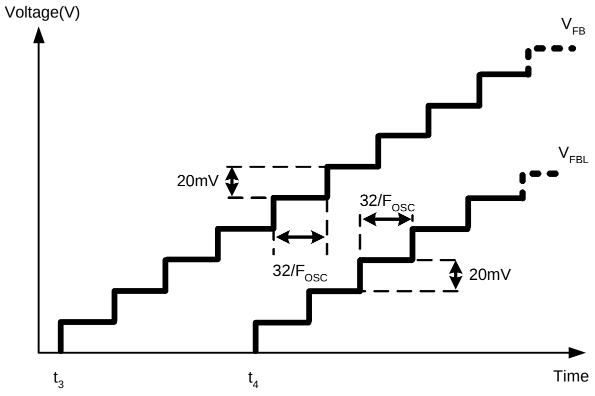


Figure 2. The Controlled Stepped FB and FBL Voltage during Soft-Start

Over-Current Protection

Connect a resistor (R_{OCSET}) from this pin to GND, an internal 40µA current source will flow through this resistor and create a voltage drop, which will be compared with the voltage across the lower MOSFET. When the voltage across the lower MOSFET exceeds the voltage drop across the R_{OCSET}, an over-current condition is detected and the controller will shutdown the IC directly, and the converter's output is latched.

The APW7068 has a internal OCP voltage source, and the value is around 0.25V. When the R_{OCSET} x I_{OCSET} is bigger than 0.25V or the OCSET PIN is floating (no R_{OCSET} resistor), the over current threshold will be the internal default value 0.25V.

The threshold of the over current limit is therefore given by:

$$I_{LIMIT} = \frac{I_{OCSET} \times R_{OCSET}}{R_{DS(ON)}(Low - Side)}$$

For the over-current is never occurred in the normal operating load range; the variation of all parameters in the above equation should be determined.

- The MOSFET's $R_{DS(ON)}$ is varied by temperature and gate to source voltage, the user should determine the maximum $R_{DS(ON)}$ in manufacturer's datasheet.
- The minimum I_{OCSET} (36uA) and minimum R_{OCSET} should be used in the above equation.
- Note that the I_{LIMIT} is the current flow through the lower MOSFET; I_{LIMIT} must be greater than maximum output current add the half of inductor ripple current.

Function Description (Cont.)

Over-Current Protection (Cont.)

When OCSET PIN is floating, the V_{OCSET} will be pulled high and the over current threshold will be the internal default value 0.25V. When the voltage drop across the lower MOSFET's $R_{DS(ON)}$ is larger than 0.25V, an over-current condition is detected, the controller will shutdown the IC directly, and latch the converter's output.

Over Voltage Protection

The FB pin is monitored during converter operation by its own Over Voltage(OV) comparator. If the FB voltage is over 135% of the reference voltage, the controller will make Low-Side gate signal fully turn on until the fault events are removed.

Under Voltage Protection

The FBL pin is monitored during converter operation by its own Under Voltage (UV) comparator. If the FBL voltage drop below 50% of the reference voltage (50% of 0.8V = 0.4V), a fault signal is internally generated, and the device turns off both high-side and low-side MOSFET and the converter's output is latched to be floating. The controller will shutdown the IC directly.

Shutdown and Enable

Pulling low the FS_DIS pin near GND by an open drain transistor or other pull-down device (< 1k. impedance) will shutdown both regulators. Upon release of the FS_DIS pin, it will enable both outputs back into regulation. In shutdown mode, the UGATE and LGATE turn off and pull to PHASE and GND respectively.

Application Information

Output Voltage Selection

The output voltage of PWM converter can be programmed with a resistive divider. Use 1% or better resistors for the resistive divider is recommended. The FB pin is the inverter input of the error amplifier, and the reference voltage is 0.8V. The output voltage is determined by:

$$V_{OUT1} = 0.8 \times \left(1 + \frac{R1}{R_{GND1}}\right)$$

Where R1 is the resistor connected from V_{OUT1} to FB and R_{GND1} is the resistor connected from FB to GND.

The linear regulator output voltage V_{OUT2} is also set by means of an external resistor divider. The FBL pin is the inverter input of the error amplifier, and the reference voltage is 0.8V. The output voltage is determined by:

$$V_{OUT2} = 0.8 \times \left(1 + \frac{R4}{R_{GND2}}\right)$$

Where R4 is the resistor connected from V_{OUT2} to FBL and R_{GND2} is the resistor connected from FBL to GND.

Linear Regulator Input/Output Capacitor Selection

The input capacitor is chosen based on its voltage rating. Under load transient condition, the input capacitor will momentarily supply the required transient current. The output capacitor for the linear regulator is chosen to minimize any droop during load transient condition. In addition, the capacitor is chosen based on its voltage rating.

Linear Regulator Input/Output MOSFET Selection

The maximum DRIVE voltage is about 10V when V_{CC12} is equal 12V. Since this pin drives an external N-channel MOSFET, therefore the maximum output voltage of the linear regulator is dependent upon the V_{GS}.

$$V_{OUT2MAX} = 10 - V_{GS}$$

Another criterion is its efficiency of heat removal. The power dissipated by the MOSFET is given by:

$$P_D = I_{OUT2} \times (V_{IN2} - V_{OUT2})$$

Where I_{OUT2} is the maximum load current, V_{OUT2} is the nominal output voltage.

In some applications, heatsink might be required to help maintain the junction temperature of the MOSFET below its maximum rating.

Linear Regulator Compensation Selection

The linear regulator is stable over all loads current. However, the transient response can be further enhanced by connecting a RC network between the FBL and DRIVE pin. Depending on the output capacitance and load current of the application, the value of this RC network is then varied.

PWM Compensation

The output LC filter of a step down converter introduces a double pole, which contributes with -40dB/decade gain slope and 180 degrees phase shift in the control loop. A

Application Information (Cont.)

PWM Compensation (Cont.)

compensation network among COMP, FB and V_{OUT1} should be added. The compensation network is shown in Figure 6. The output LC filter consists of the output inductor and output capacitors. The transfer function of the LC filter is given by:

$$GAIN_{LC} = \frac{1 + s \times ESR \times C_{OUT1}}{s^2 \times L \times C_{OUT1} + s \times ESR \times C_{OUT1} + 1}$$

The poles and zero of this transfer functions are:

$$F_{LC} = \frac{1}{2 \times \pi \times \sqrt{L \times C_{OUT1}}}$$

$$F_{ESR} = \frac{1}{2 \times \pi \times ESR \times C_{OUT1}}$$

The F_{LC} is the double poles of the LC filter, and F_{ESR} is the zero introduced by the ESR of the output capacitor.

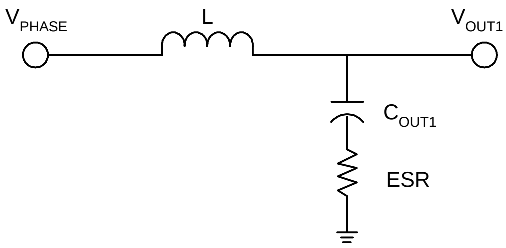


Figure 3. The Output LC Filter

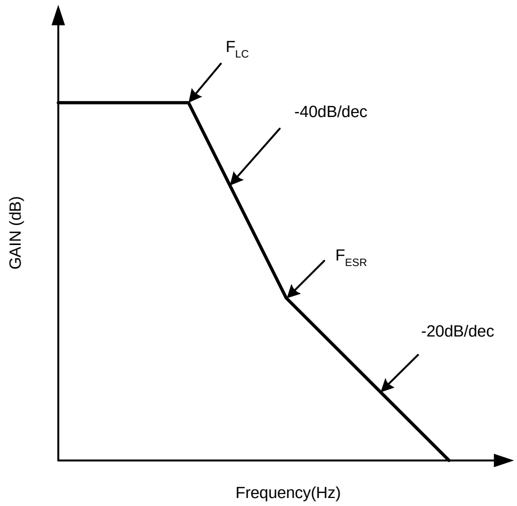


Figure 4. The LC Filter GAIN and Frequency

The PWM modulator is shown in Figure 5. The input is the output of the error amplifier and the output is the PHASE node. The transfer function of the PWM modulator is given by:

$$GAIN_{PWM} = \frac{V_{IN}}{\Delta V_{OSC}}$$

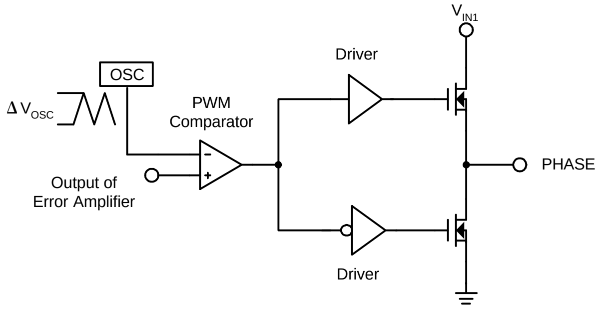


Figure 5. The PWM Modulator

The compensation network is shown in Figure 6. It provides a close loop transfer function with the highest zero crossover frequency and sufficient phase margin.

The transfer function of error amplifier is given by:

$$GAIN_{AMP} = \frac{V_{COMP}}{V_{OUT1}} = \frac{\frac{1}{sC1} // \left(R2 + \frac{1}{sC2}\right)}{R1 // \left(R3 + \frac{1}{sC3}\right)}$$

$$= \frac{R1 + R3}{R1 \times R3 \times C1} \times \frac{\left(s + \frac{1}{R2 \times C2}\right) \times \left(s + \frac{1}{(R1 + R3) \times C3}\right)}{s\left(s + \frac{C1 + C2}{R2 \times C1 \times C2}\right) \times \left(s + \frac{1}{R3 \times C3}\right)}$$

The poles and zeros of the transfer function are:

$$F_{Z1} = \frac{1}{2 \times \pi \times R2 \times C2}$$

$$F_{Z2} = \frac{1}{2 \times \pi \times (R1 + R3) \times C3}$$

$$F_{P1} = \frac{1}{2 \times \pi \times R2 \times \left(\frac{C1 \times C2}{C1 + C2}\right)}$$

$$F_{P2} = \frac{1}{2 \times \pi \times R3 \times C3}$$

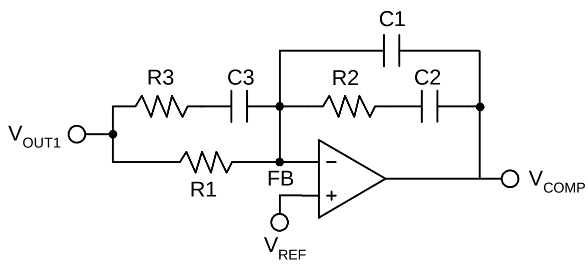


Figure 6. Compensation Network

Application Information (Cont.)

PWM Compensation (Cont.)

The closed loop gain of the converter can be written as:

$GAIN_{LC}$ X $GAIN_{PWM}$ X $GAIN_{AMP}$

Figure 7. shows the asymptotic plot of the closed loop converter gain, and the following guidelines will help to design the compensation network. Using the below guidelines should give a compensation similar to the curve plotted. A stable closed loop has a -20dB/ decade slope and a phase margin greater than 45 degree.

1. Choose a value for R1, usually between 1K and 5K.

2. Select the desired zero crossover frequency

F_O: (1/5 ~ 1/10) X $F_S > F_O > F_{ESR}$

Use the following equation to calculate R2:

$$R2 = \frac{\Delta V_{OSC}}{V_{IN}} \times \frac{F_O}{F_{LC}} \times R1$$

3. Place the first zero F_{Z1} before the output LC filter double pole frequency F_{LC}.

F_{Z1} = 0.75 X F_{LC}

Calculate the C2 by the equation:

$$C2 = \frac{1}{2 \times \pi \times R2 \times F_{LC} \times 0.75}$$

4. Set the pole at the ESR zero frequency F_{ESR}:

$F_{P1} = F_{ESR}$

Calculate the C1 by the equation:

$$C1 = \frac{C2}{2 \times \pi \times R2 \times C2 \times F_{ESR} - 1}$$

5. Set the second pole F_{P2} at the half of the switching frequency and also set the second zero F_{Z2} at the output LC filter double pole F_{LC}. The compensation gain should not exceed the error amplifier open loop gain, check the compensation gain at F_{P2} with the capabilities of the error amplifier.

F_{P2} = 0.5 X F_S

$F_{Z2} = F_{LC}$

Combine the two equations will get the following component calculations:

$$R3 = \frac{R1}{\frac{F_S}{2 \times F_{LC}} - 1}$$

$$C3 = \frac{1}{\pi \times R3 \times F_S}$$

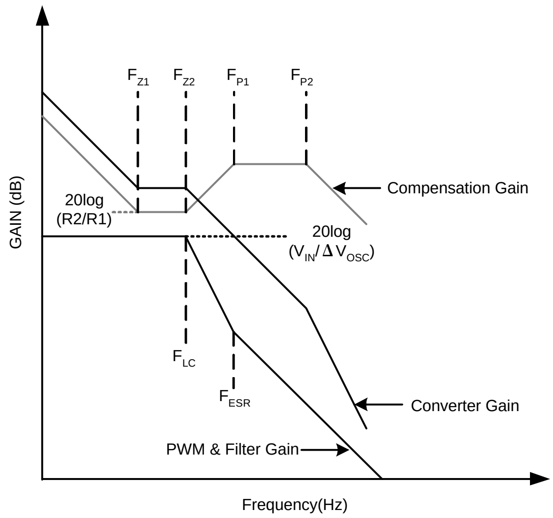


Figure 7. Converter Gain and Frequency

Output Inductor Selection

The inductor value determines the inductor ripple current and affects the load transient response. Higher inductor value reduces the inductor's ripple current and induces lower output ripple voltage. The ripple current and ripple voltage can be approximated by:

$$I_{RIPPLE} = \frac{V_{IN1} - V_{OUT1}}{F_S \times L} \times \frac{V_{OUT1}}{V_{IN1}}$$

$$\Delta V_{OUT1} = I_{RIPPLE} \times ESR$$

where F_S is the switching frequency of the regulator.

Although increase of the inductor value and frequency reduces the ripple current and voltage, a tradeoff will exist between the inductor's ripple current and the regulator load transient response time.

A smaller inductor will give the regulator a faster load transient response at the expense of higher ripple current. Increasing the switching frequency (F_S) also reduces the ripple current and voltage, but it will increase the switching loss of the MOSFET and the power dissipation of the converter. The maximum ripple current occurs at the maximum input voltage. A good starting point is to choose the ripple current to be approximately 30% of the maximum output current. Once the inductance value has been chosen, select an inductor that is capable of carrying the required peak current without going into

Application Information (Cont.)

Output Inductor Selection (Cont.)

saturation. In some types of inductors, especially core that is made of ferrite, the ripple current will increase abruptly when it saturates. This will result in a larger output ripple voltage.

Output Capacitor Selection

Higher capacitor value and lower ESR reduce the output ripple and the load transient drop. Therefore, selecting high performance low ESR capacitors is intended for switching regulator applications. In some applications, multiple capacitors have to be parallel to achieve the desired ESR value. A small decoupling capacitor in parallel for bypassing the noise is also recommended, and the voltage rating of the output capacitors also must be considered. If tantalum capacitors are used, make sure they are surge tested by the manufactures. If in doubt, consult the capacitors manufacturer.

Input Capacitor Selection

The input capacitor is chosen based on the voltage rating and the RMS current rating. For reliable operation, select the capacitor voltage rating to be at least 1.3 times higher than the maximum input voltage. The maximum RMS current rating requirement is approximately $I_{OUT1}/2$, where I_{OUT1} is the load current. During power up, the input capacitors have to handle large amount of surge current. If tantalum capacitors are used, make sure they are surge tested by the manufactures. If in doubt, consult the capacitors manufacturer. For high frequency decoupling, a ceramic capacitor 1uF can be connected between the drain of upper MOSFET and the source of lower MOSFET.

MOSFET Selection

The selection of the N-channel power MOSFETs are determined by the $R_{DS(ON)}$, reverse transfer capacitance (C_{RSS}) and maximum output current requirement. There are two components of loss in the MOSFETs: conduction loss and transition loss. For the upper and lower MOSFET, the losses are approximately given by the following:

$$P_{UPPER} = I_{OUT1}^{2}(1+TC)(R_{DS(ON)})D + (0.5)(I_{OUT1})(V_{IN1})(t_{SW})F_S$$

$$P_{LOWER} = I_{OUT1}^{2}(1+TC)(R_{DS(ON)})(1-D)$$

Where I_{OUT1} is the load current

TC is the temperature dependency of $R_{DS(ON)}$

F_S is the switching frequency

t_{SW} is the switching interval

D is the duty cycle

Note that both MOSFETs have conduction loss while the upper MOSFET include an additional transition loss. The switching internal, t_{SW}, is a function of the reverse transfer capacitance C_{RSS}. The (1+TC) term is to factor in the temperature dependency of the $R_{DS(ON)}$ and can be extracted from the "$R_{DS(ON)}$ vs Temperature" curve of the power MOSFET.

Layout Consideration

In any high switching frequency converter, a correct layout is important to ensure proper operation of the regulator. With power devices switching at 300kHz or above, the resulting current transient will cause voltage spike across the interconnecting impedance and parasitic circuit elements. As an example, consider the turn-off transition of the PWM MOSFET. Before turn-off, the MOSFET is carrying the full load current. During turn-off, current stops flowing in the MOSFET and is free-wheeling by the lower MOSFET and parasitic diode. Any parasitic inductance of the circuit generates a large voltage spike during the switching interval. In general, using short, wide printed circuit traces should minimize interconnecting impedances and the magnitude of voltage spike. And signal and power grounds are to be kept separate till combined using ground plane construction or single point grounding. Figure 8. illustrates the layout, with bold lines indicating high current paths; these traces must be short and wide. Components along the bold lines should be placed lose together. Below is a checklist for your layout:

- The metal plate of the bottom of the packages (QFN-16) must be soldered to the PCB and connected to the GND plane on the backside through several thermal vias.

- Keep the switching nodes (UGATE, LGATE and PHASE) away from sensitive small signal nodes since these nodes are fast moving signals. Therefore, keep traces to these nodes as short as possible.

- The traces from the gate drivers to the MOSFETs (UG, LG, DRIVE) should be short and wide.

- Place the source of the high-side MOSFET and the drain of the low-side MOSFET as close as possible. Minimizing the impedance with wide layout plane between the two pads reduces the voltage bounce of the node.

- Decoupling capacitor, compensation component, the resistor dividers and boot capacitors should be close their pins. (For example, place the decoupling ceramic capacitor near the drain of the high-side MOSFET as close as possible. The bulk capacitors are also placed near the drain).

- The input capacitor should be near the drain of the upper MOSFET; the output capacitor should be near the loads. The input capacitor GND should be close to the output capacitor GND and the lower MOSFET GND.

- The drain of the MOSFETs (V_{IN1} and PHASE nodes) should be a large plane for heat sinking.

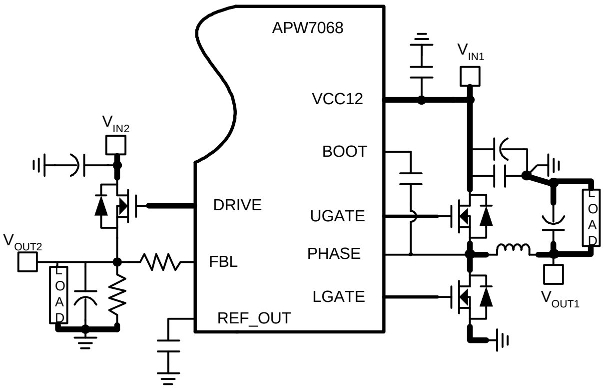
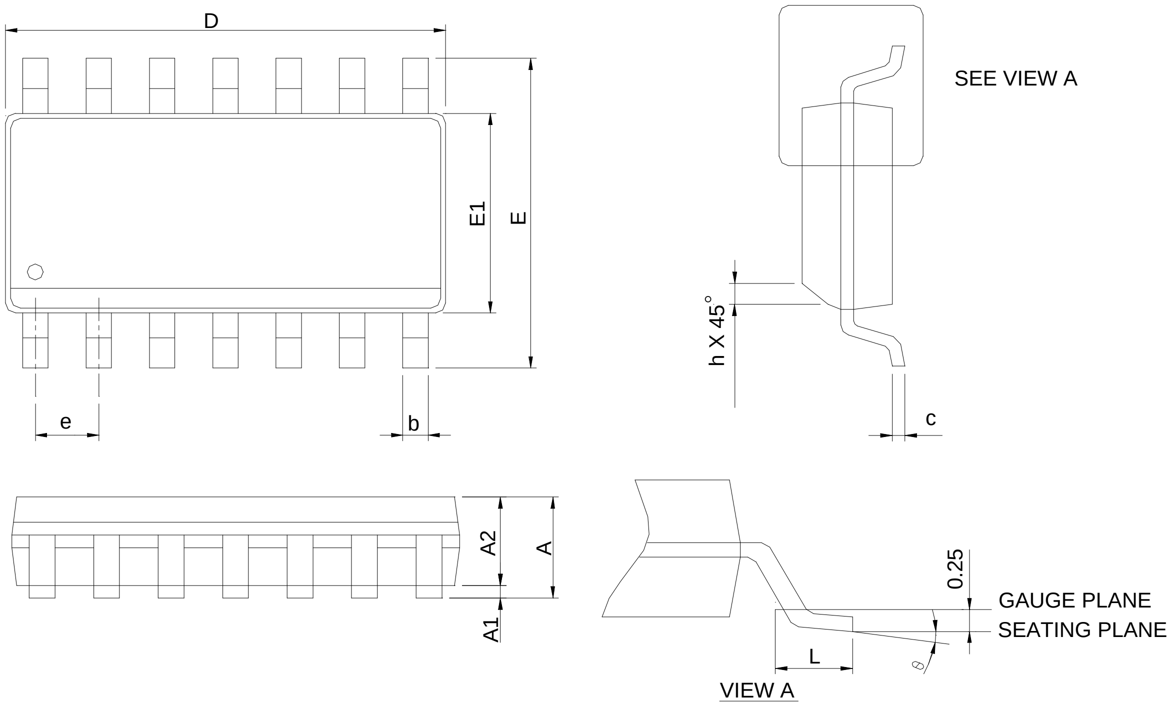


Figure 8. Layout Guidelines

Package Information

SOP – 14

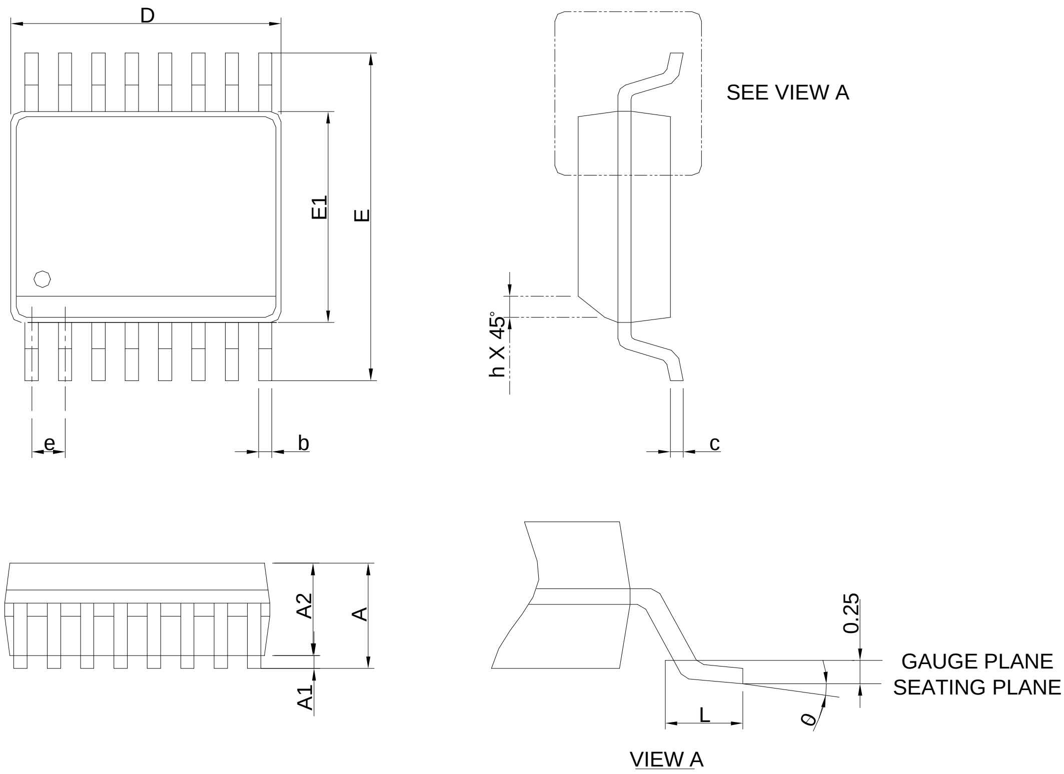


SYMBOL	SOP-14			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A		1.75		0.069
A1	0.10	0.25	0.004	0.010
A2	1.25		0.049	
b	0.31	0.51	0.012	0.020
c	0.17	0.25	0.007	0.010
D	8.55	8.75	0.337	0.344
E	5.80	6.20	0.228	0.244
E1	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
h	0.25	0.50	0.010	0.020
L	0.40	1.27	0.016	0.050
θ	0°	8°	0°	8°

Note: 1. Follow JEDEC MS-012 AB.
2. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion or gate burrs shall not exceed 6 mil per side.
3. Dimension "E" does not include inter-lead flash or protrusions. Inter-lead flash and protrusions shall not exceed 10 mil per side.

Package Information

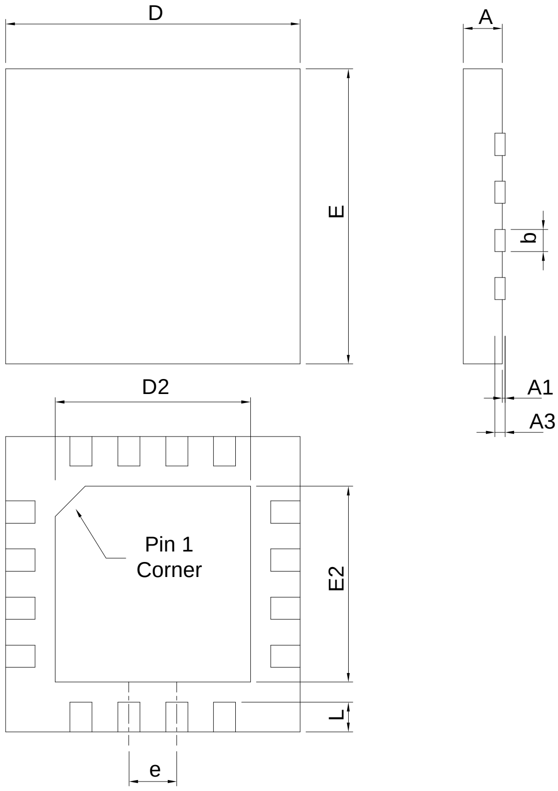
QSOP-16



SYMBOL	QSOP-16			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A		1.75		0.069
A1	0.10	0.25	0.004	0.010
A2	1.24		0.049	
b	0.20	0.30	0.008	0.012
c	0.15	0.25	0.006	0.010
D	4.90 BSC		0.193 BSC	
E	5.99 BSC		0.236 BSC	
E1	3.91 BSC		0.154 BSC	
e	0.635 BSC		0.025 BSC	
L	0.40	1.27	0.016	0.050
h	0.25	0.50	0.010	0.020
θ	0°	8°	0°	8°

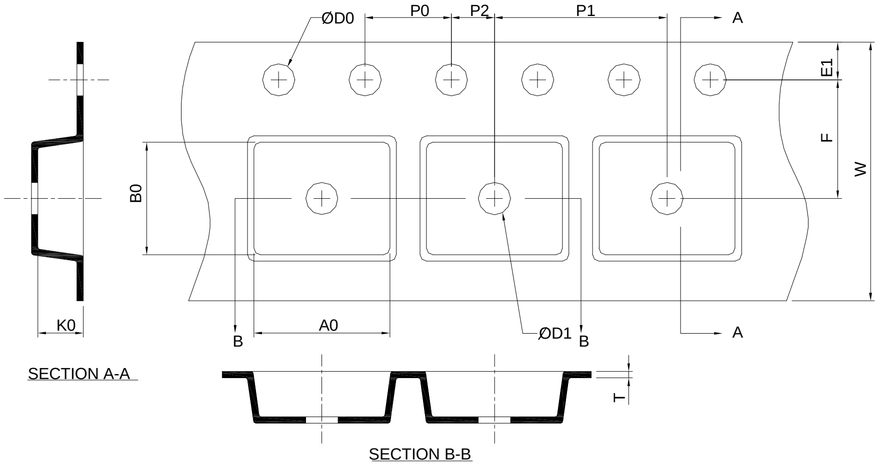
Package Information

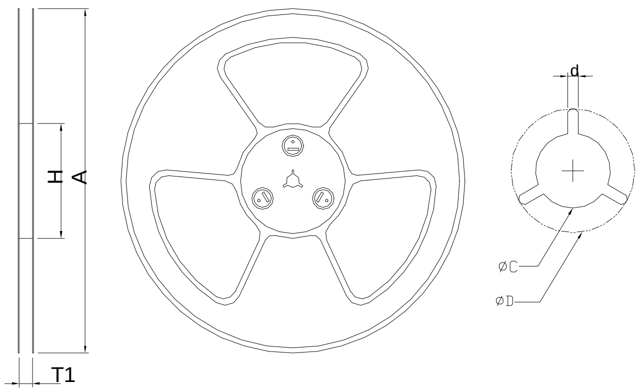
QFN4x4-16



SYMBOL	QFN4x4-16			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	0.80	1.00	0.031	0.039
A1	0.00	0.05	0.000	0.002
A3	0.20 REF		0.008 REF	
b	0.25	0.35	0.010	0.014
D	4.00 BSC		0.157 BSC	
D2	2.50	2.80	0.098	0.110
E	4.00 BSC		0.157 BSC	
E2	2.50	2.80	0.098	0.110
e	0.65 BSC		0.026 BSC	
L	0.30	0.50	0.012	0.020

Carrier Tape & Reel Dimensions





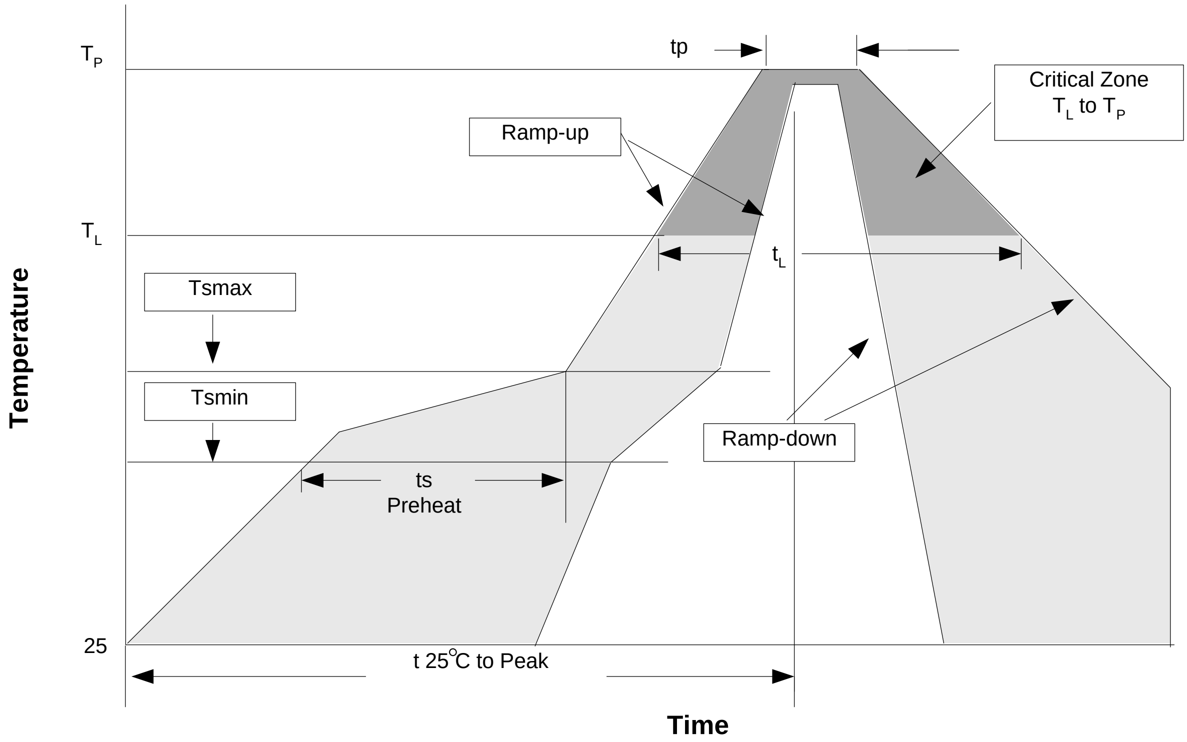
Application	A	H	T1	C	d	D	W	E1	F
SOP-14	330.0±2.00	50 MIN.	16.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	16.0±0.30	1.75±0.10	7.50±0.05
	P0	**P1**	**P2**	**D0**	**D1**	**T**	**A0**	**B0**	**K0**
	4.0±0.10	8.0±0.10	2.0±0.05	1.5+0.10 -0.00	1.5 MIN.	0.6+0.00 -0.40	6.40±0.20	9.00±0.20	2.10±0.20
Application	**A**	**H**	**T1**	**C**	**d**	**D**	**W**	**E1**	**F**
QSOP- 16	330 ± 1	62 +1.5	12.75+ 0.15	2 ± 0.5	12.4 ± 0.2	2 ± 0.2	12± 0. 3	8± 0.1	1.75±0.1
	P0	**P1**	**P2**	**D0**	**D1**	**T**	**A0**	**B0**	**K0**
	5.5± 1	1.55 +0.1	1.55+ 0.25	4.0 ± 0.1	2.0 ± 0.1	6.4 ± 0.1	5.2± 0. 1	2.1± 0.1	0.3±0.013
Application	**A**	**H**	**T1**	**C**	**d**	**D**	**W**	**E1**	**F**
QFN4x4-16	330.0±2.00	50 MIN.	12.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	12.0±0.30	1.75±0.10	5.5±0.10
	P0	**P1**	**P2**	**D0**	**D1**	**T**	**A0**	**B0**	**K0**
	4.0±0.10	8.0±0.10	2.0±0.10	1.5+0.10 -0.00	1.5 MIN.	0.6+0.00 -0.40	4.35±0.20	4.35±0.20	1.1±0.20

(mm)

Devices Per Unit

Package Type	Unit	Quantity
SOP- 14	Tape & Reel	2500
QSOP- 16	Tape & Reel	2500
QFN4x4-16	Tape & Reel	3000

Reflow Condition (IR/Convection or VPR Reflow)



Reliability Test Program

Test item	Method	Description
SOLDERABILITY	MIL-STD-883D-2003	245°C, 5 SEC
HOLT	MIL-STD-883D-1005.7	1000 Hrs Bias @125°C
PCT	JESD-22-B,A102	168 Hrs, 100%RH, 121°C
TST	MIL-STD-883D-1011.9	-65°C~150°C, 200 Cycles
ESD	MIL-STD-883D-3015.7	VHBM > 2KV, VMM > 200V
Latch-Up	JESD 78	10ms, 1_{tr} > 100mA

Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Average ramp-up rate (T_L to T_P)	3°C/second max.	3°C/second max.
Preheat - Temperature Min (Tsmin) - Temperature Max (Tsmax) - Time (min to max) (ts)	 100°C 150°C 60-120 seconds	 150°C 200°C 60-180 seconds
Time maintained above: - Temperature (T_L) - Time (t_L)	 183°C 60-150 seconds	 217°C 60-150 seconds
Peak/Classificatioon Temperature (Tp)	See table 1	See table 2
Time within 5°C of actual Peak Temperature (tp)	10-30 seconds	20-40 seconds
Ramp-down Rate	6°C/second max.	6°C/second max.
Time 25°C to Peak Temperature	6 minutes max.	8 minutes max.

Notes: All temperatures refer to topside of the package. Measured on the body surface.

Table 1. SnPb Entectic Process – Package Peak Reflow Temperatures

Package Thickness	Volume mm^3 <350	Volume mm^3 ^{3}350
<2.5 mm	240 +0/-5°C	225 +0/-5°C
≥2.5 mm	225 +0/-5°C	225 +0/-5°C

Table 2. Pb-free Process – Package Classification Reflow Temperatures

Package Thickness	Volume mm^3 <350	Volume mm^3 350-2000	Volume mm^3 >2000
<1.6 mm	260 +0°C*	260 +0°C*	260 +0°C*
1.6 mm – 2.5 mm	260 +0°C*	250 +0°C*	245 +0°C*
≥2.5 mm	250 +0°C*	245 +0°C*	245 +0°C*

* Tolerance: The device manufacturer/supplier **shall** assure process compatibility up to and including the stated classification temperature (this means Peak reflow temperature +0°C. For example 260°C+0°C) at the rated MSL level.

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