DATASHEET

(DEVICE : WS1213, 4x4 **JAPAN CDMA** PAM)

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Power Amplifier Module for J-CDMA(887-925MHz)

The WS1213 is a CDMA(Code Division Multiple Access) power amplifier module designed for handsets operating in the 887-925MHz bandwidth. The WS1213 is manufactured on an advanced InGaP HBT (Hetero-junction Bipolar Transistor) MMIC(Microwave Monolithic Integrated Circuit) technology offering state-of-the-art reliability, temperature stability and ruggedness.
The WS1213 meets stringent CDMA linearity requirements to and beyond 27.5dBm output power.
The 4mmx4mm form factor 10-pin surface mount package is self contained, incorporating 50ohm input and output matching networks.

General Features

- 3.0um InGaP HBT Technology
- Good Linearity
- High Efficiency
- 10-pin Surface Mounting Package(4mmx4mmx1.4mm)
- 50ohm Input and Output Matching
- CDMA 95A/B, CDMA2000-1X/EVDO

Applications

- Digital Cellular(J-CDMA)

Functional Block Diagram

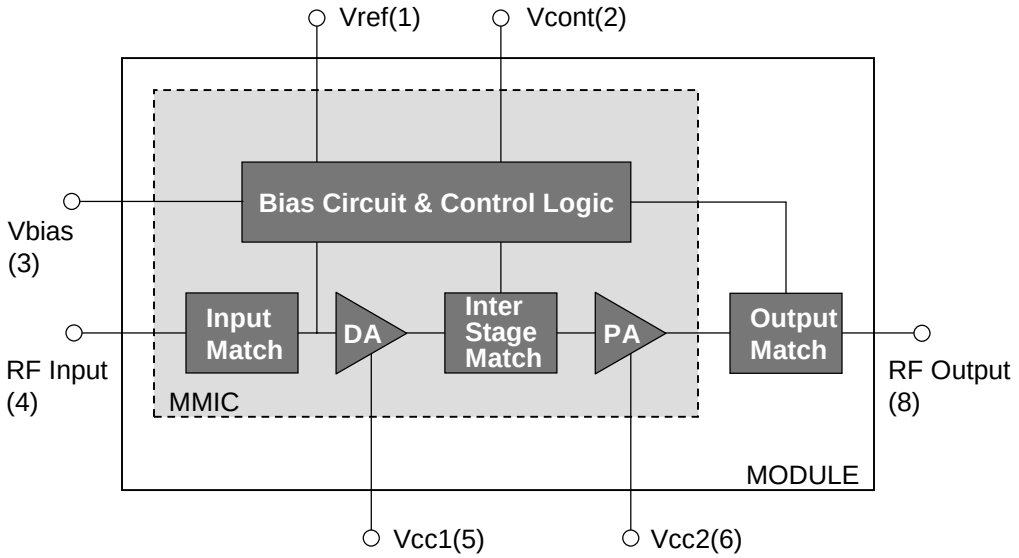


Table 1. Absolute Maximum Ratings

Parameter	Symbol	Minimum	Nominal	Maximum	Unit
RF Input Power	Pin	-	-	10.0	dBm
DC Supply Voltage	Vcc	-	3.4	6.0	V
DC Reference Voltage	Vref	-	2.85	3.3	V
Case Operating Temperature	Tc	-30	25	+110	°C
Storage Temperature	Tstg	-55	-	+125	°C

Table 2. Recommended Operating Conditions

Parameter	Symbol	Minimum	Nominal	Maximum	Unit
DC Supply Voltage	Vcc	3.2	3.4	4.2	V
DC Reference Voltage	Vref	2.75	2.85	2.95	V
Bias Supply Voltage	Vbias	2.75	2.85	4.2	V
Mode Control Voltage - High Power Mode - Low Power Mode	 Vcont Vcont	 - -	 0 2.85	 - -	 V V
Operating Frequency	Fo	887	-	925	MHz
Case Operating Temperature	To	-30	-	85	°C

Table 3. Power Range Truth Table

Power Mode	Symbol	Vref	Vcont*1	Range
High Power*2	PR2	2.85	Low	16dBm – 27.5dBm
Low Power*2	PR1	2.85	High	< 16dBm
Shut Down*3	-	0	-	-

*1 High(2.0V – 3.0V), Low(0.0V – 0.5V)
*2 To change between High Power Mode and Low Power Mode, switch Vcont accordingly
*3 In order to shut down the module, turn off Vref accordingly

Table 4. Electrical Characteristics for CDMA (Vcc=3.4V, Vref=2.85V)

Characteristics		Symbol	Condition	Min	Typ	Max	Unit
Gain		G1	Pout=16dBm	15	18		dB
		G2	Pout=27.5dBm	25	28		dB
Power Added Efficiency		PAE1	Pout=16dBm		18		%
		PAE2	Pout=27.5dBm		39		%
Total Supply Current		Icc1	Pout=16dBm		65		mA
		Icc2	Pout=27.5dBm		420		mA
Quiescent Current 1		Iq1	Low Power Mode		14		mA
		Iq2	High Power Mode		90		mA
Reference Current		Iref1	Pout=16dBm		5		mA
		Iref2	Pout=27.5dBm		3		mA
Control Current		Icont	Pout=16dBm		0.15		mA
Total Supply Current in Power-down Mode		Ipd	Vcc=3.4 Vref=0		0.5	5	uA
Adjacent Channel Power 1 *1	885KHz offset	ACPR1 low	Pout=16dBm		-52		dBc
	1.98MHz offset	ACPR2 low			-62		dBc
Adjacent Channel Power 2 *1	885KHz offset	ACPR1 high	Pout=27.5dBm		-52		dBc
	1.98MHz offset	ACPR2 high			-61		dBc
Harmonic Suppression	Second	2f0			-35		dBc
	Third	3f0			-55		dBc
Input VSWR		VSWR			2:1	2.5:1	
Stability (Spurious Output)		S	VSWR 6:1			-60	dBc
Rx Band Noise Power		RxBN	Pout=27.5dBm		-135		dBm/Hz
Ruggedness		Ru	No damage			10:1	VSWR

*1 Adjacent channel power is measured using IS-95 modulated input signal

Figure 1. Evaluation Board Schematic

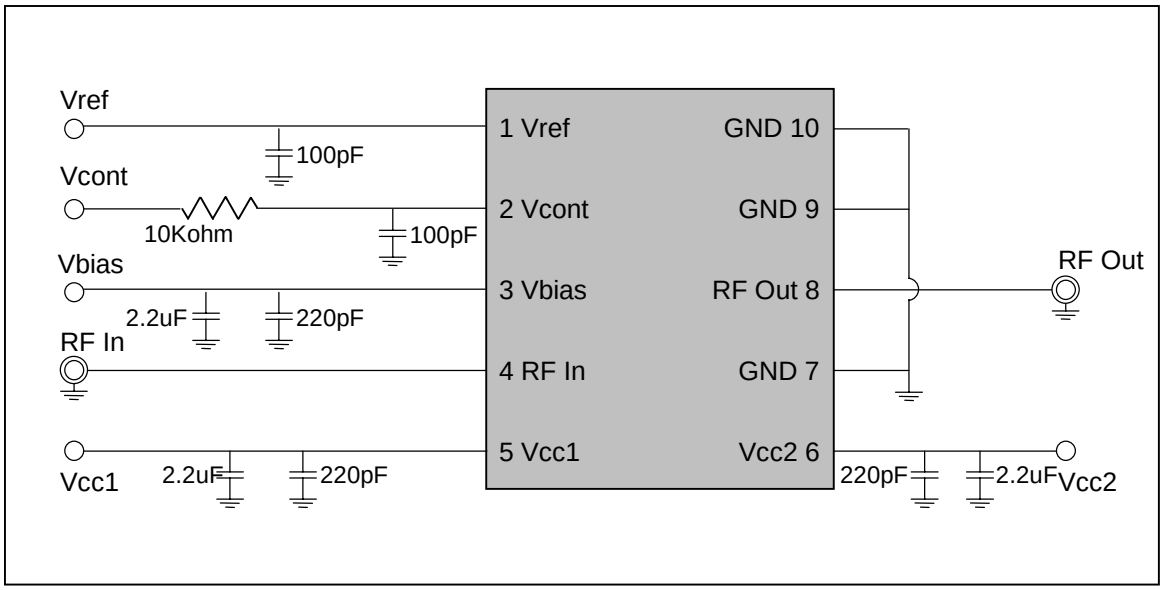


Figure 2. Evaluation Board Assembly Diagram

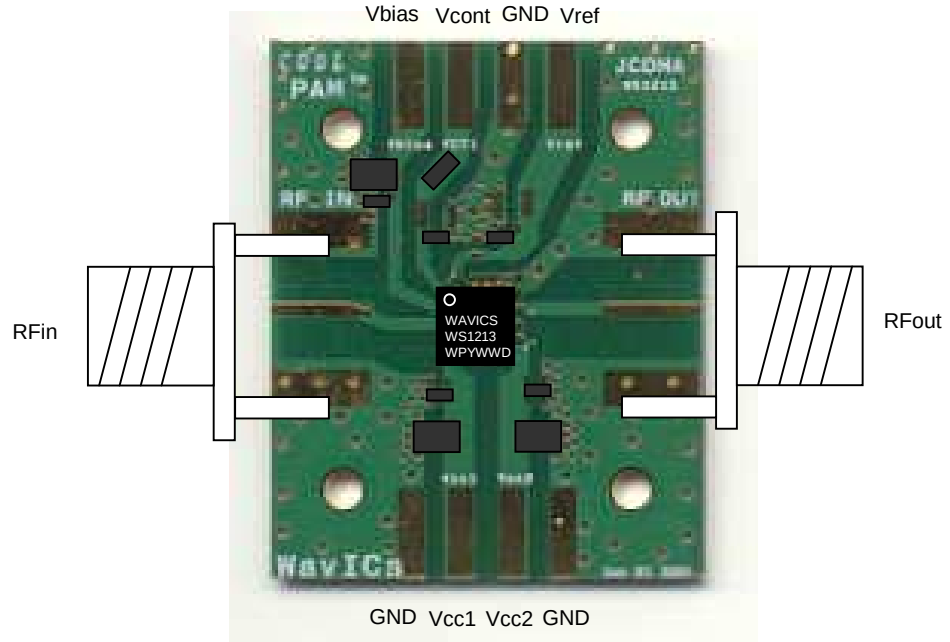
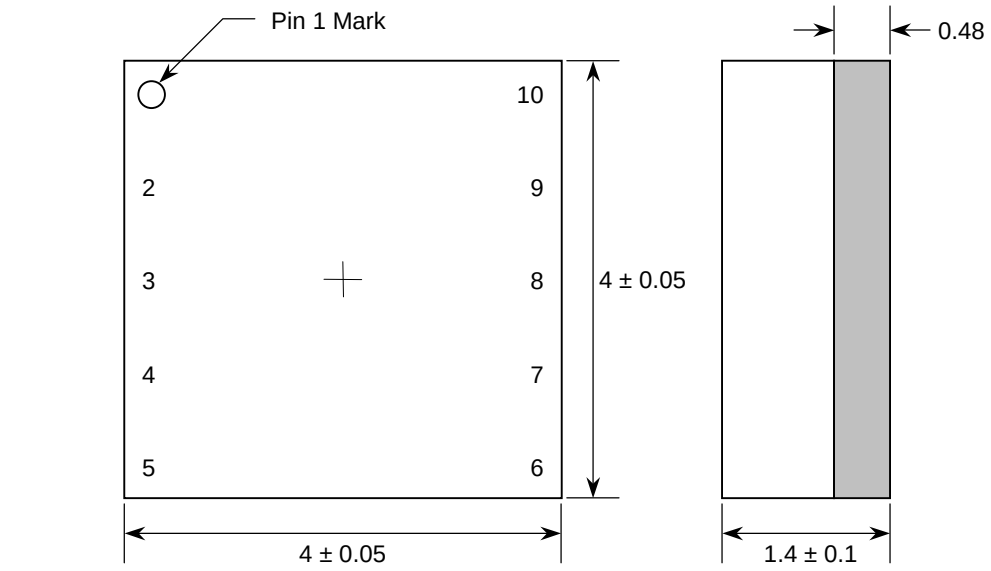
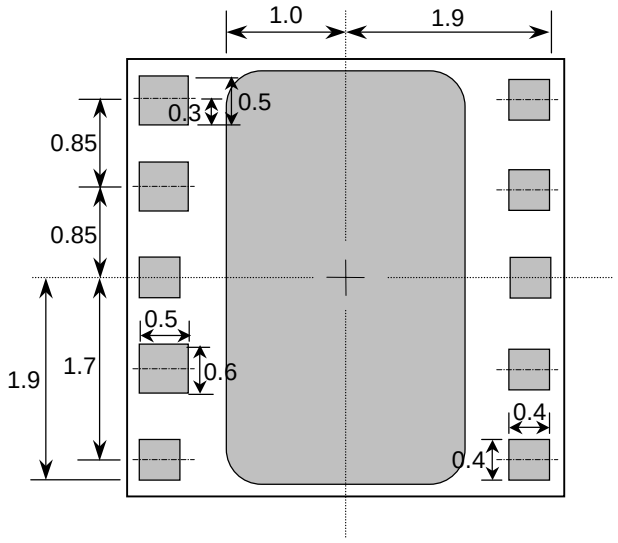


Figure 1. Package Dimensional Drawing and Pin Descriptions



X-RAY TOP VIEW SIDE VIEW



BOTTOM VIEW

Pin #	Name	Description
1	Vref	Reference Voltage
2	Vcont	Control Voltage
3	Vbias	Bias Supply
4	RF In	RF Input
5	Vcc1	Supply Voltage
6	Vcc2	Supply Voltage
7	GND	Ground
8	RF Out	RF Output
9	GND	Ground
10	GND	Ground

PIN DESCRIPTIONS

all dimensions are in millimeters

Figure 2. Marking Specification

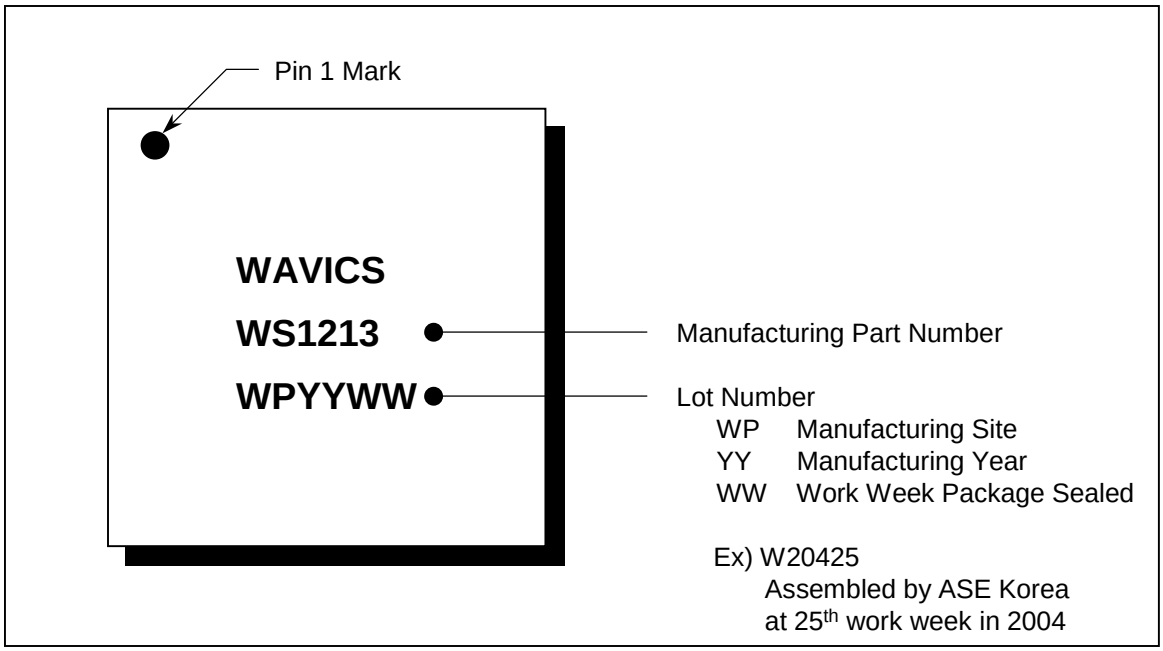
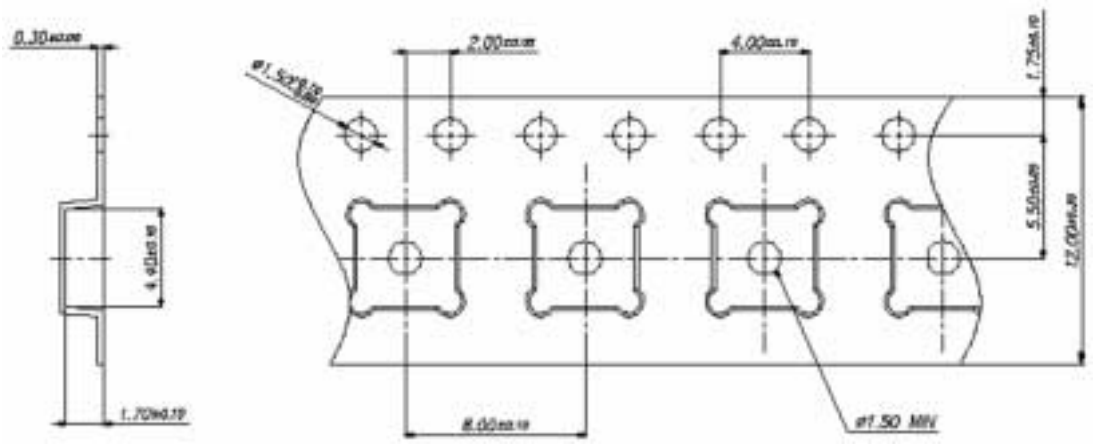


Figure 1. Tape and Reel Format – 4mm x 4mm

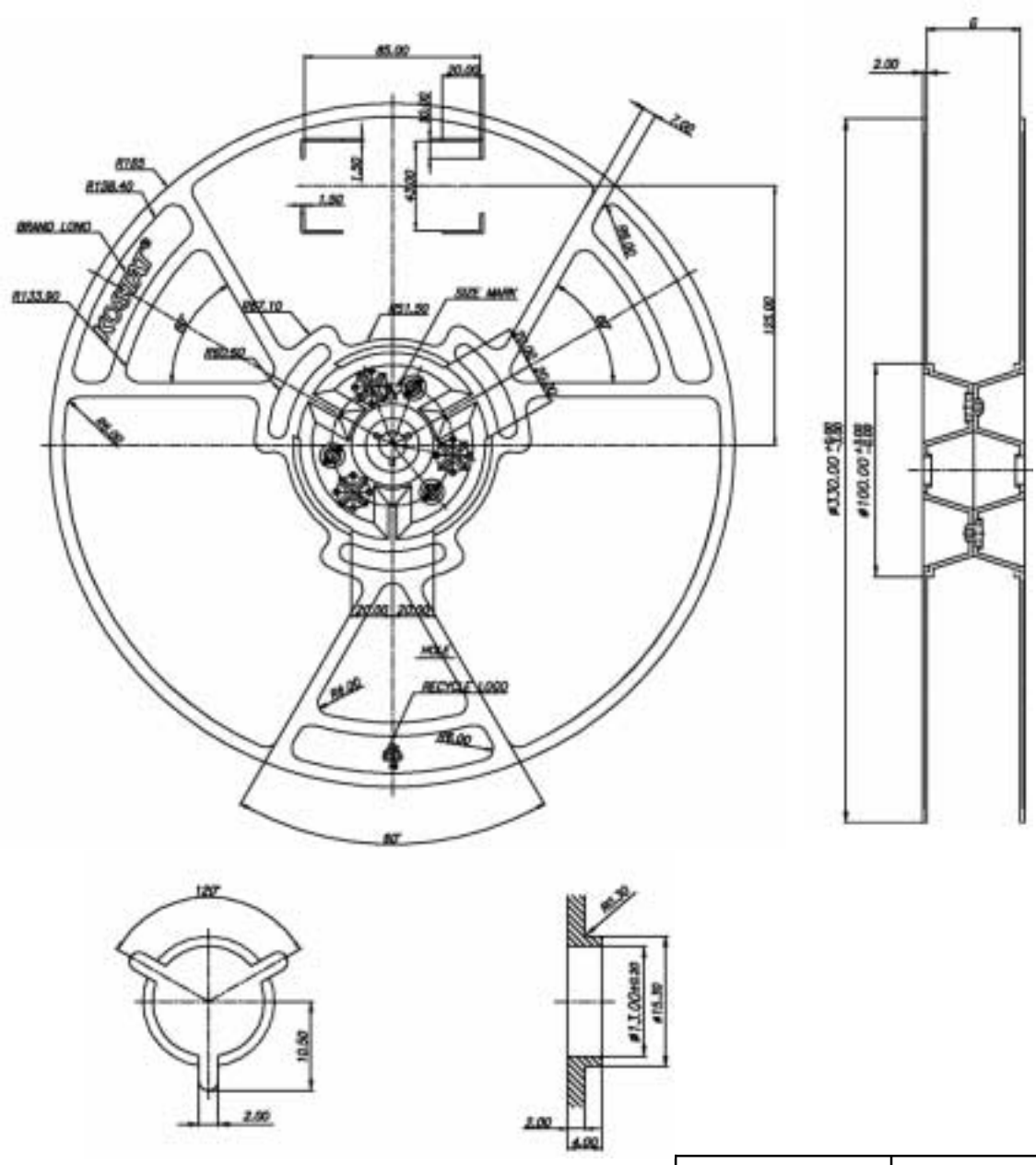


NOTES

1. Package Type : 4mm x 4mm
2. Tape Width : 12mm
3. Pocket Pitch : 8mm
4. Pocket Depth : 1.6mm
5. Reel Capacity : 2500ea
6. Max Reel Dia : 13”

all dimensions are in millimeters

Figure 2. Plastic Reel Format – 13”/4”



Detail of Pin Hole

Tape Width	12.00mm
Size Mark(XX)	12
G $^{+2.00}_{-0.00}$	12.4

all dimensions are in millimeters

1. ESD (Electrostatic Discharge)

Electrostatic discharge occurs naturally in the environment. With the increase in voltage potential, the outlet of neutralization or discharge will be sought. If the acquired discharge route is through a semiconductor device, destructive damage will result.

ESD countermeasure methods should be developed and used to control potential ESD damage during handling in a factory environment at each manufacturing site.

Table 1. ESD Classification

Pin #	Name	Description	HBM	CDM / MM	Classification
1	Vref	Reference Voltage	+/- 2000V	+/- 200V	**Class 2**
2	Vcont	Control Voltage			
3	Vbias	Bias Supply			
4	RF In	RF Input			
5	Vcc1	Supply Voltage			
6	Vcc2	Supply Voltage			
7	GND	Ground			
8	RF Out	RF Output			
9	GND	Ground			
10	GND	Ground			

NOTE : Module products should be considered extremely ESD sensitive

2. MSL (Moisture Sensitivity Level)

Plastic encapsulated surface mount package is sensitive to damage induced by absorbed moisture and temperature. WAVICS follows JEDEC Standard J-STD 020B. Each component and package type is classified for moisture sensitivity by soaking a known dry package at various temperatures and relative humidity, and times. After soak, the components are subjected to three consecutive simulated reflows.

The out of bag exposure time maximum limits are determined by the classification test describe above which corresponds to a MSL classification level 6 to 1 according to the JEDEC standard IPC/JEDEC J-STD-020B and J-STD-033.

WS1213 is MSL3. Thus, according to the J-STD-033 p.11 the maximum Manufacturers Exposure Time (MET) for this part is 168 hours. After this time period, the part would need to be removed from the reel, de-taped and then re-bake.

Table 2. Moisture Classification Level and Floor Life

MSL Level	Floor Life (out of bag) at factory ambient =< 30°C/60% RH or as stated
1	Unlimited at =< 30°C/85% RH
2	1 year
2a	4 weeks
3	**168 hours**
4	72 hours
5	48 hours
5a	24 hours
6	Mandatory bake before use. After bake, must be reflowed within the time limit specified on the label

NOTE: The MSL Level is marked on the MSL Label on each shipping bag.

MSL classification reflow temperature for the WS1213 is targeted at 250°C +0/-5°C. Figure 1 and Table 3 show typical SMT profile for maximum temperature of 250°C.

Figure 1. Typical SMT Reflow Profile for Maximum Temperature = 250 +0/-5ºC

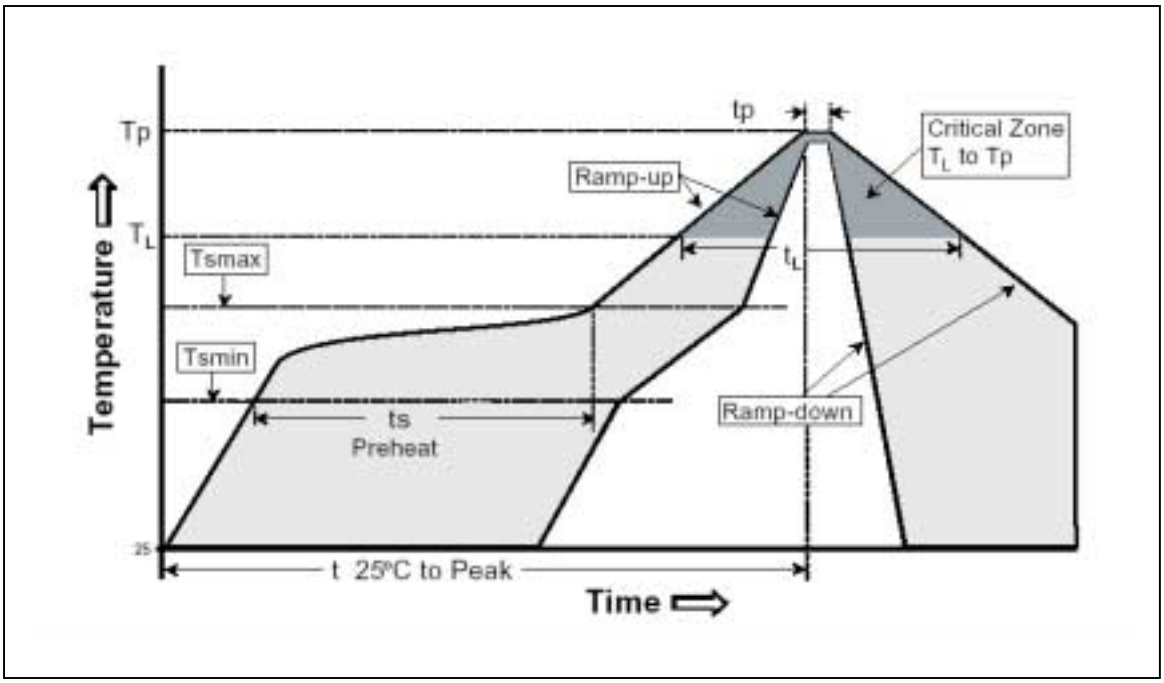


Table 3. Typical SMT Reflow Profile for Maximum Temperature = 250 +0/-5ºC

Profile Feature	Sn-Pb Solder	Pb-Free Solder
Average ramp-up rate (T_L to T_P)	3 ºC/sec max	3 ºC/sec max
Preheat - Temperature Min (Tsmin) - Temperature Max (Tsmax) - Time (min to max) (ts)	 100 ºC 150 ºC 60-120 sec	 100 ºC 150 ºC 60-180 sec
Tsmax to T_L - Ramp-up Rate		3 ºC/sec max
Time maintained above: - Temperature (T_L) - Time (T_L)	 183 ºC 60-150 sec	 217 ºC 60-150 sec
Peak temperature (Tp)	225 +0/-5 ºC	250 +0/-5 ºC
Time within 5 ºC of actual Peak Temperature (tp)	10-30 sec	10-30 sec
Ramp-down Rate	6 ºC/sec max	6 ºC/sec max
Time 25 ºC to Peak Temperature	6 min max.	8 min max.

3. Storage Conditions

Packages described in this document must be stored in sealed moisture barrier, anti-static bags. Shelf life in a sealed moisture barrier bag is 12 months at <40ºC and 90% relative humidity (RH) J-STD-033 p.7.

3-1. Out-of-Bag Time Duration

After unpacking the device must be soldered to the PCB within 168 hours as listed in the J-STD-020B p.11 with factory conditions <30ºC and 60% RH.

3-2. Baking

It is not necessary to re-bake the part if both conditions(storage conditions and out-of-bag condition) have been satisfied. Baking must be done if at least one of the conditions above have not been satisfied. The baking conditions are 125ºC for 24 hours J-STD-033 p.8.

CAUTION: Tape and reel materials typically cannot be baked at the temperature described above. If out-of-bag exposure time is exceeded, parts must be baked for a longer time at low temperatures, or the parts must be re-reeled, de-taped, re-baked and then put back on tape and reel. (See moisture sensitive warning label on each shipping bag for information of baking)

4. Board Rework

4-1. Component Removal, Rework and Remount

If a component is to be removed from the board, it is recommended that localized heating be used and the maximum body temperatures of any surface mount component on the board not exceed 200˚C. This method will minimize moisture related component damage. If any component temperature exceeds 200˚C, the board must be baked dry per 4-2 prior to rework and/or component removal. Component temperatures **shall** be measured at the top center of the package body. Any SMD packages that have not exceeded their floor life can be exposed to a maximum body temperature as high as their specified maximum reflow temperature.

4-1-1. Removal for Failure Analysis

Not following the requirements of 4-1 may cause moisture/reflow damage that could hinder or completely prevent the determination of the original failure mechanism.

4-1-2. Baking of Populated Boards

Some SMD packages and board materials are not able to withstand long duration bakes at 125˚C. Examples of this are some FR-4 materials, which cannot withstand a 24 hr bake at 125°C. Batteries and electrolytic capacitors are also Temperature sensitive. With component and board temperature restrictions in mind, choose a bake temperature from Table 4-1 in J-STD 033; then determine the appropriate bake duration based on the component to be removed. For additional considerations see IPC-7711 and IPC-7721.

4. Derating due to Factory Environmental Conditions

Factory floor life exposures for SMD packages removed from the dry bags will be a function of the ambient environmental conditions. A safe, yet conservative, handling approach is to expose the SMD packages only up to the maximum time limits for each moisture sensitivity level as shown in Table 2. This approach, however, does not work if the factory humidity or temperature are greater than the testing conditions of 30˚C/60% RH. A solution for addressing this problem is to derate the exposure times based on the knowledge of moisture diffusion in the component packaging materials (ref. JESD22-A120). Recommended equivalent total floor life exposures can be estimated for a range of humidity's and temperatures based on the nominal plastic thickness for each device. Table 4 lists equivalent derated floor lives for humidity's ranging from 20-90% RH for three temperatures, 20˚C, 25˚C, and 30˚C. This table is applicable to SMDs molded with novolac, biphenyl or multifunctional epoxy mold compounds. The following assumptions were used in calculating Table 4:

1. Activation Energy for diffusion = 0.35eV (smallest known value).
2. For ≤60% RH, use Diffusivity = 0.121exp (- 0.35eV/kT) mm2/s
   (this uses smallest known Diffusivity @ 30˚C).
3. For >60% RH, use Diffusivity = 1.320exp (- 0.35eV/kT) mm2/s
   (this uses largest known Diffusivity @ 30˚C).

Table 4. Recommended Equivalent Total Floor Life (days) @ 20°C, 25°C & 30°C
For ICs with Novolac, Biphenyl and Multifunctional Epoxies
(Reflow at same temperature at which the component was classified)

Maximum Percent Relative Humidity												
Package Type and Body Thickness	Moisture Sensitivity Level	5%	10%	20%	30%	40%	50%	60%	70%	80%	90%	
Body Thickness ≥3.1 mm including PQFPs >84 pins, PLCCs (square) All MQFPs or All BGAs ≥1 mm	Level 2a	∞ ∞ ∞	∞ ∞ ∞	∞ ∞ ∞	60 78 103	41 53 69	33 42 57	28 36 47	10 14 19	7 10 13	6 8 10	30°C 25°C 20°C
	Level 3	∞ ∞ ∞	∞ ∞ ∞	10 13 17	9 11 14	8 10 13	7 9 12	7 9 12	5 7 10	4 6 8	4 5 7	30°C 25°C 20°C
	Level 4	∞ ∞ ∞	5 6 8	4 5 7	4 5 7	4 5 7	3 5 7	3 4 6	3 3 5	2 3 4	2 3 4	30°C 25°C 20°C
	Level 5	∞ ∞ ∞	4 5 7	3 5 7	3 4 6	2 4 5	2 3 5	2 3 4	2 2 3	1 2 3	1 2 3	30°C 25°C 20°C
	Level 5a	∞ ∞ ∞	2 3 5	1 2 4	1 2 3	1 2 3	1 2 3	1 2 2	1 1 2	1 1 2	1 1 2	30°C 25°C 20°C
Body 2.1 mm ≤ Thickness <3.1 mm including PLCCs (rectangular) 18-32 pins SOICs (wide body) SOICs ≥20 pins, PQFPs ≤80 pins	Level 2a	∞ ∞ ∞	∞ ∞ ∞	∞ ∞ ∞	∞ ∞ ∞	86 148 ∞	39 51 69	28 37 49	4 6 8	3 4 5	2 3 4	30°C 25°C 20°C
	Level 3	∞ ∞ ∞	∞ ∞ ∞	19 25 32	12 15 19	9 12 15	8 10 13	7 9 12	3 5 7	2 3 5	2 3 4	30°C 25°C 20°C
	Level 4	∞ ∞ ∞	7 9 11	5 7 9	4 5 7	4 5 6	3 4 6	3 4 5	2 3 4	2 2 3	1 2 3	30°C 25°C 20°C
	Level 5	∞ ∞ ∞	4 5 6	3 4 5	3 3 5	2 3 4	2 3 4	2 3 4	1 2 3	1 1 3	1 1 2	30°C 25°C 20°C
	Level 5a	∞ ∞ ∞	2 2 3	1 2 2	1 2 2	1 2 2	1 2 2	1 2 2	1 1 2	0.5 1 2	0.5 1 1	30°C 25°C 20°C
Body Thickness <2.1 mm including SOICs <18 pins All TQFPs, TSOPs or all BGAs <1 mm body thickness	Level 2a	∞ ∞ ∞	∞ ∞ ∞	∞ ∞ ∞	∞ ∞ ∞	∞ ∞ ∞	∞ ∞ ∞	28 ∞ ∞	1 2 2	1 1 2	1 1 1	30°C 25°C 20°C
	Level 3	∞ ∞ ∞	∞ ∞ ∞	∞ ∞ ∞	∞ ∞ ∞	∞ ∞ ∞	11 14 20	7 10 13	1 2 2	1 1 2	1 1 1	30°C 25°C 20°C
	Level 4	∞ ∞ ∞	∞ ∞ ∞	∞ ∞ ∞	9 12 17	5 7 9	4 5 7	3 4 6	1 2 2	1 1 2	1 1 1	30°C 25°C 20°C
	Level 5	∞ ∞ ∞	∞ ∞ ∞	13 18 26	5 6 8	3 4 6	2 3 5	2 3 4	1 2 2	1 1 2	1 1 1	30°C 25°C 20°C
	Level 5a	∞ ∞ ∞	10 13 18	3 5 6	2 3 4	1 2 3	1 2 2	1 2 2	1 1 2	1 1 2	0.5 1 1	30°C 25°C 20°C

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