



PRELIMINARY

AP9A110/AP9A110L

5V, 128K x 8 High-Speed, Low-Power, CMOS Static RAM with Optional 2V Data Retention

Features

- Fast access times: 12 and 15 ns
- Drives a 50 pF load vs. 30 pF industry-standard load
- Multiple center power and ground pins for improved noise immunity
- 2V/250 μ A data retention ("L" version)
- Low active power: 467 mW (Max.) at 15 ns
- Low standby current: 11 mW (Max.)
- Fully static operation, no clock or refresh required
- TTL and CMOS-compatible inputs and outputs
- Single 5V \pm 10% power supply
- Packaged in industry-standard 300-mil and 400-mil 32-Pin SOJ
- Commercial and industrial temperature ranges

Aptos' high-performance, 0.35 μ m, CMOS process technology. This highly reliable process coupled with innovative circuit design techniques, yields high performance at low power consumption.

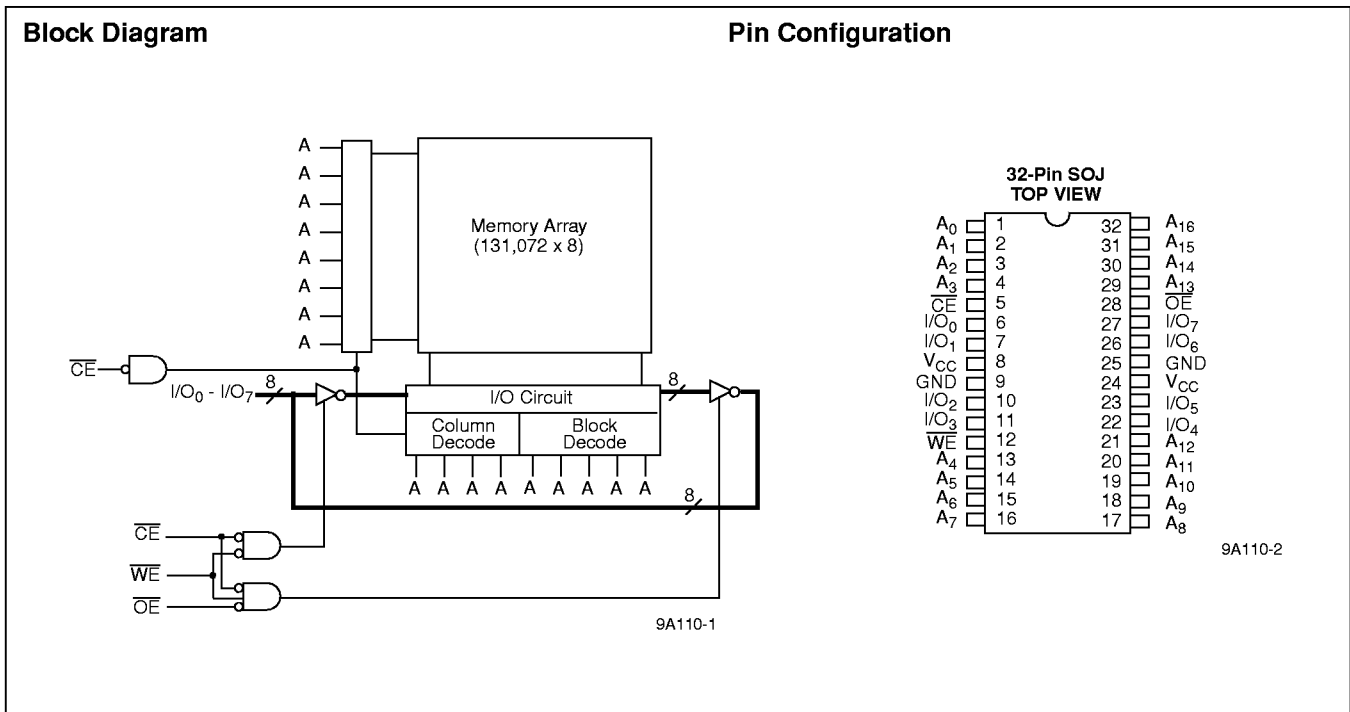
When Chip Enable (\overline{CE}) is HIGH the device assumes a standby mode at which the power dissipation can be reduced down to 11 mW (Max.) at CMOS input levels. At 2V V_{CC} , power is reduced to 0.5 mW (Max.) ("L" version).

Easy memory expansion is provided by using asserted LOW \overline{CE} and asserted LOW Output Enable inputs (\overline{OE}). The asserted LOW Write Enable (\overline{WE}) controls both writing and reading of the memory.

The AP9A110/AP9A110L is pin-compatible with other 5V, 128K x 8 center power and ground SRAMs in the SOJ package.

Functional Description

The Aptos AP9A110/AP9A110L is a high-speed, low-power, 128K x 8 CMOS static RAM. It is fabricated using



Selection Guide

	AP9A110/L-12	AP9A110/L-15
Maximum Access Time (ns)	12	15
Maximum Operating Current (mA)	90	85
Maximum Standby Current (mA)	2	2

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature..... -65 °C to +150 °C

Ambient Temperature

with Power Applied..... -55 °C to +125 °C

V_{CC} Supply Relative to GND..... -1.0 V to +7.0 V

Voltage on Any Pin Relative to GND..... -0.5 V to $V_{CC}+0.5$ V

Short Circuit Output Current ¹..... ±50 mA

Power Dissipation..... 1.0 W

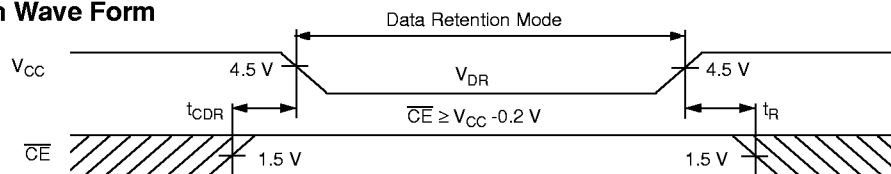
Electrical Characteristics Over the Operating Range (0°C ≤ T_A ≤ 70°C, V_{CC} = 5 V ±10% Max.) -Commercial

Symbol	Parameter	Test Conditions	9A110/L-12		9A110/L-15		Unit
			Min.	Max.	Min.	Max.	
I _{CC1}	Dynamic Operating Current ²	$V_{CC} = \text{Max.}, I_{OUT} = 0 \text{ mA}, \overline{CE} = V_{IL}, f = f_{\text{max.}}$		90		85	mA
I _{CC2}	Operating Current ²	$V_{CC} = \text{Max.}, I_{OUT} = 0 \text{ mA}, \overline{CE} = V_{IL}, f = 0$		60		60	mA
I _{SB1}	TTL Standby Current -TTL Inputs	$V_{CC} = \text{Max.}, V_{IN} = V_{IH} \text{ or } V_{IL}, \overline{CE} \geq V_{IH}, f = f_{\text{max.}}$		15		15	mA
I _{SB2}	CMOS Standby Current -CMOS Inputs	$V_{CC} = \text{Max.}, \overline{CE} \geq V_{CC} - 0.2 \text{ V}, V_{IN} \geq V_{CC} - 0.2 \text{ V} \text{ or } V_{IN} \leq 0.2 \text{ V}, f = 0$		2		2	mA
I _{LI}	Input Leakage Current	$GND \leq V_{IN} \leq V_{CC}$	-1	1	-1	1	μA
I _{LO}	Output Leakage Current	$GND \leq V_{OUT} \leq V_{CC},$ Output Disabled	-1	1	-1	1	μA
V _{OH}	Output High Voltage	$V_{CC} = \text{Min.}, I_{OH} = -4.0 \text{ mA}$	2.4		2.4		V
V _{OL}	Output Low Voltage	$V_{CC} = \text{Min.}, I_{OL} = 8.0 \text{ mA}$		0.4		0.4	V
V _{IH}	Input High Voltage ³		2.2	$V_{CC} + 0.5$	2.2	$V_{CC} + 0.5$	V
V _{IL}	Input Low Voltage ³		-0.5	0.8	-0.5	0.8	V

Data Retention Characteristics ("L Version) -Commercial

Symbol	Description	Test Conditions ⁴	Min.	Max.	Unit
V _{DR}	V _{CC} for Data Retention	$V_{CC} = V_{DR} = 2.0 \text{ V},$ $\overline{CE} \geq V_{CC} - 0.2 \text{ V}, V_{IN} \geq V_{CC} - 0.2 \text{ V}$ or $V_{IN} \leq 0.2 \text{ V}$	2.0		V
I _{CCDR}	Data Retention Current			250	μA
t _{CDR}	Chip Deselect to Data Retention Time		0		ns
t _R	Operation Recovery Time		t _{RC}		ns

Data Retention Wave Form



Capacitance ⁵

Symbol	Description	Max.	Unit
C _{IN}	Input Capacitance	5	pF
C _{IO}	I/O Capacitance	5	pF

Notes:

1. No more than one output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
2. I_{CC} is dependent upon output loading and cycle rates. Specified values are with outputs open.

3. V_{IL} undershoot = -1.0V where t=t_{RC}/4 per cycle. V_{IH} overshoot = V_{CC} +1.0V where t=t_{RC}/4 per cycle.

4. No input may exceed V_{CC} +0.5V (DC).

5. Tested initially and after any design or process changes that may effect these parameters.

Electrical Characteristics Over the Operating Range ($0^{\circ}\text{C} \leq T_A \leq 70^{\circ}\text{C}$, $V_{CC} = 5\text{ V} \pm 10\% \text{ Max.}$) -Industrial

Symbol	Parameter	Test Conditions	9A110/L-12		9A110/L-15		Unit
			Min.	Max.	Min.	Max.	
I_{CC1}	Dynamic Operating Current ²	$V_{CC} = \text{Max.}, I_{OUT} = 0\text{ mA}, \overline{CE} = V_{IL}, f = f_{\text{max.}}$		105		95	mA
I_{CC2}	Operating Current ²	$V_{CC} = \text{Max.}, I_{OUT} = 0\text{ mA}, \overline{CE} = V_{IL}, f = 0$		70		70	mA
I_{SB1}	TTL Standby Current -TTL Inputs	$V_{CC} = \text{Max.}, V_{IN} = V_{IH} \text{ or } V_{IL}, \overline{CE} \geq V_{IH}, f = f_{\text{max.}}$		25		25	mA
I_{SB2}	CMOS Standby Current -CMOS Inputs	$V_{CC} = \text{Max.}, \overline{CE} \geq V_{CC} - 0.2\text{ V}, V_{IN} \geq V_{CC} - 0.2\text{ V} \text{ or } V_{IN} \leq 0.2\text{ V}, f = 0$		5		5	mA
I_{LI}	Input Leakage Current	$\text{GND} \leq V_{IN} \leq V_{CC}$	-5	5	-5	5	μA
I_{LO}	Output Leakage Current	$\text{GND} \leq V_{OUT} \leq V_{CC}, \text{ Output Disabled}$	-5	5	-5	5	μA
V_{OH}	Output High Voltage	$V_{CC} = \text{Min.}, I_{OH} = -4.0\text{ mA}$	2.4		2.4		V
V_{OL}	Output Low Voltage	$V_{CC} = \text{Min.}, I_{OL} = 8.0\text{ mA}$		0.4		0.4	V
V_{IH}	Input High Voltage ³		2.2	$V_{CC} + 0.5$	2.2	$V_{CC} + 0.5$	V
V_{IL}	Input Low Voltage ³		-0.5	0.8	-0.5	0.8	V

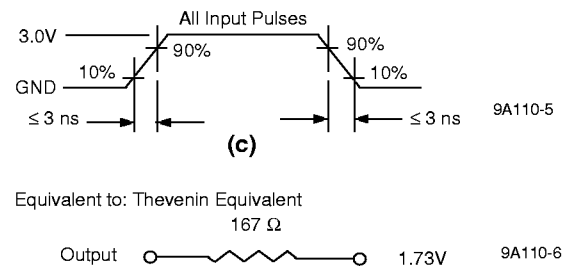
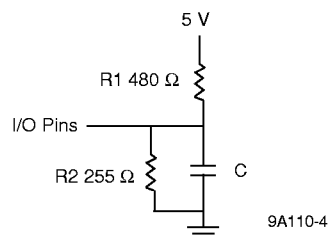
Data Retention Characteristics ("L" Version) -Industrial

Symbol	Description	Test Conditions ⁴	Min.	Max.	Unit
V_{DR}	V_{CC} for Data Retention	$V_{CC} = V_{DR} = 2.0\text{ V}, \overline{CE} \geq V_{CC} - 0.2\text{ V}, V_{IN} \geq V_{CC} - 0.2\text{ V} \text{ or } V_{IN} \leq 0.2\text{ V}$	2.0		V
I_{CCDR}	Data Retention Current			5	mA
t_{CDR}	Chip Deselect to Data Retention Time		0		ns
t_R	Operation Recovery Time		t_{RC}		ns

AC Test Loads and Waveforms

(a) $C_1 = 50\text{ pF}$
INCLUDING JIG
AND SCOPE

(b) $C_2 = 5\text{ pF}$
INCLUDING JIG
AND SCOPE



Switching Characteristics Over the Operating Range ^{6,7}

Parameter	Description	9A110/L-12		9A110/L-15		Unit
		Min.	Max.	Min.	Max.	
<i>Read Cycle</i> ⁸						
t_{RC}	Read Cycle Time	12		15		ns
t_{AA}	Address Access Time		12		15	ns
t_{OHA}	Output Hold Time	3		3		ns
t_{ACE}	\overline{CE} Access Time		12		15	ns
t_{DOE}	\overline{OE} Access Time		5		7	ns
t_{LZOE} ⁹	\overline{OE} to Low-Z Output	0		0		ns
t_{HZOE} ⁹	\overline{OE} to High-Z Output		5		6	ns
t_{LZCE} ⁹	\overline{CE} to Low-Z Output	3		3		ns
t_{HZCE} ⁹	\overline{CE} to High-Z Output		6		8	ns
t_{PU}	\overline{CE} to Power Up	0		0		ns
t_{PD}	\overline{CE} to Power Down		12		15	ns
<i>Write Cycle</i> ¹⁰						
t_{WC}	Write Cycle Time	12		15		ns
t_{SCE}	\overline{CE} to Write End	8		10		ns
t_{AW}	Address Set-up Time to Write End	8		10		ns
t_{HA}	Address Hold to Write End	0		0		ns
t_{SA}	Address Set-up Time to Write Start	0		0		ns
t_{PWE1} ¹¹	\overline{WE} Pulse Width ($\overline{OE} = \text{HIGH}$)	8		10		ns
t_{PWE2}	\overline{WE} Pulse Width ($\overline{OE} = \text{LOW}$)	12		12		ns
t_{SD}	Data Set-up to Write End	6		7		ns
t_{HD}	Data Hold from Write End	0		0		ns
t_{HZWE} ⁹	\overline{WE} LOW to High-Z Output		6		7	ns
t_{LZWE} ⁹	\overline{WE} HIGH to Low-Z Output	2		2		ns

Notes:

6. Test conditions assume signal transition times of 3 ns or less, timing reference levels of 1.5 V, input pulse levels of 0 V to 3.0 V and output loading specified in AC Test Loads and Waveforms *Figure (a)* unless otherwise noted.

7. I/O will assume the High-Z state if $\overline{OE} \geq V_{IH}$.

8. \overline{WE} is HIGH for a Read Cycle.

9. Tested with the load in AC Test Loads and Waveforms *Figure (b)*. Transition is measured $\pm 500\text{mV}$ from steady state voltage.

10. The internal write time is defined by the overlap of \overline{CE} LOW and \overline{WE} LOW. All signals must be in valid states to initiate a Write,

but any can be deasserted to terminate the Write. The Data Input Set-up and Hold timing is referenced to the rising or falling edge of the signal that terminates the write.

11. Tested with \overline{OE} HIGH for a minimum of 4 ns before $\overline{WE} = \text{LOW}$ to place I/O in High-Z state.

12. The device is continuously selected. $\overline{OE}, \overline{CE} = V_{IL}$.

13. Address is valid prior to, or coincident with, \overline{CE} LOW transitions.

14. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} and t_{HZOE} is less than t_{LZOE} .

Pin Descriptions

A₀ - A₁₆: Address Inputs

These 17 address inputs select one of the 131,072 8-bit words in the RAM.

\overline{CE} : Chip Enable Input

\overline{CE} is asserted LOW. The Chip Enable is asserted LOW to read from or write to the device. If Chip Enable is deasserted, the device is deselected and is in a standby power mode. The I/O pins will be in the High-Z state when the device is deselected.

\overline{OE} : Output Enable Input

The Output Enable input is asserted LOW. If the Output Enable is asserted LOW while \overline{CE} is asserted (LOW) and

\overline{WE} is deasserted (HIGH), data from the SRAM will be present on the I/O pins. The I/O pins will be in the High-Z state when \overline{OE} is deasserted.

\overline{WE} : Write Enable Input

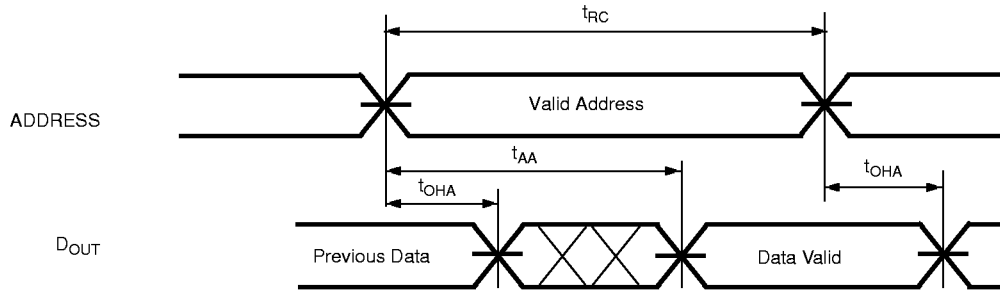
The Write Enable input is asserted LOW and controls read and write operations. When \overline{CE} and \overline{WE} are both asserted (LOW) input data present on the I/O pins will be written into the selected memory location.

I/O₀ - I/O₇: Common Input/Output Pins

GND: Ground

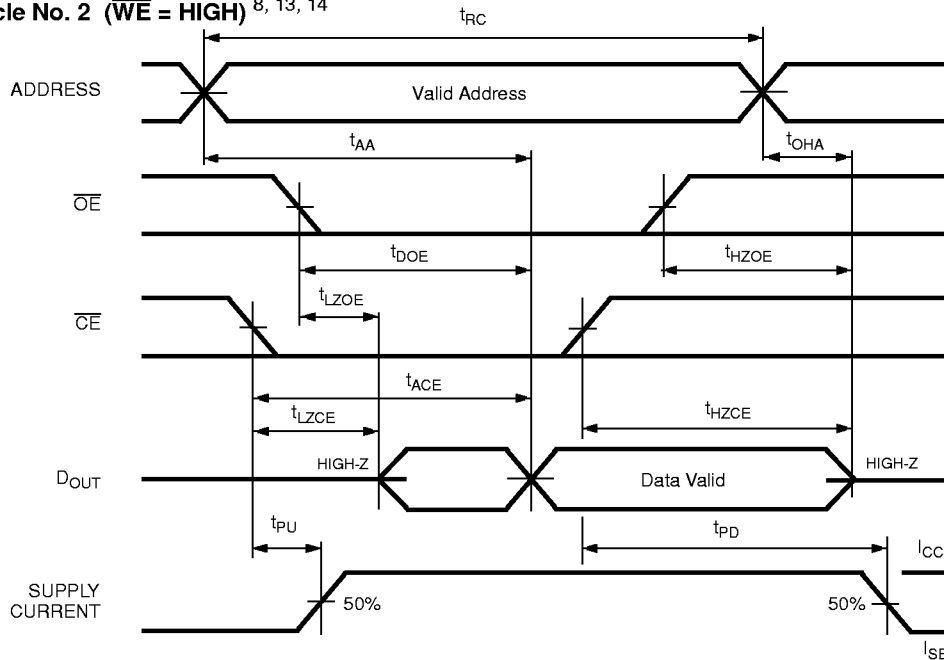
Switching Waveforms

Read Cycle No. 1 ($\overline{CE} = \text{LOW}$, $\overline{OE} = \text{LOW}$, $\overline{WE} = \text{HIGH}$)^{8, 12}



9A110-7

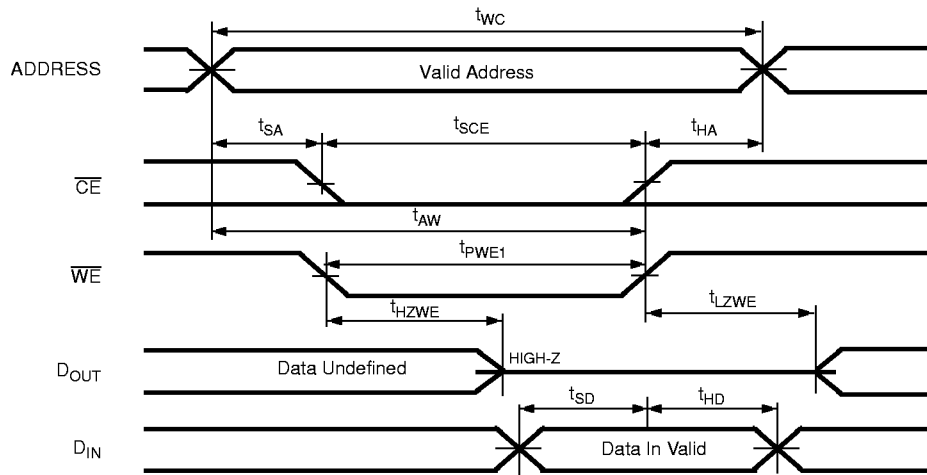
Read Cycle No. 2 ($\overline{WE} = \text{HIGH}$)^{8, 13, 14}



9A110-8

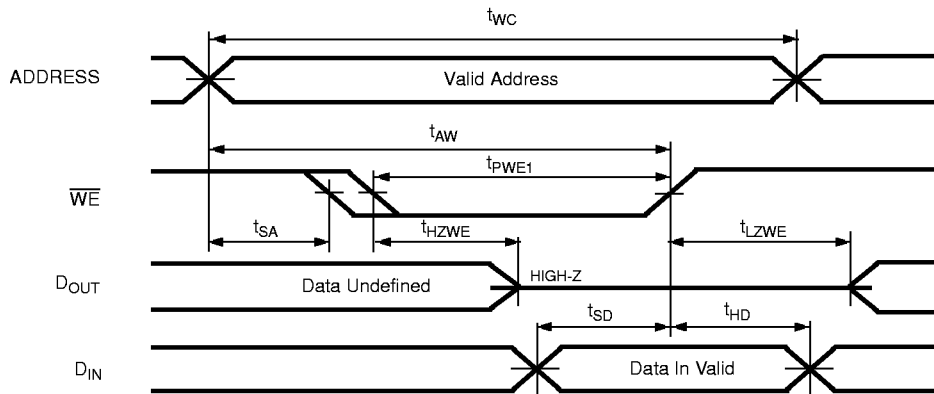
Switching Waveforms (continued)

Write Cycle No.1 (\overline{CE} controlled, \overline{OE} is HIGH or LOW: \overline{CE} Terminates Write) ¹⁰



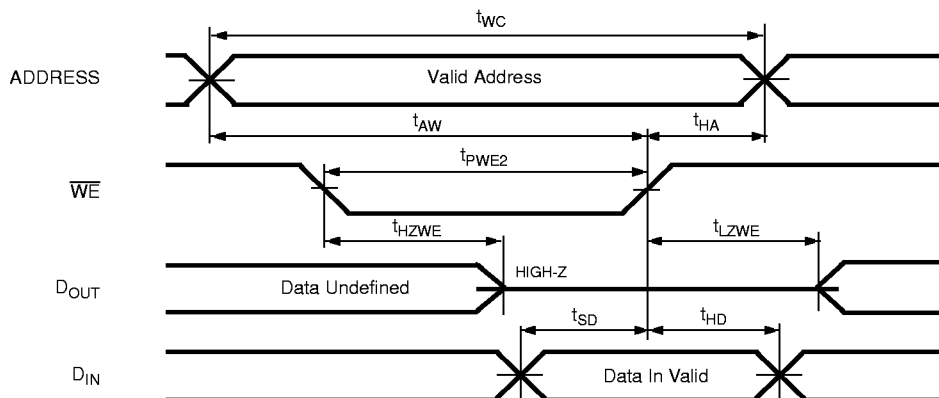
9A110-9

Write Cycle No.2 (\overline{WE} controlled, \overline{OE} is HIGH, \overline{CE} is LOW: \overline{WE} Terminates Write) ¹⁰



9A110-10

Write Cycle No.3 (\overline{WE} controlled, \overline{OE} is LOW, \overline{CE} is LOW: \overline{WE} Terminates Write) ¹⁰



9A110-11



PRELIMINARY

AP9A110/AP9A110L

Truth Table

Mode	\overline{WE}	\overline{CE}	\overline{OE}	I/O	I _{CC}
Standby	X	H	X	High-Z	I _{SB1} , I _{SB2}
Selected/Output Disabled	H	L	H	High-Z	I _{CC1} , I _{CC2}
Read	H	L	L	D _{OUT}	I _{CC1} , I _{CC2}
Write	L	L	X	D _{IN}	I _{CC1} , I _{CC2}

Ordering Information*Standard - AP9A110*

Speed	Part Number	Package Name	Package Type	Temperature Range
12	AP9A110-12VC	V32.1	32-Pin (400-Mil) Small Outline J-Bend	Commercial
	AP9A110-12V3C	V32.2	32-Pin (300-Mil) Small Outline J-Bend	
	AP9A110-12VI	V32.1	32-Pin (400-Mil) Small Outline J-Bend	Industrial
	AP9A110-12V3I	V32.2	32-Pin (300-Mil) Small Outline J-Bend	
15	AP9A110-15VC	V32.1	32-Pin (400-Mil) Small Outline J-Bend	Commercial
	AP9A110-15V3C	V32.2	32-Pin (300-Mil) Small Outline J-Bend	
	AP9A110-15VI	V32.1	32-Pin (400-Mil) Small Outline J-Bend	Industrial
	AP9A110-15V3I	V32.2	32-Pin (300-Mil) Small Outline J-Bend	

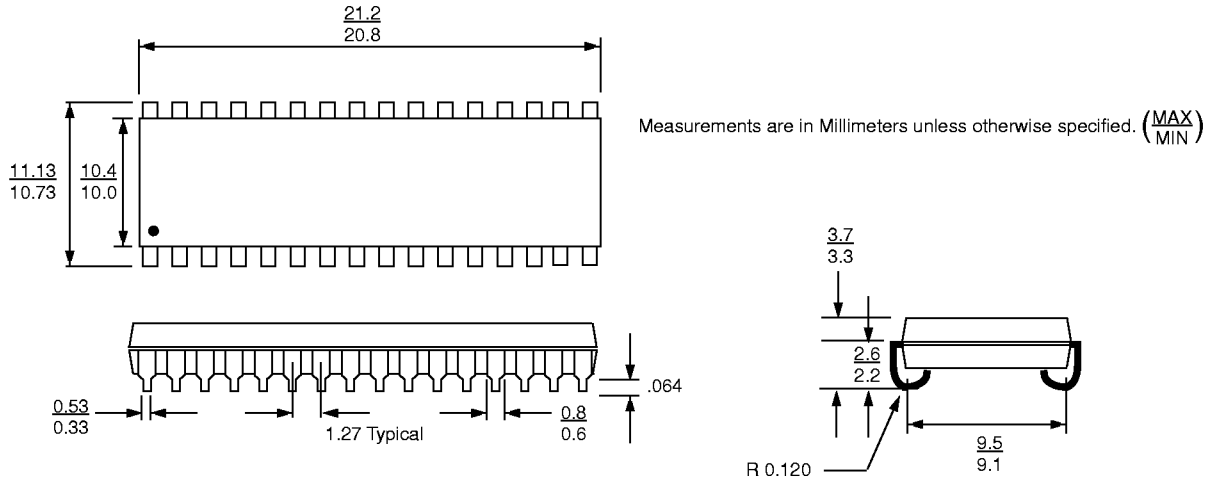
With Optional 2V Data Retention - AP9A110L

Speed	Part Number	Package Name	Package Type	Temperature Range
12	AP9A110L-12VC	V32.1	32-Pin (400-Mil) Small Outline J-Bend	Commercial
	AP9A110L-12V3C	V32.2	32-Pin (300-Mil) Small Outline J-Bend	
	AP9A110L-12VI	V32.1	32-Pin (400-Mil) Small Outline J-Bend	Industrial
	AP9A110L-12V3I	V32.2	32-Pin (300-Mil) Small Outline J-Bend	
15	AP9A110L-15VC	V32.1	32-Pin (400-Mil) Small Outline J-Bend	Commercial
	AP9A110L-15V3C	V32.2	32-Pin (300-Mil) Small Outline J-Bend	
	AP9A110L-15VI	V32.1	32-Pin (400-Mil) Small Outline J-Bend	Industrial
	AP9A110L-15V3I	V32.2	32-Pin (300-Mil) Small Outline J-Bend	

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Package Diagrams

V32.1 - 32-Pin (400-Mil) Small Outline J-Bend (SOJ)



V32.2 - 32-Pin (300-Mil) Small Outline J-Bend (SOJ)

