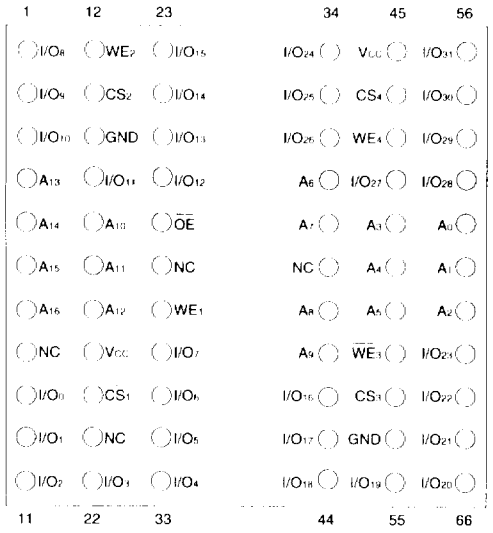
128Kx32 SRAM MODULE

FEATURES

- Access Times of 25 to 45nS
- MIL-STD-883 Compliant Devices Available
- Rad Tolerant Devices Available
- Packaging
  - 66-pin, PGA Type, 1.185 inch square Hermetic Ceramic HIP (Package 401), SMD Number 5962-93187
  - 68 lead, 40mm, Hermetic CQFP (Package 501), SMD Number 5962-95595
  - 68 lead, 40mm Low Profile CQFP, 3.5mm (0.140") (Package 502)
  - 68 lead, Hermetic CQFP (G2), 22mm (0.880 inch) square (Package 500). Designed to fit JEDEC 68 lead 0.990" CQFJ footprint (Fig. 3)
- Organized as 128Kx32; User Configurable as 256Kx16 or 512Kx8
- Commercial, Industrial and Military Temperature Ranges
- 5 Volt Power Supply
- Low Power CMOS
- TTL Compatible Inputs and Outputs
- Built in Decoupling Caps and Multiple Ground Pins for Low Noise Operation
- Weight
  WS128K32-XHX - 13 grams typical
  WS128K32-XG4X - 20 grams typical
- Each of these devices is upgradeable to 512Kx32

FIG. 1 PIN CONFIGURATION FOR WS128K32N-XHX, SMD 5962-93187

TOP VIEW



PIN DESCRIPTION

I/O_{0-31}	Data Inputs/Outputs
A_{0-16}	Address Inputs
$\overline{WE}_{1-4}$	Write Enables
$\overline{CS}_{1-4}$	Chip Selects
$\overline{OE}$	Output Enable
V_{CC}	Power Supply
GND	Ground
NC	Not Connected

BLOCK DIAGRAM

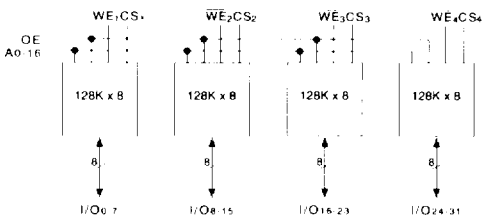
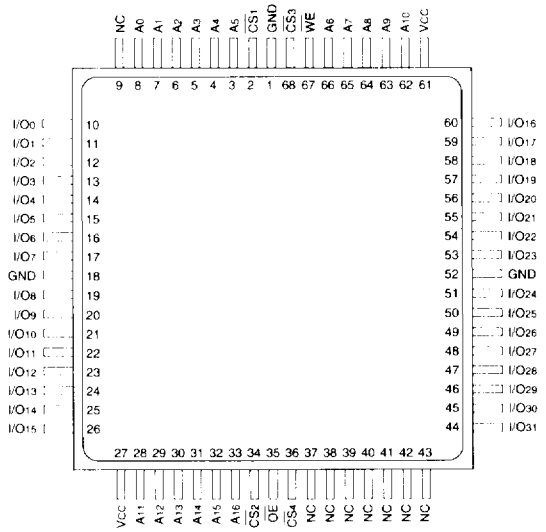


FIG. 2 PIN CONFIGURATION FOR WS128K32-XG4X, SMD 5962-95595

TOP VIEW



PIN DESCRIPTION

I/O0-31	Data Inputs/Outputs
A0-16	Address Inputs
$\overline{WE}$	Write Enable
$\overline{CS}$1-4	Chip Selects
$\overline{OE}$	Output Enable
Vcc	Power Supply
GND	Ground
NC	Not Connected

BLOCK DIAGRAM

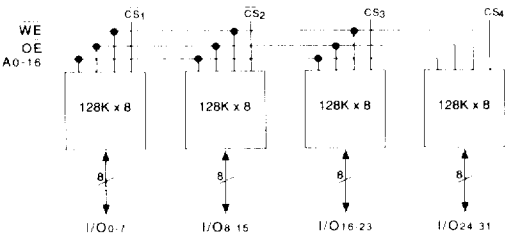
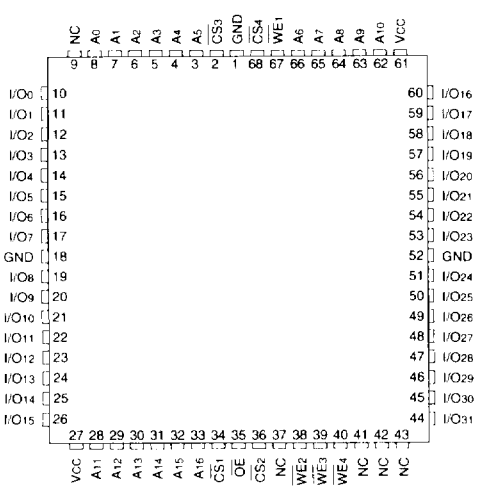
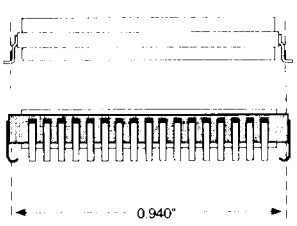


FIG. 3 PIN CONFIGURATION FOR WS128K32-XG2X

TOP VIEW



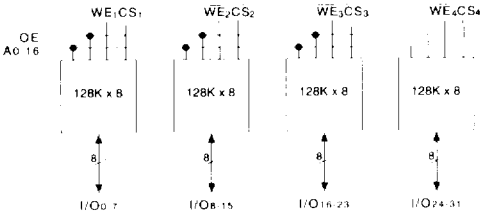


The White 68 lead G2 CQFP fills the same fit and function as the JEDEC 68 lead CQFJ or 68 PLCC. But the G2 has the TCE and lead inspection advantage of the CQFP form.

PIN DESCRIPTION

I/O0-31	Data Inputs/Outputs
A0-16	Address Inputs
$\overline{WE}$1-4	Write Enables
$\overline{CS}$1-4	Chip Selects
$\overline{OE}$	Output Enable
Vcc	Power Supply
GND	Ground
NC	Not Connected

BLOCK DIAGRAM



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ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Unit
Operating Temperature	T_A	-55	+125	°C
Storage Temperature	T_{STG}	-65	+150	°C
Signal Voltage Relative to GND	V_G	-0.5	Vcc+0.5	V
Junction Temperature	T_J		150	C
Supply Voltage	V_{CC}	-0.5	7.0	V

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V_{CC}	4.5	5.5	V
Input High Voltage	V_{IH}	2.2	V_{CC} + 0.3	V
Input Low Voltage	V_{IL}	-0.5	+0.8	V

TRUTH TABLE

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Mode	Data I/O	Power
H	X	X	Standby	High Z	Standby
L	L	H	Read	Data Out	Active
L	H	H	Out Disable	High Z	Active
L	X	L	Write	Data In	Active

CAPACITANCE

(T_A = +25°C)

Parameter	Symbol	Conditions	Max	Unit
$\overline{OE}$ capacitance	C_{OE}	V_{IN} = 0 V, f = 1.0 MHz	50	pF
$\overline{WE}_{1-4}$ capacitance	C_{WE}	V_{IN} = 0 V, f = 1.0 MHz		pF
HIP (PGA)			20	
CQFP G4			50	
CQFP G2			20	
$\overline{CS}_{1-4}$ capacitance	C_{CS}	V_{IN} = 0 V, f = 1.0 MHz	20	pF
Data I/O capacitance	C_{IO}	$V_{I/O}$ = 0 V, f = 1.0 MHz	20	pF
Address input capacitance	C_{AD}	V_{IN} = 0 V, f = 1.0 MHz	50	pF

This parameter is guaranteed by design but not tested.

DC CHARACTERISTICS

(V_{CC} = 5.0V, V_{SS} = 0V, T_A = -55°C to +125°C)

Parameter	Sym	Conditions	-25		-35		-45		Units
			Min	Max	Min	Max	Min	Max	
Input Leakage Current	I_{LI}	V_{CC} = 5.5, V_{IN} = GND to V_{CC}		10		10		10	µA
Output Leakage Current	I_{LO}	$\overline{CS}$ = V_{IH}, $\overline{OE}$ = V_{IH}, V_{OUT} = GND to V_{CC}		10		10		10	µA
Operating Supply Current x 32 Mode	I_{CC} x 32	$\overline{CS}$ = V_{IL}, $\overline{OE}$ = V_{IH}, f = 5MHz, V_{CC} = 5.5		500		500		420	mA
Standby Current	I_{SB}	$\overline{CS}$ = V_{IH}, $\overline{OE}$ = V_{IH}, f = 5MHz, V_{CC} = 5.5		60		60		60	mA
Output Low Voltage	V_{OL}	I_{OL} = 8mA, V_{CC} = 4.5		0.4		0.4		0.4	V
Output High Voltage	V_{OH}	I_{OH} = -4.0mA, V_{CC} = 4.5	2.4		2.4		2.4		V

NOTE: DC test conditions: V_{IH} = V_{CC} -0.3V, V_{IL} = 0.3V

DATA RETENTION CHARACTERISTICS

(T_A = -55°C to +125°C)

Parameter	Symbol	Conditions	-25			-35			-45			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Data Retention Supply Voltage	V_{DR}	$\overline{CS}$ > V_{CC} -0.2V	2.0		5.5	2.0		5.5	2.0		5.5	V
Data Retention Current	I_{CCDR1}	V_{CC} = 3V		0.5	8.0		0.5	8.0		0.5	8.0	mA
	I_{CCDR2}	V_{CC} = 2V		0.25	4.0		0.25	4.0		0.25	4.0	mA

AC CHARACTERISTICS

(V_{CC} = 5.0V, T_A = -55°C to +125°C)

Parameter Read Cycle	Symbol	-25		-35		-45		Units
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	25		35		45		nS
Address Access Time	t_{AA}		25		35		45	nS
Output Hold from Address Change	t_{OH}	5		5		5		nS
Chip Select Access Time	t_{ACS}		25		35		45	nS
Output Enable to Output Valid	t_{OE}		15		20		25	nS
Chip Select to Output in Low Z	t_{CLZ}	5		5		5		nS
Output Enable to Output in Low Z	t_{OLZ}[1]	5		5		5		nS
Chip Disable to Output in High Z	t_{CHZ}[1]		12		15		20	nS
Output Disable to Output in High Z	t_{OHZ}[1]		12		15		20	nS

1. This parameter is guaranteed by design but not tested.

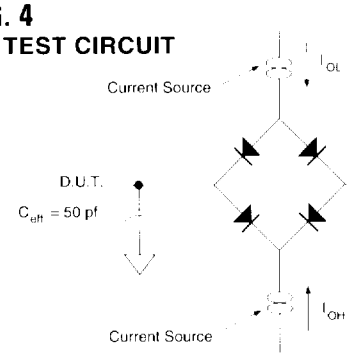
AC CHARACTERISTICS

(V_{CC} = 5.0V, T_A = -55°C to +125°C)

Parameter Write Cycle	Symbol	-25		-35		-45		Units
		Min	Max	Min	Max	Min	Max	
Write Cycle Time	t_{WC}	25		35		45		nS
Chip Select to End of Write	t_{CW}	20		30		40		nS
Address Valid to End of Write	t_{AW}	20		30		40		nS
Data Valid to End of Write	t_{DW}	15		18		20		nS
Write Pulse Width	t_{WP}	20		30		40		nS
Address Setup Time	t_{AS}	0		0		0		nS
Address Hold Time	t_{AH}	0		0		0		nS
Output Active from End of Write	t_{OW}[1]	5		5		5		nS
Write Enable to Output in High Z	t_{WHZ}[1]		10		15		15	nS
Data Hold from Write Time	t_{DH}	0		0		0		nS

1. This parameter is guaranteed by design but not tested.

FIG. 4
AC TEST CIRCUIT



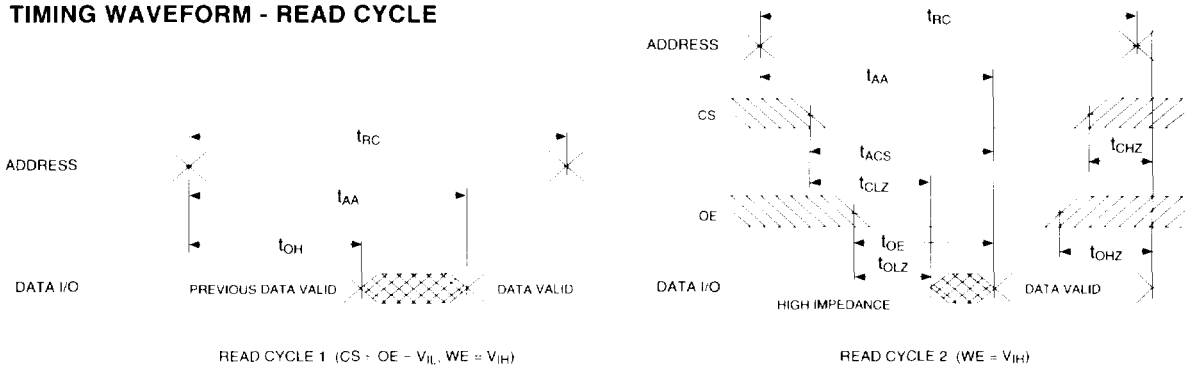
V_Z = 1.5V
(Bipolar Supply)

AC TEST CONDITIONS

Parameter	Typ	Unit
Input Pulse Levels	V_{IL} = 0, V_{IH} = 3.0	V
Input Rise and Fall	5	nS
Input and Output Reference Level	1.5	V
Output Timing Reference Level	1.5	V

NOTES:
V_Z is programmable from -2V to +7V.
I_{OL} & I_{OH} programmable from 0 to 16mA.
Tester Impedance Z_0 = 75 Ω.
V_Z is typically the midpoint of V_{OH} and V_{OL}.
I_{OL} & I_{OH} are adjusted to simulate a typical resistive load circuit.
ATE tester includes jig capacitance.

FIG. 5
TIMING WAVEFORM - READ CYCLE



READ CYCLE 1 ($\overline{CS}$ = $\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH})

READ CYCLE 2 ($\overline{WE}$ = V_{IH})

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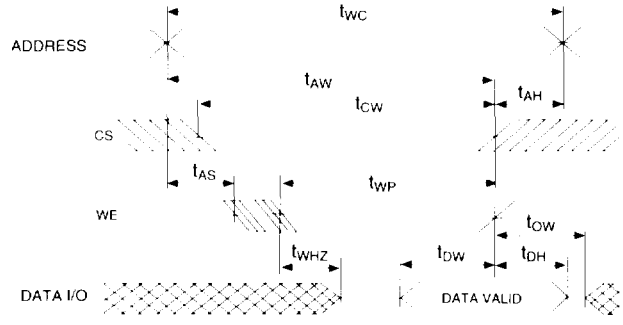
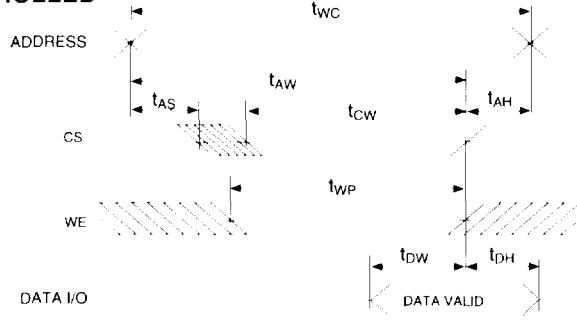
FIG. 6
WRITE CYCLE - $\overline{WE}$ CONTROLLED



WRITE CYCLE 1, $\overline{WE}$ CONTROLLED ($\overline{OE}$ = V_{IH})

FIG. 7
WRITE CYCLE - $\overline{CS}$ CONTROLLED



WRITE CYCLE 2, $\overline{CS}$ CONTROLLED ($\overline{OE}$ = V_{IH})

ORDERING INFORMATION

W S 128K 32 X - XXX X X X

SPECIAL PROCESSING:
E = Epitaxial Layer

DEVICE GRADE:
Q = MIL-STD-883 Compliant
M = Military Screened -55°C to +125°C
I = Industrial -40°C to +85°C
C = Commercial 0°C to +70°C

PACKAGE TYPE:
H = Ceramic Hex-In-line Package, HIP (Package 401)
G2 = 22 mm Ceramic Quad Flat Pack, CQFP (Package 500)
G4 = 40 mm Ceramic Quad Flat Pack, CQFP (Package 501)
G4T = 40 mm Low Profile CQFP (Package 502)

ACCESS TIME in nS

IMPROVEMENT MARK:
N = No Connect at pin 8, 21, 28 and 39 in HIP for Upgrades

ORGANIZATION, 128Kx32
User configurable as 256Kx16 or 512Kx8

SRAM

WHITE MICROELECTRONICS

Device Type	Speed	Package	SMD Number
128K x 32 SRAM Module	45nS	66 pin HIP	5962-93187 06HXX
128K x 32 SRAM Module	**35nS**	**66 pin HIP**	**5962-93187 07HXX**
128K x 32 SRAM Module	25nS	66 pin HIP	5962-93187 08HXX
128K x 32 SRAM Module	45nS	68 pin CQFP	5962-95595 06HXX
128K x 32 SRAM Module	**35nS**	**68 pin CQFP**	**5962-95595 07HXX**
128K x 32 SRAM Module	25nS	68 pin CQFP	5962-95595 08HXX