TDC1058
Monolithic Video A/D Converter
8-Bit, 20 Msps, Low Power

Description

The TDC1058 is a flash analog-to-digital converter capable of converting a video-speed signal into a stream of 8-bit digital words at 20 Msps (MegaSamples Per Second). Since the TDC1058 is a flash converter, a sample-and-hold circuit is not required.

The TDC1058 consists of 255 clocked latching comparators, combining logic, and an output register. A single convert clock controls the conversion operation. The unit can be configured to give either true or inverted outputs in binary or offset two's complement coding. All digital I/Os are TTL compatible.

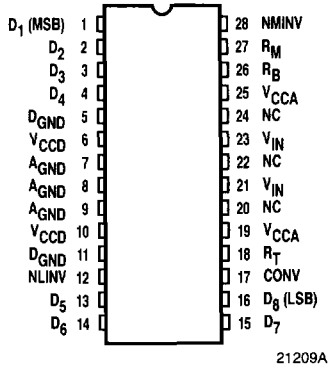
Features

- 8-bit resolution
- DC to 20 Msps conversion rate
- 7 MHz full-power bandwidth
- 60 MHz small signal -3 dB bandwidth
- 1/2 LSB linearity
- 600 mW power dissipation
- +5V single supply operation
- Lowest cost
- Pin compatible with CXA1096P, ADC-304
- Sample-and-hold circuit not required
- Analog input range +3V to +5V
- Differential phase 0.5°
- Differential gain 1%
- Selectable data format
- Available in plastic DIP, CERDIP, and PLCC

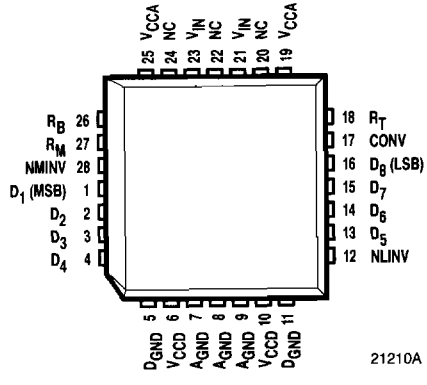
Applications

- Digital television
- PC-based data acquisition
- Video digitizing
- Medical imaging
- High energy physics
- Low cost, low power, high-speed data conversion

Pin Assignments

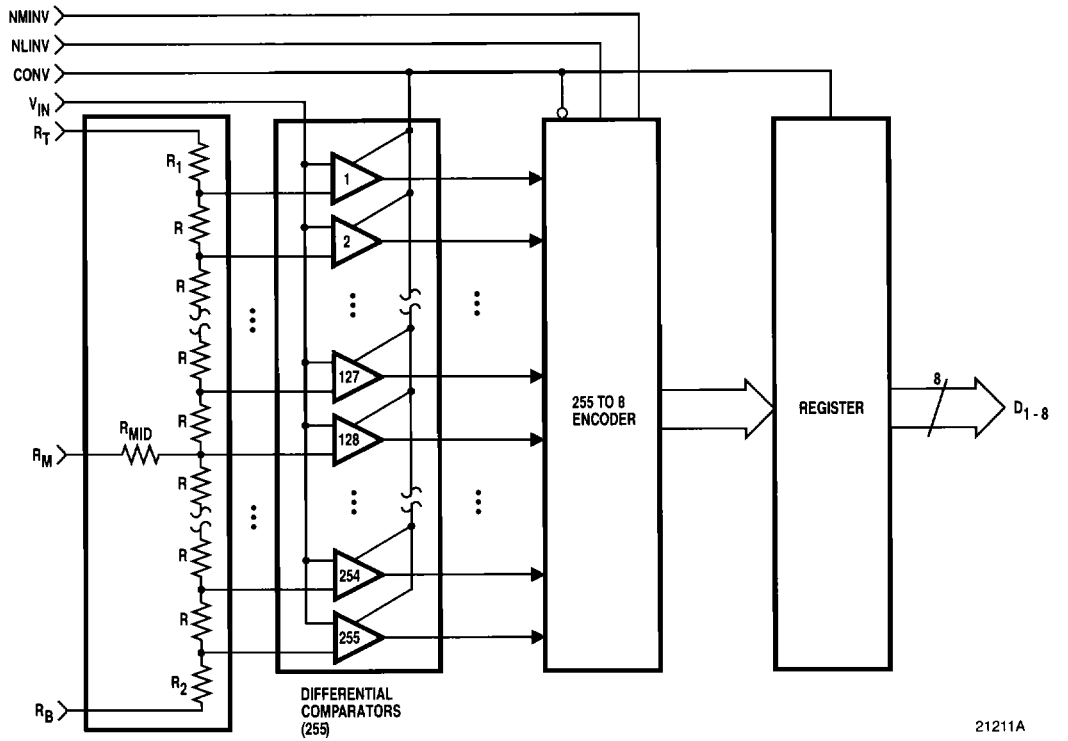


28 Pin CERDIP – B6 Package
28 Pin Plastic DIP – N6 Package



28 Leaded Plastic Chip Carrier – R3 Package

Functional Block Diagram



Functional Description

General Information

The TDC1058 has three functional sections: a comparator array, encoding logic, and output registers. The comparator array compares the input signal with 255 reference voltages to produce an N-of-255 code (or thermometer code, since all the comparators whose reference is more negative than the input signal will be on, and all those whose reference is more positive will be off). The encoding logic converts the N-of-255 code into the user's choice of coding. The output register holds the output constant between updates.

Power

The TDC1058 operates from a single supply voltage: +5.0V. All power and ground pins must be connected.

Reference

The TDC1058 converts analog signals in the range $V_{RB} \leqslant V_{IN} \leqslant V_{RT}$ into digital form. Nominally, V_{RB} is set to 3V and V_{RT} is set to 5V. However, the specifications of the TDC1058 are guaranteed as long as the following three reference operating conditions are met: 1.) the voltage applied across the reference resistor

Reference (cont.)

chain (V_{RT}-V_{RB}) is within the range of 1.8 to 2.2V, 2.) $V_{RT} \leq (V_{CCA} + 0.1V)$ and 3.) $V_{RB} \geq 2.65V$. Therefore, if the supply voltage is expected to drop below 4.9V, the reference voltages should be lowered accordingly. For instance, if the system design allows the supply voltage to drop to the minimum recommended value of 4.75V, V_{RT} should be set to 4.65V and V_{RB} should be set to 2.65V. These reference voltages will allow the TDC1058 to give fully guaranteed performance over the full supply voltage range. See the ***Operating Conditions Table*** for further information.

Linearity is guaranteed with no adjustment; however, a midpoint tap, R_M, allows for the optional trimming of converter integral linearity as well as the creation of a nonlinear transfer function. This is explained in the ***Application Note TP-19 "Non-Linear A/D Conversion."*** The circuit shown in ***Figure 7*** will provide approximately a 1/2 LSB adjustment of the linearity at midscale. The characteristic impedance seen at this node is approximately 220 Ohms and should be driven from a low-impedance source. Note that any load applied to this node will affect linearity and any noise introduced at this point will degrade the overall SNR. Due to the slight variation in the reference current with clock and input signals, R_T and R_B should be low-impedance-to-ground points. For circuits in which the reference is not varied, a bypass capacitor (0.01 to 0.1μF) to ground is recommended. If the reference inputs are exercised dynamically (as in an automatic gain control circuit) a low-impedance reference source is required. The reference voltages may be varied dynamically at up to 5MHz; however, device performance is specified with fixed reference voltages as defined in the ***Operating Conditions Table***.

Analog Input

For precise quantization, the TDC1058 uses latching comparators. The source impedance of the driving circuit must be less than 25 Ohms, for optimum overall system performance. If the input signal is between the V_{RT} and V_{RB} references, the output will be a binary number from 0 to 255. When a signal outside the recommended input voltage range (V_{RB} to V_{RT}) is applied, the output will remain at either full-scale value. The input signal will not damage the TDC1058 if it remains within the range specified in the ***Absolute Maximum Ratings Table***. Both analog input pins are connected together internally and therefore either one or both may be used.

Convert

The TDC1058 requires an external convert (CONV) signal. Because the TDC1058 is a flash converter it does not require a track-and-hold circuit. A sample is taken (the outputs of the comparators are latched) within t_{STO} (Sampling Time Offset) after a rising edge on the CONV pin. The result is encoded on the falling edge, and then transferred to the output registers on the next rising edge. The output becomes valid t_D (Output Delay Time) after the rising edge of CONVert and remains valid for at least t_{HO} (Output Hold Time) after the rising edge of CONVert. Therefore, the value of sample N becomes valid t_D after the rising edge of clock N+1 and remains valid until t_{HO} after the rising edge of clock N+2. (See *Figure 1, Timing Diagram.*)

Output Format Control

Two output format control pins, NMINV and NLINV, are provided. These controls are for DC (i.e., steady state) use. They permit the output coding to be either straight binary or offset two's complement, in either true or inverted sense, according to the ***Output Coding Table***. These pins are active LOW, as signified by the N prefix in the signal name. They may be tied to V_{CC} (through a 4.7 kOhm resistor) for a logic HIGH or D_{GND} for a logic LOW.

Outputs

The outputs of the TDC1058 are TTL compatible and capable of driving four low-power Schottky TTL (54/74 LS) loads or the equivalent. The outputs hold the previous data for a minimum of t_{HO} after the rising edge of the CONVert signal.

Not Connected

There are several pins that have no internal connection to the chip. They should be left open.

Package Interconnections

Signal Type	Signal Name	Function	Value	B6, N6, R3 Package Pins
Power	V_{CCD}	Digital Supply Voltage	+5.0V	6, 10
	V_{CCA}	Analog Supply Voltage	+5.0V	19, 25
	A_{GND}	Analog Ground	0.0V	7, 8, 9
	D_{GND}	Digital Ground	0.0V	5, 11
Reference	R_T	Reference Resistor (Top)	5.0V	18
	R_M	Reference Resistor (Middle)	4.0V	27
	R_B	Reference Resistor (Bottom)	3.0V	26
Analog Input	V_{IN}	Analog Signal Input	See Text	21, 23
Convert	CONV	Convert	TTL	17
Format Control	NMINV	Not Most Significant Bit Invert	TTL	28
	NLINV	Not Least Significant Bit Invert	TTL	12
Data Output	D_1	Most Significant Bit Output	TTL	1
	D_2		TTL	2
	D_3		TTL	3
	D_4		TTL	4
	D_5		TTL	13
	D_6		TTL	14
	D_7		TTL	15
	D_8	Least Significant Bit Output	TTL	16
Not Connected	NC	Not Connected	Open	20, 22, 24

Figure 1. Timing Diagram

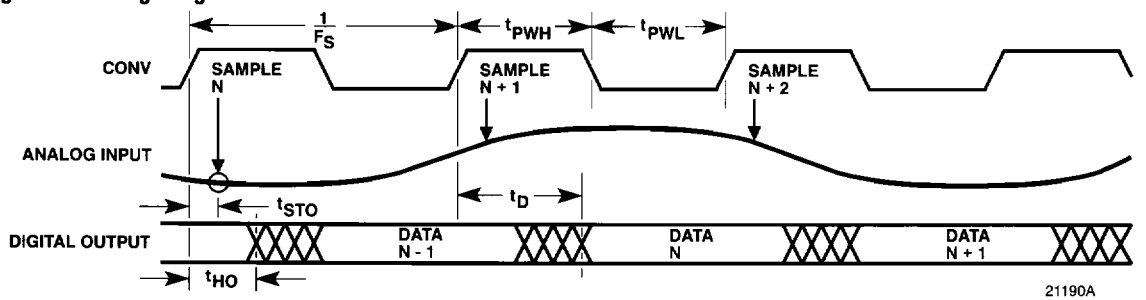
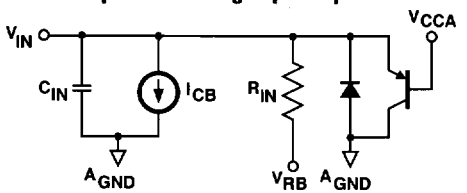


Figure 2. Simplified Analog Input Equivalent Circuit



C_{IN} IS A NONLINEAR JUNCTION CAPACITANCE
V_{RB} IS A VOLTAGE EQUAL TO THE VOLTAGE ON PIN R_B

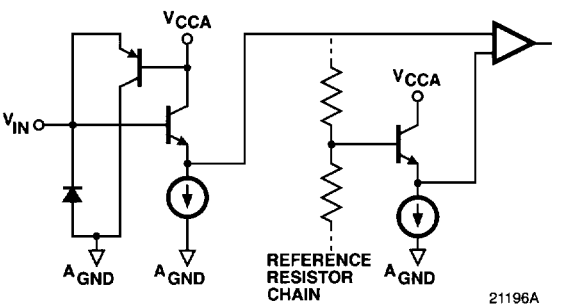


Figure 3. Convert Input Equivalent Circuit

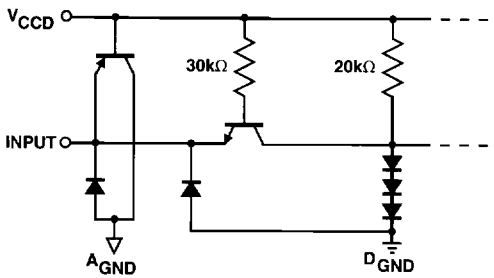
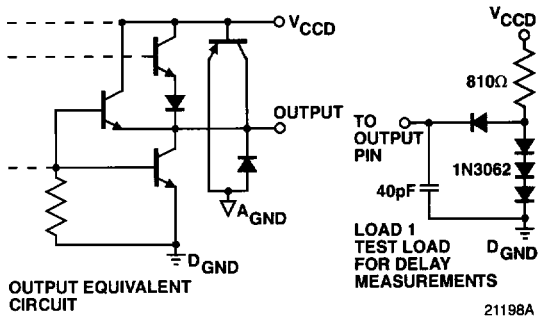


Figure 4. Output Circuit



Output Coding Table

Input Voltage	Binary		Offset Two's Complement	
	True	Inverted	True	Inverted
	NMINV = HIGH NLINV = HIGH	NMINV = LOW NLINV = LOW	NMINV = LOW NLINV = HIGH	NMINV = HIGH NLINV = LOW
5.0000V	0000 0000	1111 1111	1000 0000	0111 1111
4.9922V	0000 0001	11111110	1000 0001	0111 1110
•	•	•	•	•
•	•	•	•	•
•	•	•	•	•
4.0078V	0111 1111	1000 0000	1111 1111	0000 0000
4.0000V	1000 0000	0111 1111	0000 0000	1111 1111
3.9922V	1000 0001	0111 1110	0000 0001	1111 1110
•	•	•	•	•
•	•	•	•	•
•	•	•	•	•
3.0156V	1111 1110	0000 0001	0111 1110	1000 0001
3.0078V	1111 1111	0000 0000	0111 1111	1000 0000

Notes:
1. NMINV and NLINV are to be considered DC controls. They may be tied to +5V through a 4.7 kOhm resistor for a logic HIGH or tied to ground for a logic LOW.
2. Voltages are code midpoints.

Absolute maximum ratings (beyond which the device may be damaged) [1]

Power Supply Voltages

V_{CCA} (measured to A_{GND})	-0.5 to +7.0V
V_{CCD} (measured to D_{GND})	-0.5 to +7.0V
A_{GND} (measured to D_{GND})	-0.5 to +0.5V

Input Voltages

CONV, NLINV, NMINV	-0.5 to V_{CC}+0.5V
V_{IN}, V_{RT}, V_{RB} (measured to A_{GND})	-0.5 to +5.5V
V_{RT} (measured to V_{RB})	-2.2 to +2.2V

Input Currents

CONV, NLINV, NMINV	-50 to +50 mA
V_{IN}, V_{RT}, V_{RB}	-100 to +100 mA

Digital Outputs

Applied voltage[2]	-0.5 to V_{CC}+0.5V
Applied current[3,4]	-50 to +50 mA
Short-circuit duration (single output in HIGH state to GND)	1 second.

Temperature

Operating, ambient (all packages except N6 and R3)	-55 to +125°C
(N6 and R3 packages only)	-20 to 90°C
junction (all packages)	+175°C
Lead, soldering, all packages (10 seconds)	+300°C
Storage	-65 to +150°C

Notes:
1. Absolute maximum ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied.
2. Applied voltage must be current limited to specified range, and measured with respect to GND.
3. Forcing voltage must be limited to specified range.
4. Current is specified as conventional current, flowing into the device.

Operating Conditions

Parameter		Temperature Range						Units
		Standard			Extended			
		Min	Nom	Max	Min	Nom	Max	
V_{CCA}	Analog Supply Voltage	4.75	5.0	5.25	4.50	5.0	5.50	V
V_{CCD}	Digital Supply Voltage	4.75	5.0	5.25	4.50	5.0	5.50	V
V_{AGND}	Analog Ground Voltage (Measured to D_{GND})	-0.1	0.0	0	+0.1	0	0.1	V
t_{PWL}	CONV Pulse Width, LOW	19			18			ns
t_{PWH}	CONV Pulse Width, HIGH	27			22			ns
V_{IL}	Input Voltage, Logic LOW			0.8			0.8	V
V_{IH}	Input Voltage, Logic HIGH	2.0			2.0			V
I_{OL}	Output Current, Logic LOW			4.0			4.0	mA
I_{OH}	Output Current, Logic HIGH			-400			-400	µA
V_{RT}	Most Positive Reference Input [1]		5.0	V_{CCA} = 0.1	4.9	5.0	5.1	V
V_{RB}	Most Negative Reference Input [1]	2.65	3.0		2.9	3.0	3.1	V
V_{RT}-V_{RB}	Voltage Reference Differential	1.8	2.0	2.2	1.8	2.0	2.2	V
V_{IN}	Input Voltage	V_{RB}		V_{RT}	V_{RB}		V_{RT}	V
T_A	Ambient Temperature, Still Air	0		70				°C
TA	Case Temperature				-55		125	°C

Note: 1. V_{RT} must be more positive than V_{RB}, and voltage reference differential must be within specified range.

Thermal characteristics (approximate)

Parameter		Package	Typical	Units
Θ_{ja}	Thermal Resistance, Junction to Ambient	N6	45	°C/W
		R3	65	°C/W
		B6	50	°C/W
Θ_{jc}	Thermal Resistance, Junction to Case	N6	17	°C/W
		R3	14	°C/W
		B6	TBD	°C/W

Electrical characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range				Units
			Standard		Extended		
			Min	Max	Min	Max	
$I_{CCA} + I_{CCD}$	Total Supply Current	V_{CC}=Max[1]		160		160	mA
I_{REF}	Reference Current	V_{RT}, V_{RB}=Nom		30		50	mA
R_{REF}	Total Reference Resistance		67		40		Ohms
R_{IN}	Input Equivalent Resistance	V_{RT}, V_{RB}=Nom, V_{IN}=V_{RB}	80		40		kOhms
C_{IN}	Input Capacitance	V_{RT}, V_{RB}=Nom, V_{IN}=V_{RB}		50		50	pF
I_{CB}	Input Constant Bias Current	V_{CCA}=Max		250		500	µA
I_{IL}	Input Current, Logic LOW	V_{CC}=Max, V_I=0.4V		-0.6		-0.6	mA
I_{IH}	Input Current, Logic HIGH	V_{CC}=Max, V_I=2.4V	-200	50	-400	50	µA
I_I	Input Current, Max Input Voltage	VCC=Min, I_{OL}=Max		1.0		1.0	mA
V_{OL}	Output Voltage, Logic LOW	V_{CC}=Min, I_{OL}=Max		0.5		0.5	V
V_{OH}	Output Voltage, Logic HIGH	V_{CC}=Min, I_{OH}=Max	2.4		2.4		V
I_{OS}	Short-Circuit Output Current	V_{CC}=Max, Output HIGH, one pin to ground, one second duration max		-40		-40	mA
C_I	Digital Input Capacitance	T_A=25°C, F=1 MHz		15		15	pF

Note: 1. Worst case, all digital inputs and outputs LOW.

Switching characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range				Units
			Standard		Extended		
			Min	Max	Min	Max	
F_S	Maximum Conversion Rate		20		20		Msps
t_{STO}	Sampling Time Offset		-2	10	-2	10	ns
t_D	Output Delay	V_{CC}=Min, Load 1, Figure 4		35		35	ns
t_{HO}	Output Hold Time	V_{CC}=Min, Load 1, Figure 4	5		5		ns

System performance characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range				Units
			Standard		Extended		
			Min	Max	Min	Max	
E_{LI}	Linearity Error Integral, Independent	V_{RT}, V_{RB}=Nom		0.2		±0.2	%
E_{LD}	Linearity Error Differential			0.2		±0.2	%
C_S	Code Size		25	175	25	175	% Nom
E_{OT}	Offset Error, Top	V_{IN}=V_{RT}	-10	+10		+15	mV
E_{OB}	Offset Error, Bottom	V_{IN}=V_{RB}		-15		-15	mV
T_{CO}	Offset Error, Temperature Coefficient		-20	±20		±20	µV/°C
BW	Bandwidth, Full-Scale Input	No Spurious or Missing Codes	7		7		Mhz
BW_{SS}	-3 dB Bandwidth, Small Signal	-20 dBFS Input	60		60		MHz
t_{TR}	Transient Response, Full Scale		70		70		ns
SNR	Signal-to-Noise Ratio	10 MHz Bandwidth, 20 Msps Conversion Rate					
	Peak Signal/RMS Noise	1.248 MHz Input	54		53		dB
		2.438 MHz Input	53		52		dB
	RMS Signal/RMS Noise	1.248 MHz Input	45		44		dB
		2.438 MHz Input	44		43		dB
E_{AP}	Aperture Error			60		60	ps
DG	Differential Gain Error	F_S=4 x NTSC		2.0		2.0	%

Figure 5. Typical Interface Circuit

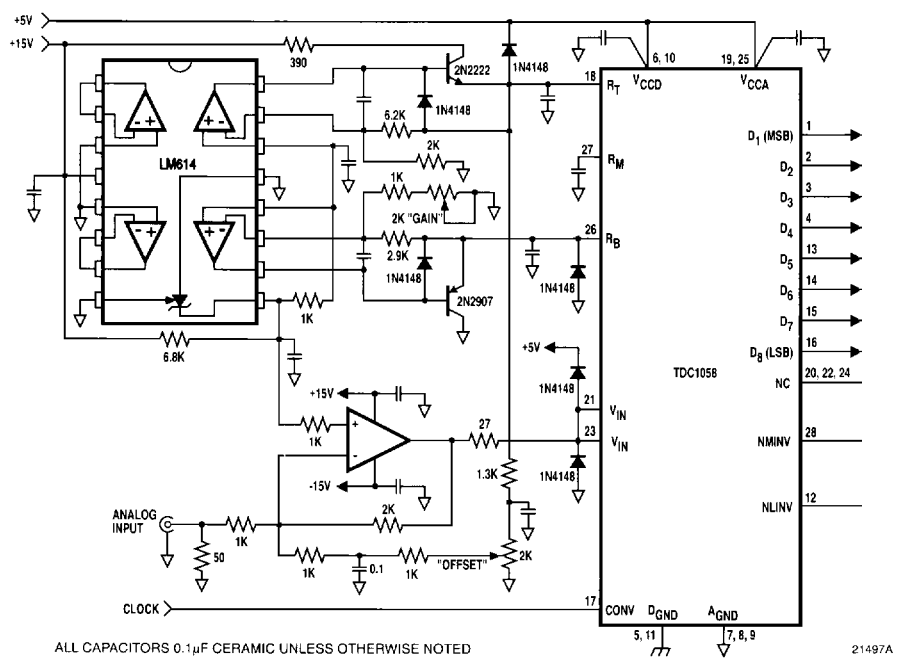


Figure 6. Inexpensive Interface Circuit

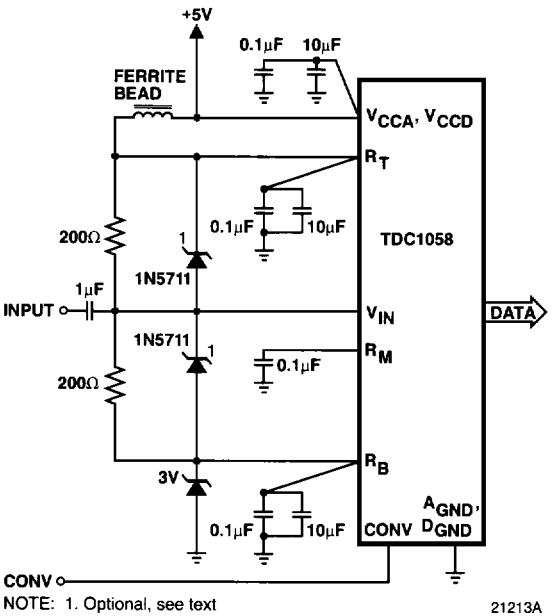
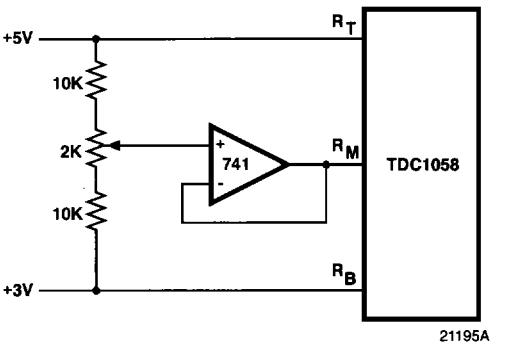


Figure 7. Optional Midscale Linearity Adjust



Typical Interface Circuit

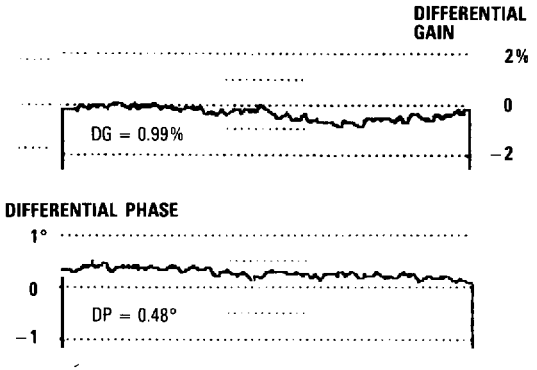
The *Typical Interface Circuit (Figure 5)* shows an example of a high-performance application circuit for the TDC1058. The wideband analog input amplifier drives the A/D converter directly. Bipolar inputs to the amplifier can be accommodated by adjusting the offset control. TRW's TDC4614 provides a stable reference for both the offset and gain control. All V_{IN} pins are con-nected close to the device package and the input ampli-fier's feedback loop should be closed at that point. The buffer has an inverting gain of two, increasing a 1Vp-p video input signal to the recommended 2Vp-p input for the TDC1058. Proper decoupling is recommended for all systems.

The bottom reference voltage (V_{RB}) is supplied by an inverting amplifier or the TDC4614, buffered with a PNP transistor. The transistor provides a low-impedance source and is necessary to sink the current flowing through the reference resistor chain.

The ***Inexpensive Interface Circuit*** shown in ***Figure 6*** offers considerable parts reduction for cost-sensitive applications where DC response is not required and loss of some power supply rejection is tolerable. The 200 Ohm resistors bias the input to +4V and provide the current to the zener diode to provide the reference bottom voltage. The 1µF capacitor decouples the input signal from the DC voltage present at the input of the TDC1058. The 10µF and 0.1µF capacitors, as well as the ferrite bead, provide power supply decoupling. The 1N5711 Schottky diodes are for protection against overvoltages at the input and are not required if these precautions are taken elsewhere in the circuit.

Typical Performance Curves

A. Typical Differential Phase and Gain



Convert Frequency = 14.3181800MHz
Analog Input = 3.57954550MHz

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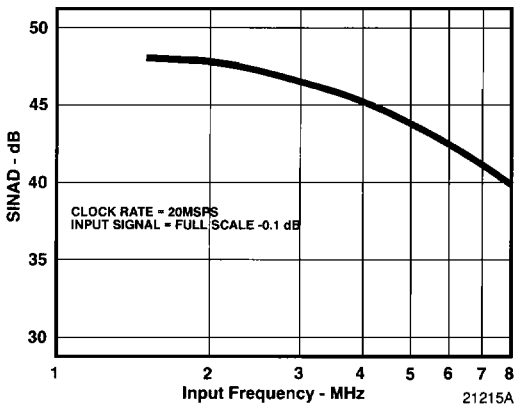
B. Typical SINAD (SNR + Distortion) vs. Input Frequency



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Ordering Information

Product Number	Temperature Range	Screening	Package	Package Marking
TDC1058B6C	STD - T_A = 0°C to 70°C	Commercial	28-Pin CERDIP	1058B6C
TDC1058B6V	EXT - T_C = -55°C to 125°C	MIL-STD-883	28-Pin CERDIP	1058B6V
TDC1058N6C	STD - T_A = 0°C to 70°C	Commercial	28-Pin Plastic DIP	1058N6C
TDC1058R3C	STD - T_A = 0°C to 70°C	Commercial	28-Lead Plastic J-Leaded Chip Carrier	1058R3C

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