

CMOS single-chip 8-bit microcontrollers

80C52/80C54/80C58

DESCRIPTION

The 80C52/80C54/80C58 Single-Chip 8-Bit Microcontroller is manufactured in an advanced CMOS process and is a derivative of the 80C51 microcontroller family. The 80C52/80C54/80C58 has the same instruction set as the 80C51.

This device provides architectural enhancements that make it applicable in a variety of applications for general control systems. The 80C52 contains 8k × 8 ROM memory, the 80C54 contains 16k × 8 ROM memory, and 80C58 contains 32k × 8 ROM memory, a volatile 256 × 8 read/write data memory, four 8-bit I/O ports, three 16-bit timer/event counters, a multi-source, four-priority-level, nested interrupt structure, an enhanced UART and on-chip oscillator and timing circuits. For systems that require extra capability, the 80C52/54/58 can be expanded using standard TTL compatible memories and logic.

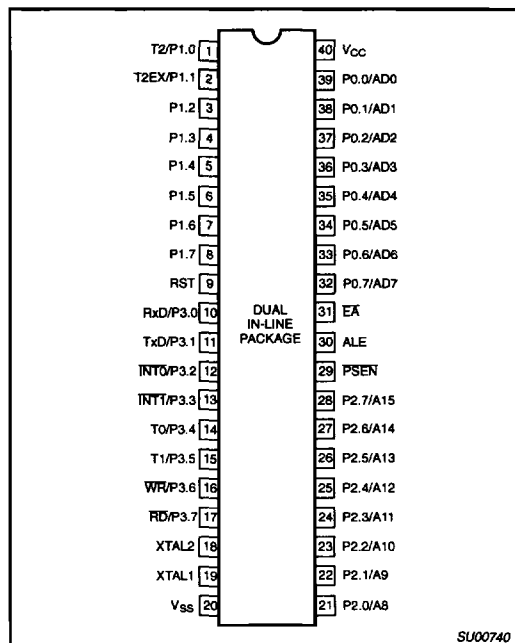
Its added features make it an even more powerful microcontroller for applications that require pulse width modulation, high-speed I/O and up/down counting capabilities such as motor control. It also has a more versatile serial channel that facilitates multiprocessor communications.

See 87C52/80C32 and 87C54/87C58 data sheets for EPROM and ROMless devices.

FEATURES

- 80C51 central processing unit
- Full static operation
- 8k × 8 ROM: 80C52;
16k × 8 ROM: 80C54;
32k × 8 ROM: 80C58;
all capable of addressing external memory to 64k bytes
 - Two level program security system
 - 64 byte encryption array
- 256 × 8 RAM, expandable externally to 64k bytes
- Speed range up to 33MHz
- Operating voltage 5V ±10%
- Three 16-bit timer/counters
 - T2 is an up/down counter
- 6 interrupt sources
- 4 level priority
- Four 8-bit I/O ports
- Full-duplex enhanced UART
 - Framing error detection
 - Automatic address recognition
- Power control modes
 - Idle mode
 - Power-down mode
- Once (On Circuit Emulation) Mode
- Five package styles
- Programmable clock out
- Low EMI (Inhibit ALE)
- Second DPTR register
- Asynchronous port reset

PIN CONFIGURATIONS



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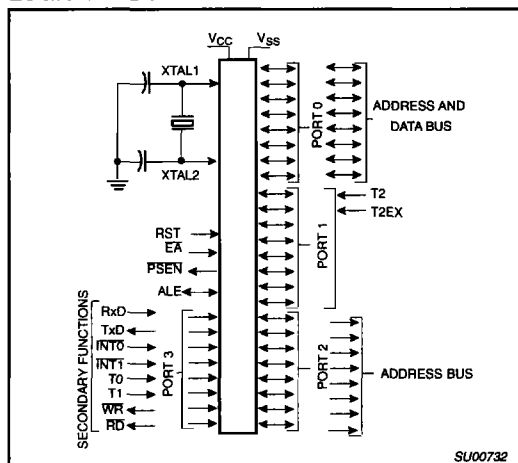
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ORDERING INFORMATION

ROM 8k x 8	ROM 16k x 8	ROM 32k x 8	TEMPERATURE RANGE °C AND PACKAGE	FREQ MHz	DRAWING NUMBER
P80C52EBPN	P80C54EBPN	P80C58EBPN	0 to +70, Plastic Dual In-line Package	16	SOT129-1
P80C52EBAA	P80C54EBAA	P80C58EBAA	0 to +70, Plastic Leaded Chip Carrier	16	SOT187-2
P80C52EBBB	P80C54EBBB	P80C58EBBB	0 to +70, Plastic Quad Flat Pack	16	SOT307-2
P80C52EFPN	P80C54EFPN	P80C58EFPN	-40 to +85, Plastic Dual In-line Package	16	SOT129-1
P80C52EFA A	P80C54EFA A	P80C58EFA A	-40 to +85, Plastic Leaded Chip Carrier	16	SOT187-2
P80C52EFBB	P80C54EFBB	P80C58EFBB	-40 to +85, Plastic Quad Flat Pack	16	SOT307-2
P80C52IBP N	P80C54IBP N	P80C58IBP N	0 to +70, Plastic Dual In-line Package	24	SOT129-1
P80C52IBA A	P80C54IBA A	P80C58IBA A	0 to +70, Plastic Leaded Chip Carrier	24	SOT187-2
P80C52IBB B	P80C54IBB B	P80C58IBB B	0 to +70, Plastic Quad Flat Pack	24	SOT307-2
P80C52IFP N	P80C54IFP N	P80C58IFP N	-40 to +85, Plastic Dual In-line Package	24	SOT129-1
P80C52IFA A	P80C54IFA A	P80C58IFA A	-40 to +85, Plastic Leaded Chip Carrier	24	SOT187-2
P80C52IFB B	P80C54IFB B	P80C58IFB B	-40 to +85, Plastic Quad Flat Pack	24	SOT307-2
P80C52NBAA	P80C54NBAA	P80C58NBAA	0 to +70, Plastic Leaded Chip Carrier	33	SOT187-2
P80C52NBPN	P80C54NBPN	P80C58NBPN	0 to +70, Plastic Dual In-line Package	33	SOT129-1
P80C52NB BB	P80C54NB BB	P80C58NB BB	0 to +70, Plastic Quad Flat Pack	33	SOT307-2
P80C52NFA A	P80C54NFA A	P80C58NFA A	-40 to +85, Plastic Leaded Chip Carrier	33	SOT187-2
P80C52NFPN	P80C54NFPN	P80C58NFPN	-40 to +85, Plastic Dual In-line Package	33	SOT129-1
P80C52NFBB	P80C54NFBB	P80C58NFBB	-40 to +85, Plastic Quad Flat Pack	33	SOT307-2

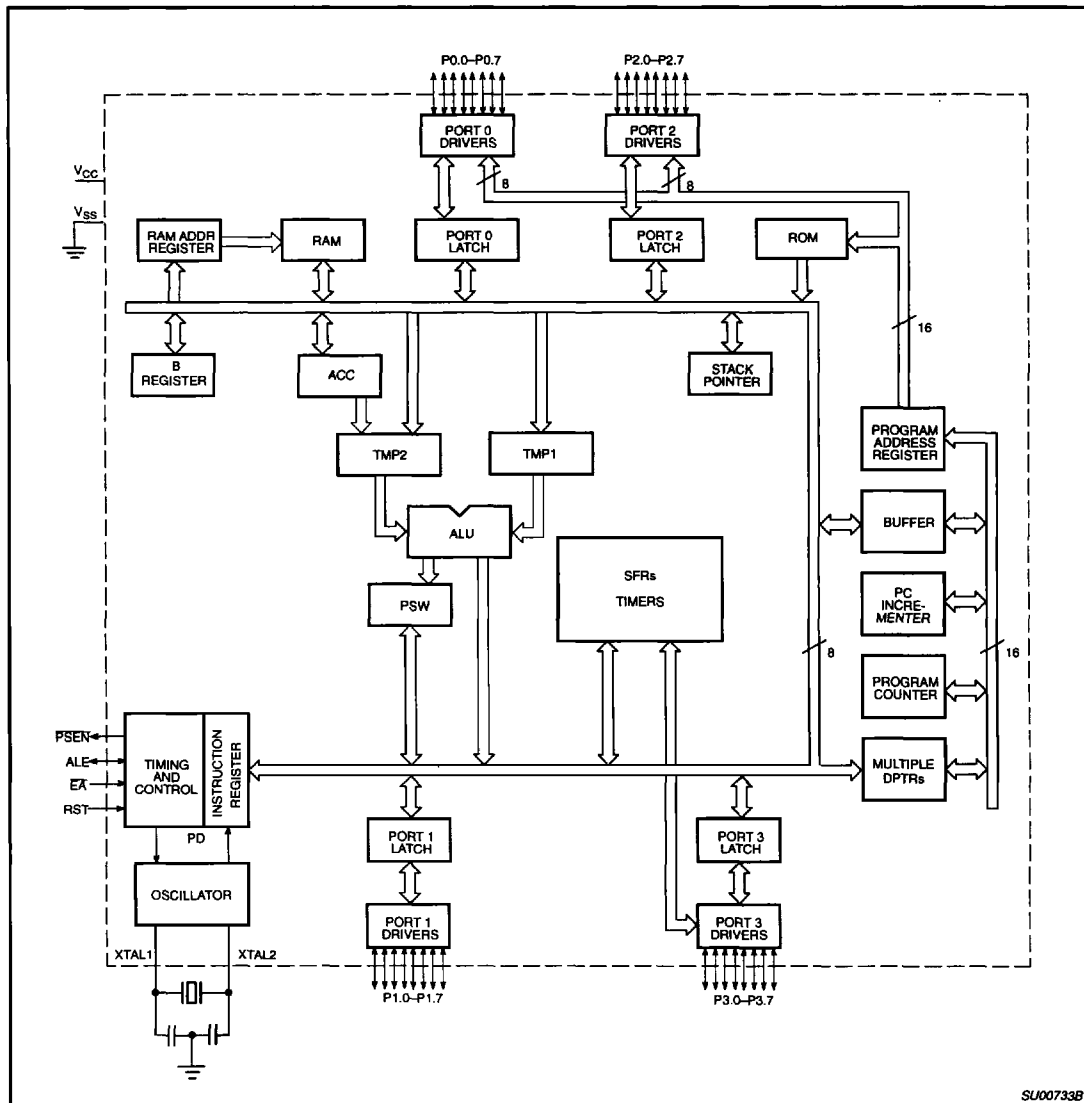
LOGIC SYMBOL



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BLOCK DIAGRAM



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Table 1. 80C52/80C54/80C58 Special Function Registers

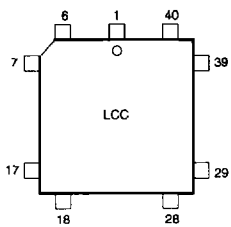
SYMBOL	DESCRIPTION	DIRECT ADDRESS	BIT ADDRESS, SYMBOL, OR ALTERNATIVE PORT FUNCTION								RESET VALUE
			MSB				LSB				
ACC*	Accumulator	E0H	E7	E6	E5	E4	E3	E2	E1	E0	00H
AUXR#	Auxiliary	8EH	-	-	-	-	-	-	-	AO	xxxxxxx0B
AUXR1#	Auxiliary 1	A2H	-	-	-	-	-	-	-	DPS	xxxxxxx0B
B*	B register	F0H	F7	F6	F5	F4	F3	F2	F1	F0	00H
DPTR:	Data Pointer (2 bytes)										
DPH	Data Pointer High	83H									00H
DPL	Data Pointer Low	82H									00H
			AF	AE	AD	AC	AB	AA	A9	A8	
IE*	Interrupt Enable	A8H	EA	EC	ET2	ES	ET1	EX1	ET0	EX0	00H
			BF	BE	BD	BC	BB	BA	B9	BB	
IP*	Interrupt Priority	B8H	-	-	PT2	PS	PT1	PX1	PT0	PX0	x0000000B
			B7	B6	B5	B4	B3	B2	B1	B0	
IPH#	Interrupt Priority High	B7H	-	-	PT2H	PSH	PT1H	PX1H	PT0H	PX0H	x0000000B
			87	86	85	84	83	82	81	80	
P0*	Port 0	80H	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0	FFH
			97	96	95	94	93	92	91	90	
P1*	Port 1	90H	-	-	-	-	-	-	T2EX	T2	FFH
			A7	A6	A5	A4	A3	A2	A1	A0	
P2*	Port 2	A0H	AD15	AD14	AD13	AD12	AD11	AD10	AD9	AD8	FFH
			B7	B6	B5	B4	B3	B2	B1	B0	
P3*	Port 3	B0H	RD	WR	T1	T0	INT1	INT0	TxD	RxD	FFH
PCON#1	Power Control	87H	SMOD1	SMOD0	-	POF ²	GF1	GF0	PD	IDL	00xx0000B
			D7	D6	D5	D4	D3	D2	D1	D0	
PSW*	Program Status Word	D0H	CY	AC	F0	RS1	RS0	OV	-	P	00H
RACAP2H#	Timer 2 Capture High	CBH									00H
RACAP2L#	Timer 2 Capture Low	CAH									00H
SADDR#	Slave Address	A9H									00H
SADEN#	Slave Address Mask	B9H									00H
SBUF	Serial Data Buffer	99H									xxxxxxx0B
			9F	9E	9D	9C	9B	9A	99	98	
SCON*	Serial Control	98H	SMQ/FE	SM1	SM2	REN	TB8	RB8	T1	RI	00H
SP	Stack Pointer	81H									07H
			8F	8E	8D	8C	8B	8A	89	88	
TCON*	Timer Control	88H	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0	00H
			CF	CE	CD	CC	CB	CA	C9	C8	
T2CON*	Timer 2 Control	C8H	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/T2	CP/RL2	00H
T2MOD#	Timer 2 Mode Control	C9H	-	-	-	-	-	-	T2OE	DCEN	xxxxxx00B
TH0	Timer High 0	8CH									00H
TH1	Timer High 1	8DH									00H
TH2#	Timer High 2	CDH									00H
TL0	Timer Low 0	8AH									00H
TL1	Timer Low 1	8BH									00H
TL2#	Timer Low 2	CCH									00H
TMOD	Timer Mode	89H	GATE	C/T	M1	M0	GATE	C/T	M1	M0	00H

* SFRs are bit addressable.
 # SFRs are modified from or added to the 80C51 SFRs.
 - Reserved bits.
 1. Reset value depends on reset source.
 2. Bit will not be affected by Reset. POF is not present in 80C52.

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PLASTIC LEADED CHIP CARRIER PIN FUNCTIONS

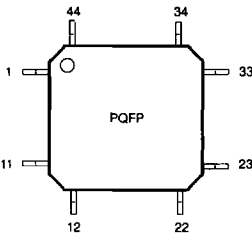


Pin	Function	Pin	Function	Pin	Function
1	NC*	16	P3.4/T0	31	P2.7/A15
2	P1.0/T2	17	P3.5/T1	32	PSEN
3	P1.1/T2EX	18	P3.6/WR	33	ALE
4	P1.2	19	P3.7/RD	34	NC*
5	P1.3	20	XTAL2	35	EA
6	P1.4	21	XTAL1	36	P0.7/AD7
7	P1.5	22	V _{SS}	37	P0.6/AD6
8	P1.6	23	NC*	38	P0.5/AD5
9	P1.7	24	P2.0/A8	39	P0.4/AD4
10	RST	25	P2.1/A9	40	P0.3/AD3
11	P3.0/RxD	26	P2.2/A10	41	P0.2/AD2
12	NC*	27	P2.3/A11	42	P0.1/AD1
13	P3.1/TxD	28	P2.4/A12	43	P0.0/AD0
14	P3.2/INT0	29	P2.5/A13	44	V _{CC}
15	P3.3/INT1	30	P2.6/A14		

* DO NOT CONNECT

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PLASTIC QUAD FLAT PACK PIN FUNCTIONS



Pin	Function	Pin	Function	Pin	Function
1	P1.5	16	V _{SS}	31	P0.6/AD6
2	P1.6	17	NC*	32	P0.5/AD5
3	P1.7	18	P2.0/A8	33	P0.4/AD4
4	RST	19	P2.1/A9	34	P0.3/AD3
5	P3.0/RxD	20	P2.2/A10	35	P0.2/AD2
6	NC*	21	P2.3/A11	36	P0.1/AD1
7	P3.1/TxD	22	P2.4/A12	37	P0.0/AD0
8	P3.2/INT0	23	P2.5/A13	38	V _{CC}
9	P3.3/INT1	24	P2.6/A14	39	NC*
10	P3.4/T0	25	P2.7/A15	40	P1.0/T2
11	P3.5/T1	26	PSEN	41	P1.1/T2EX
12	P3.6/WR	27	ALE	42	P1.2
13	P3.7/RD	28	NC*	43	P1.3
14	XTAL2	29	EA	44	P1.4
15	XTAL1	30	P0.7/AD7		

* DO NOT CONNECT

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PIN DESCRIPTIONS

MNEMONIC	PIN NUMBER			TYPE	NAME AND FUNCTION				
	DIP	LCC	QFP						
V _{SS}	20	22	16	I	Ground: 0V reference.				
V _{CC}	40	44	38	I	Power Supply: This is the power supply voltage for normal, idle, and power-down operation.				
P0.0–0.7	39–32	43–36	37–30	I/O	Port 0: Port 0 is an open-drain, bidirectional I/O port. Port 0 pins that have 1s written to them float and can be used as high-impedance inputs. Port 0 is also the multiplexed low-order address and data bus during accesses to external program and data memory. In this application, it uses strong internal pull-ups when emitting 1s. Port 0 also outputs the code bytes during program verification. External pull-ups are required during program verification.				
P1.0–P1.7	1–8	2–9	40–44, 1–3	I/O	Port 1: Port 1 is an 8-bit bidirectional I/O port with internal pull-ups. Port 1 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, port 1 pins that are externally pulled low will source current because of the internal pull-ups. (See DC Electrical Characteristics: I _{IL}). Port 1 also receives the low-order address byte during program memory verification. Alternate functions include: T2 (P1.0): Timer/Counter 2 external count input/Clockout T2EX (P1.1): Timer/Counter 2 Reload/Capture/Direction Control				
						1	2	40	I/O
						2	3	41	I
						3	4	42	I
						4	5	43	I/O
						5	6	44	I/O
						6	7	1	I/O
						7	8	2	I/O
8	9	3	I/O						
P2.0–P2.7	21–28	24–31	18–25	I/O	Port 2: Port 2 is an 8-bit bidirectional I/O port with internal pull-ups. Port 2 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, port 2 pins that are externally being pulled low will source current because of the internal pull-ups. (See DC Electrical Characteristics: I _{IL}). Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX @DPTR). In this application, it uses strong internal pull-ups when emitting 1s. During accesses to external data memory that use 8-bit addresses (MOV @Ri), port 2 emits the contents of the P2 special function register.				

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PIN DESCRIPTIONS (Continued)

MNEMONIC	PIN NUMBER			TYPE	NAME AND FUNCTION
	DIP	LCC	QFP		
P3.0–P3.7	10–17	11, 13–19	5, 7–13	I/O	<p>Port 3: Port 3 is an 8-bit bidirectional I/O port with internal pull-ups. Port 3 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, port 3 pins that are externally being pulled low will source current because of the pull-ups. (See DC Electrical Characteristics: I_{IL}). Port 3 also serves the special features of the 80C51 family, as listed below:</p> <p>RxD (P3.0): Serial input port</p> <p>TxD (P3.1): Serial output port</p> <p>INT0 (P3.2): External interrupt</p> <p>INT1 (P3.3): External interrupt</p> <p>T0 (P3.4): Timer 0 external input</p> <p>T1 (P3.5): Timer 1 external input</p> <p>WR (P3.6): External data memory write strobe</p> <p>RD (P3.7): External data memory read strobe</p>
		10	11	5	
	11	13	7	O	
	12	14	8	I	
	13	15	9	I	
	14	16	10	I	
	15	17	11	I	
	16	18	12	O	
	17	19	13	O	
	RST	9	10	4	
ALE	30	33	27	O	<p>Address Latch Enable: Output pulse for latching the low byte of the address during an access to external memory. In normal operation, ALE is emitted at a constant rate of 1/6 the oscillator frequency, and can be used for external timing or clocking. Note that one ALE pulse is skipped during each access to external data memory. ALE can be disabled by setting SFR auxiliary.0. With this bit set, ALE will be active only during a MOVX instruction.</p>
PSEN	29	32	26	O	<p>Program Store Enable: The read strobe to external program memory. When the 80C52/80C54/80C58 is executing code from the external program memory, PSEN is activated twice each machine cycle, except that two PSEN activations are skipped during each access to external data memory. PSEN is not activated during fetches from internal program memory.</p>
EA	31	35	29	I	<p>External Access Enable: EA must be externally held low to enable the device to fetch code from external program memory locations 0000H and 7FFFH. If EA is held high, the device executes from internal program memory unless the program counter contains an address greater than 7FFFH. If security bit 1 is programmed, EA will be internally latched on Reset.</p>
XTAL1	19	21	15	I	<p>Crystal 1: Input to the inverting oscillator amplifier and input to the internal clock generator circuits.</p>
XTAL2	18	20	14	O	<p>Crystal 2: Output from the inverting oscillator amplifier.</p>

NOTE:

To avoid "latch-up" effect at power-on, the voltage on any pin at any time must not be higher than $V_{CC} + 0.5V$ or $V_{SS} - 0.5V$, respectively.

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TIMER 2 OPERATION**Timer 2**

Timer 2 is a 16-bit Timer/Counter which can operate as either an event timer or an event counter, as selected by C/T2* in the special function register T2CON (see Figure 1). Timer 2 has three operating modes: Capture, Auto-reload (up or down counting), and Baud Rate Generator, which are selected by bits in the T2CON as shown in Table 2.

Capture Mode

In the capture mode there are two options which are selected by bit EXEN2 in T2CON. If EXEN2=0, then timer 2 is a 16-bit timer or counter (as selected by C/T2* in T2CON) which, upon overflowing sets bit TF2, the timer 2 overflow bit. This bit can be used to generate an interrupt (by enabling the Timer 2 interrupt bit in the IE register/SFR table). If EXEN2= 1, Timer 2 operates as described above, but with the added feature that a 1- to -0 transition at external input T2EX causes the current value in the Timer 2 registers, TL2 and TH2, to be captured into registers RCAP2L and RCAP2H, respectively. In addition, the transition at T2EX causes bit EXF2 in T2CON to be set, and EXF2 like TF2 can generate an interrupt (which vectors to the same location as Timer 2 overflow interrupt). The Timer 2 interrupt service routine can interrogate TF2 and EXF2 to determine which event caused the interrupt). The capture mode is illustrated in Figure 2 (There is no reload value for TL2 and TH2 in this mode. Even when a capture event occurs from T2EX, the counter keeps on counting T2EX pin transitions or osc/12 pulses.).

Auto-Reload Mode (Up or Down Counter)

In the 16-bit auto-reload mode, Timer 2 can be configured (as either a timer or counter (C/T2* in T2CON)) then programmed to count up or down. The counting direction is determined by bit DCEN(Down Counter Enable) which is located in the T2MOD register (see

Figure 3). When reset is applied the DCEN=0 which means Timer 2 will default to counting up. If DCEN bit is set, Timer 2 can count up or down depending on the value of the T2EX pin.

Figure 4 shows Timer 2 which will count up automatically since DCEN=0. In this mode there are two options selected by bit EXEN2 in T2CON register. If EXEN2=0, then Timer 2 counts up to 0FFFFH and sets the TF2 (Overflow Flag) bit upon overflow. This causes the Timer 2 registers to be reloaded with the 16-bit value in RCAP2L and RCAP2H.

The values in RCAP2L and RCAP2H are preset by software means. If EXEN2=1, then a 16-bit reload can be triggered either by an overflow or by a 1-to-0 transition at input T2EX. This transition also sets the EXF2 bit. The Timer 2 interrupt, if enabled, can be generated when either TF2 or EXF2 are 1.

In Figure 5 DCEN=1 which enables Timer 2 to count up or down. This mode allows pin T2EX to control the direction of count. When a logic 1 is applied at pin T2EX Timer 2 will count up. Timer 2 will overflow at 0FFFFH and set the TF2 flag, which can then generate an interrupt, if the interrupt is enabled. This timer overflow also causes the 16-bit value in RCAP2L and RCAP2H to be reloaded into the timer registers TL2 and TH2.

When a logic 0 is applied at pin T2EX this causes Timer 2 to count down. The timer will underflow when TL2 and TH2 become equal to the value stored in RCAP2L and RCAP2H. Timer 2 underflow sets the TF2 flag and causes 0FFFFH to be reloaded into the timer registers TL2 and TH2.

The external flag EXF2 toggles when Timer 2 underflows or overflows. This EXF2 bit can be used as a 17th bit of resolution if needed. The EXF2 flag does not generate an interrupt in this mode of operation.

		(MSB)						(LSB)	
		TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/T2	CP/RL2
Symbol	Position	Name and Significance							
TF2	T2CON.7	Timer 2 overflow flag set by a Timer 2 overflow and must be cleared by software. TF2 will not be set when either RCLK or TCLK = 1.							
EXF2	T2CON.6	Timer 2 external flag set when either a capture or reload is caused by a negative transition on T2EX and EXEN2 = 1. When Timer 2 interrupt is enabled, EXF2 = 1 will cause the CPU to vector to the Timer 2 interrupt routine. EXF2 must be cleared by software. EXF2 does not cause an interrupt in up/down counter mode (DCEN = 1).							
RCLK	T2CON.5	Receive clock flag. When set, causes the serial port to use Timer 2 overflow pulses for its receive clock in modes 1 and 3. RCLK = 0 causes Timer 1 overflow to be used for the receive clock.							
TCLK	T2CON.4	Transmit clock flag. When set, causes the serial port to use Timer 2 overflow pulses for its transmit clock in modes 1 and 3. TCLK = 0 causes Timer 1 overflows to be used for the transmit clock.							
EXEN2	T2CON.3	Timer 2 external enable flag. When set, allows a capture or reload to occur as a result of a negative transition on T2EX if Timer 2 is not being used to clock the serial port. EXEN2 = 0 causes Timer 2 to ignore events at T2EX.							
TR2	T2CON.2	Start/stop control for Timer 2. A logic 1 starts the timer.							
C/T2	T2CON.1	Timer or counter select. (Timer 2) 0 = Internal timer (OSC/12) 1 = External event counter (falling edge triggered).							
CP/RL2	T2CON.0	Capture/Reload flag. When set, captures will occur on negative transitions at T2EX if EXEN2 = 1. When cleared, auto-reloads will occur either with Timer 2 overflows or negative transitions at T2EX when EXEN2 = 1. When either RCLK = 1 or TCLK = 1, this bit is ignored and the timer is forced to auto-reload on Timer 2 overflow.							

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Figure 1. Timer/Counter 2 (T2CON) Control Register

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Table 2. Timer 2 Operating Modes

RCLK + TCLK	CP/RL2	TR2	MODE
0	0	1	16-bit Auto-reload
0	1	1	16-bit Capture
1	X	1	Baud rate generator
X	X	0	(off)

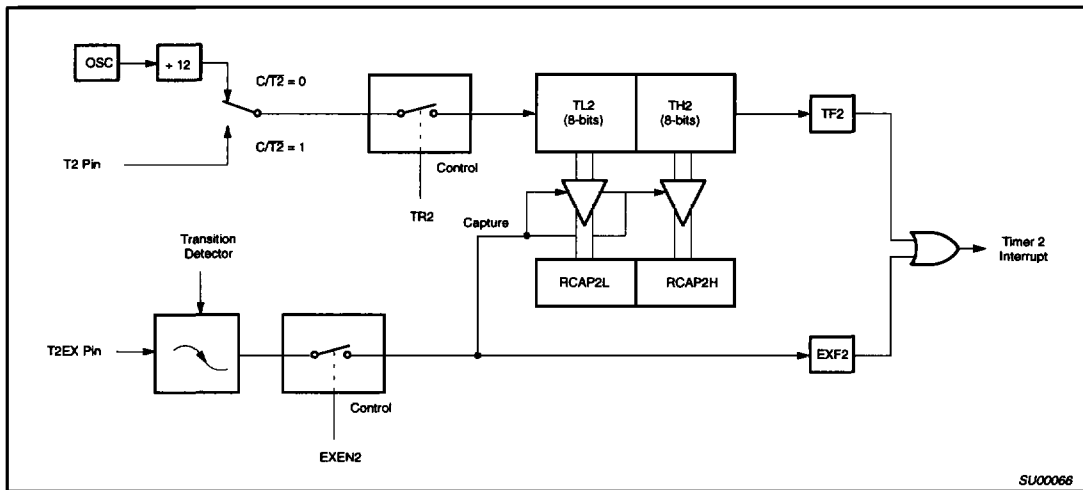


Figure 2. Timer 2 in Capture Mode

T2MOD Address = 0C9H Reset Value = XXXX XX00B

Not Bit Addressable

—	—	—	—	—	—	T2OE	DCEN
Bit 7	6	5	4	3	2	1	0

Symbol	Function
—	Not implemented, reserved for future use.*
T2OE	Timer 2 Output Enable bit. See details in Programmable Clock-Out.
DCEN	Down Count Enable bit. When set, this allows Timer 2 to be configured as an up/down counter.

* User software should not write 1s to reserved bits. These bits may be used in future 8051 family products to invoke new features. In that case, the reset or inactive value of the new bit will be 0, and its active value will be 1. The value read from a reserved bit is indeterminate.

Figure 3. Timer 2 Mode (T2MOD) Control Register

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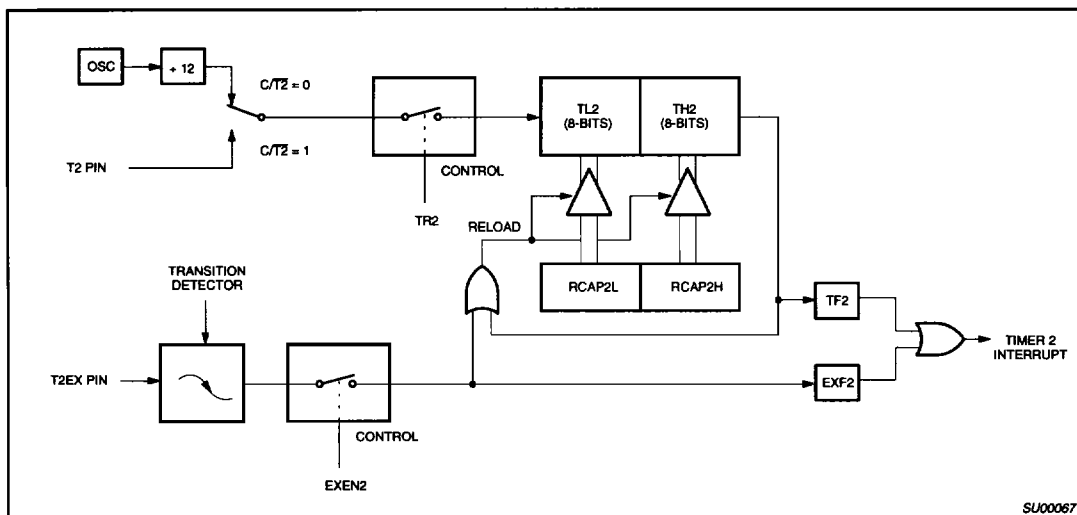


Figure 4. Timer 2 in Auto-Reload Mode (DCEN = 0)

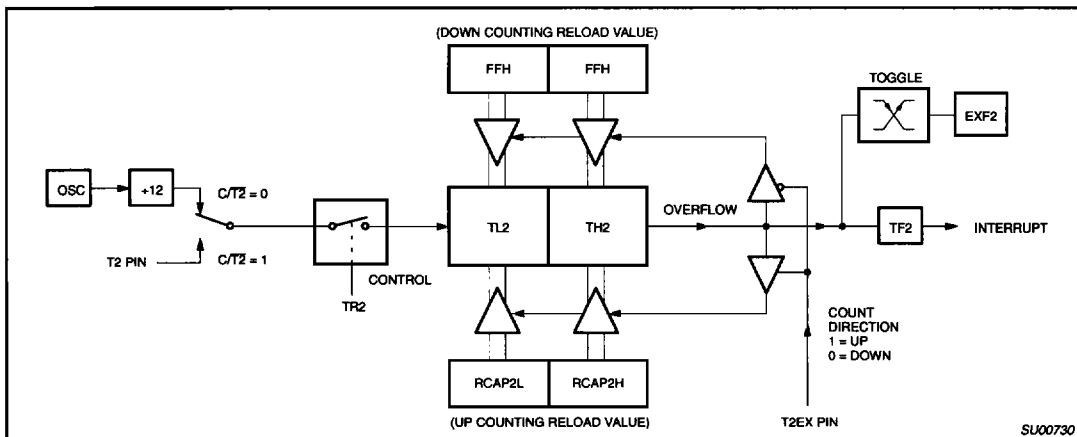


Figure 5. Timer 2 Auto Reload Mode (DCEN = 1)

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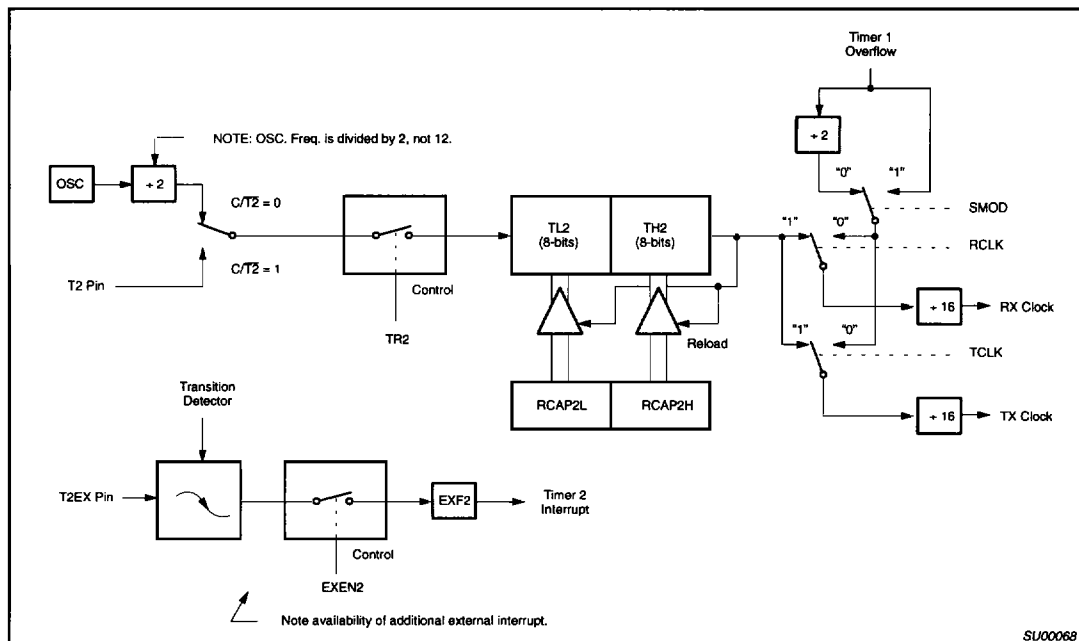


Figure 6. Timer 2 in Baud Rate Generator Mode

Table 3. Timer 2 Generated Commonly Used Baud Rates

Baud Rate	Osc Freq	Timer 2	
		RCAP2H	RCAP2L
375K	12MHz	FF	FF
9.6K	12MHz	FF	D9
2.8K	12MHz	FF	B2
2.4K	12MHz	FF	64
1.2K	12MHz	FE	C8
300	12MHz	FB	1E
110	12MHz	F2	AF
300	6MHz	FD	8F
110	6MHz	F9	57

Baud Rate Generator Mode

Bits TCLK and/or RCLK in T2CON (Table 2) allow the serial port transmit and receive baud rates to be derived from either Timer 1 or Timer 2. When TCLK= 0, Timer 1 is used as the serial port transmit baud rate generator. When TCLK= 1, Timer 2 is used as the serial port transmit baud rate generator. RCLK has the same effect for the serial port receive baud rate. With these two bits, the serial port can have different receive and transmit baud rates – one generated by Timer 1, the other by Timer 2.

Figure 6 shows the Timer 2 in baud rate generation mode. The baud rate generation mode is like the auto-reload mode, in that a rollover in TH2 causes the Timer 2 registers to be reloaded with the 16-bit value in registers RCAP2H and RCAP2L, which are preset by software.

The baud rates in modes 1 and 3 are determined by Timer 2's overflow rate given below:

$$\text{Modes 1 and 3 Baud Rates} = \frac{\text{Timer 2 Overflow Rate}}{16}$$

The timer can be configured for either "timer" or "counter" operation. In many applications, it is configured for "timer" operation (C/T2=0). Timer operation is different for Timer 2 when it is being used as a baud rate generator.

Usually, as a timer it would increment every machine cycle (i.e., 1/12 the oscillator frequency). As a baud rate generator, it increments every state time (i.e., 1/2 the oscillator frequency). Thus the baud rate formula is as follows:

$$\text{Modes 1 and 3 Baud Rates} = \frac{\text{Oscillator Frequency}}{[32 \times [65536 - (\text{RCAP2H}, \text{RCAP2L})]]}$$

Where: (RCAP2H, RCAP2L)= The content of RCAP2H and RCAP2L taken as a 16-bit unsigned integer.

The Timer 2 as a baud rate generator mode shown in Figure 6, is valid only if RCLK and/or TCLK = 1 in T2CON register. Note that a rollover in TH2 does not set TF2, and will not generate an interrupt. Thus, the Timer 2 interrupt does not have to be disabled when Timer 2 is in the baud rate generator mode. Also if the EXEN2 (T2 external enable flag) is set, a 1-to-0 transition in T2EX (Timer/counter 2 trigger input) will set EXF2 (T2 external flag) but will not cause a reload from (RCAP2H, RCAP2L) to (TH2, TL2). Therefore when Timer 2 is in use as a baud rate generator, T2EX can be used as an additional external interrupt, if needed.

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When Timer 2 is in the baud rate generator mode, one should not try to read or write TH2 and TL2. As a baud rate generator, Timer 2 is incremented every state time ($t_{osc}/2$) or asynchronously from pin T2; under these conditions, a read or write of TH2 or TL2 may not be accurate. The RCAP2 registers may be read, but should not be written to, because a write might overlap a reload and cause write and/or reload errors. The timer should be turned off (clear TR2) before accessing the Timer 2 or RCAP2 registers.

Table 3 shows commonly used baud rates and how they can be obtained from Timer 2.

Summary of Baud Rate Equations

Timer 2 is in baud rate generating mode. If Timer 2 is being clocked through pin T2(P1.0) the baud rate is:

$$\text{Baud Rate} = \frac{\text{Timer 2 Overflow Rate}}{16}$$

If Timer 2 is being clocked internally, the baud rate is:

$$\text{Baud Rate} = \frac{f_{osc}}{[32 \times [65536 - (RCAP2H, RCAP2L)]]}$$

Where f_{osc} = Oscillator Frequency

To obtain the reload value for RCAP2H and RCAP2L, the above equation can be rewritten as:

$$RCAP2H, RCAP2L = 65536 - \left(\frac{f_{osc}}{32 \times \text{Baud Rate}} \right)$$

Timer/Counter 2 Set-up

Except for the baud rate generator mode, the values given for T2CON do not include the setting of the TR2 bit. Therefore, bit TR2 must be set, separately, to turn the timer on. see Table 4 for set-up of Timer 2 as a timer. Also see Table 5 for set-up of Timer 2 as a counter.

POWER OFF FLAG³

The Power Off Flag (POF) is set by on-chip circuitry when the V_{CC} level on the 80C54/80C58 rises from 0 to 5V. The POF bit can be set or cleared by software allowing a user to determine if the reset is the result of a power-on or a warm start after powerdown. The V_{CC} level must remain above 3V for the POF to remain unaffected by the V_{CC} level.

Table 4. Timer 2 as a Timer

MODE	T2CON	
	INTERNAL CONTROL (Note 1)	EXTERNAL CONTROL (Note 2)
16-bit Auto-Reload	00H	08H
16-bit Capture	01H	09H
Baud rate generator receive and transmit same baud rate	34H	36H
Receive only	24H	26H
Transmit only	14H	16H

Table 5. Timer 2 as a Counter

MODE	TMOD	
	INTERNAL CONTROL (Note 1)	EXTERNAL CONTROL (Note 2)
16-bit	02H	0AH
Auto-Reload	03H	0BH

NOTES:

1. Capture/reload occurs only on timer/counter overflow.
2. Capture/reload occurs on timer/counter overflow and a 1-to-0 transition on T2EX (P1.1) pin except when Timer 2 is used in the baud rate generator mode.
3. POF not present in 80C52.

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OSCILLATOR CHARACTERISTICS

XTAL1 and XTAL2 are the input and output, respectively, of an inverting amplifier. The pins can be configured for use as an on-chip oscillator.

To drive the device from an external clock source, XTAL1 should be driven while XTAL2 is left unconnected. There are no requirements on the duty cycle of the external clock signal, because the input to the internal clock circuitry is through a divide-by-two flip-flop. However, minimum and maximum high and low times specified in the data sheet must be observed.

Reset

A reset is accomplished by holding the RST pin high for at least two machine cycles (24 oscillator periods), while the oscillator is running. To insure a good power-on reset, the RST pin must be high long enough to allow the oscillator time to start up (normally a few milliseconds) plus two machine cycles. At power-on, the voltage on V_{CC} and RST must come up at the same time for a proper start-up. Ports 1, 2, and 3 will asynchronously be driven to their reset condition when a voltage above V_{IH1} (min.) is applied to RESET.

Idle Mode

In the idle mode (see Table 6), the CPU puts itself to sleep while all of the on-chip peripherals stay active. The instruction to invoke the idle mode is the last instruction executed in the normal operating mode before the idle mode is activated. The CPU contents, the on-chip RAM, and all of the special function registers remain intact during this mode. The idle mode can be terminated either by any enabled interrupt (at which time the process is picked up at the interrupt service routine and continued), or by a hardware reset which starts the processor in the same manner as a power-on reset.

Power-Down Mode

To save even more power, a Power Down mode (see Table 6) can be invoked by software. In this mode, the oscillator is stopped and the instruction that invoked Power Down is the last instruction executed. The on-chip RAM and Special Function Registers retain their values until the Power Down mode is terminated.

On the 80C52/54/58 either a hardware reset or external interrupt can be used to exit from Power Down. Reset redefines all the SFRs but does not change the on-chip RAM. An external interrupt allows both the SFRs and the on-chip RAM to retain their values.

To properly terminate Power Down the reset or external interrupt should not be executed before V_{CC} is restored to its normal operating level and must be held active long enough for the oscillator to restart and stabilize (normally less than 10ms).

With an external interrupt, INT0 and INT1 must be enabled and configured as level-sensitive. Holding the pin low restarts the

oscillator but bringing the pin back high completes the exit. Once the interrupt is serviced, the next instruction to be executed after RETI will be the one following the instruction that put the device into Power Down.

Design Consideration

- When the idle mode is terminated by a hardware reset, the device normally resumes program execution, from where it left off, up to two machine cycles before the internal reset algorithm takes control. On-chip hardware inhibits access to internal RAM in this event, but access to the port pins is not inhibited. To eliminate the possibility of an unexpected write when Idle is terminated by reset, the instruction following the one that invokes Idle should not be one that writes to a port pin or to external memory.

ONCE™ Mode

The ONCE ("On-Circuit Emulation") Mode facilitates testing and debugging of systems using the 80C52/54/58 without removing the device from the circuit. The ONCE Mode is invoked by:

- Pull ALE low while the device is in reset and PSEN is high;
- Hold ALE low as RST is deactivated.

While the device is in ONCE Mode, the Port 0 pins go into a float state, and the other port pins and ALE and PSEN are weakly pulled high. The oscillator circuit remains active. While the 80C52/54/58 is in this mode, an emulator or test CPU can be used to drive the circuit. Normal operation is restored when a normal reset is applied.

Programmable Clock-Out

The 80C52/54/58 has a new feature. A 50% duty cycle clock can be programmed to come out on P1.0. This pin, besides being a regular I/O pin, has two alternate functions. It can be programmed:

- to input the external clock for Timer/Counter 2, or
- to output a 50% duty cycle clock ranging from 61Hz to 4MHz at a 16MHz operating frequency.

To configure the Timer/Counter 2 as a clock generator, bit C/T2 (in T2CON) must be cleared and bit T2OE in T2MOD must be set. Bit TR2 (T2CON.2) also must be set to start the timer.

The Clock-Out frequency depends on the oscillator frequency and the reload value of Timer 2 capture registers (RCAP2H, RCAP2L) as shown in this equation:

$$\frac{\text{Oscillator Frequency}}{4 \times (65536 - \text{RCAP2H, RCAP2L})}$$

In the Clock-Out mode Timer 2 roll-overs will not generate an interrupt. This is similar to when it is used as a baud-rate generator. It is possible to use Timer 2 as a baud-rate generator and a clock generator simultaneously. Note, however, that the baud-rate and the Clock-Out frequency will be the same.

Table 6. External Pin Status During Idle and Power-Down Mode

MODE	PROGRAM MEMORY	ALE	PSEN	PORT 0	PORT 1	PORT 2	PORT 3
Idle	Internal	1	1	Data	Data	Data	Data
Idle	External	1	1	Float	Data	Address	Data
Power-down	Internal	0	0	Data	Data	Data	Data
Power-down	External	0	0	Float	Data	Data	Data

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Enhanced UART

The UART operates in all of the usual modes that are described in the first section of *Data Handbook IC20, 80C51-Based 8-Bit Microcontrollers*. In addition the UART can perform framing error detect by looking for missing stop bits, and automatic address recognition. The 80C52/54/58 UART also fully supports *multi-processor communication as does the standard 80C51 UART*.

When used for framing error detect the UART looks for missing stop bits in the communication. A missing bit will set the FE bit in the SCON register. The FE bit shares the SCON.7 bit with SM0 and the function of SCON.7 is determined by PCON.6 (SMOD0) (see Figure 7). If SMOD0 is set then SCON.7 functions as FE. SCON.7 functions as SM0 when SMOD0 is cleared. When used as FE SCON.7 can only be cleared by software. Refer to Figure 8.

Automatic Address Recognition

Automatic Address Recognition is a feature which allows the UART to recognize certain addresses in the serial bit stream by using hardware to make the comparisons. This feature saves a great deal of software overhead by eliminating the need for the software to examine every serial address which passes by the serial port. This feature is enabled by setting the SM2 bit in SCON. In the 9 bit UART modes, mode 2 and mode 3, the Receive Interrupt flag (RI) will be automatically set when the received byte contains either the "Given" address or the "Broadcast" address. The 9 bit mode requires that the 9th information bit is a 1 to indicate that the received information is an address and not data. Automatic address recognition is shown in Figure 9.

The 8 bit mode is called Mode 1. In this mode the RI flag will be set if SM2 is enabled and the information received has a valid stop bit following the 8 address bits and the information is either a Given or Broadcast address.

Mode 0 is the Shift Register mode and SM2 is ignored.

Using the Automatic Address Recognition feature allows a master to selectively communicate with one or more slaves by invoking the Given slave address or addresses. All of the slaves may be contacted by using the Broadcast address. Two special Function Registers are used to define the slave's address, SADDR, and the address mask, SADEN. SADEN is used to define which bits in the SADDR are to be used and which bits are "don't care". The SADEN mask can be logically ANDed with the SADDR to create the "Given" address which the master will use for addressing each of the slaves. Use of the Given address allows multiple slaves to be recognized while excluding others. The following examples will help to show the versatility of this scheme:

Slave 0	SADDR =	1100 0000
	SADEN =	<u>1111 1101</u>
	Given =	1100 00X0

Slave 1	SADDR =	1100 0000
	SADEN =	<u>1111 1110</u>
	Given =	1100 00X0

In the above example SADDR is the same and the SADEN data is used to differentiate between the two slaves. Slave 0 requires a 0 in bit 0 and it ignores bit 1. Slave 1 requires a 0 in bit 1 and bit 0 is ignored. A unique address for Slave 0 would be 1100 0010 since slave 1 requires a 0 in bit 1. A unique address for slave 1 would be 1100 0001 since a 1 in bit 0 will exclude slave 0. Both slaves can be selected at the same time by an address which has bit 0 = 0 (for slave 0) and bit 1 = 0 (for slave 1). Thus, both could be addressed with 1100 0000.

In a more complex system the following could be used to select slaves 1 and 2 while excluding slave 0:

Slave 0	SADDR =	1100 0000
	SADEN =	<u>1111 1001</u>
	Given =	1100 0XX0
Slave 1	SADDR =	1110 0000
	SADEN =	<u>1111 1010</u>
	Given =	1110 0X0X
Slave 2	SADDR =	1110 0000
	SADEN =	<u>1111 1100</u>
	Given =	1110 00XX

In the above example the differentiation among the 3 slaves is in the lower 3 address bits. Slave 0 requires that bit 0 = 0 and it can be uniquely addressed by 1110 0110. Slave 1 requires that bit 1 = 0 and it can be uniquely addressed by 1110 and 0101. Slave 2 requires that bit 2 = 0 and its unique address is 1110 0011. To select Slaves 0 and 1 and exclude Slave 2 use address 1110 0100, since it is necessary to make bit 2 = 1 to exclude slave 2.

The Broadcast Address for each slave is created by taking the logical OR of SADDR and SADEN. Zeros in this result are treated as don't-cares. In most cases, interpreting the don't-cares as ones, the broadcast address will be FF hexadecimal.

Upon reset SADDR (SFR address 0A9H) and SADEN (SFR address 0B9H) are loaded with 0s. This produces a given address of all "don't cares" as well as a Broadcast address of all "don't cares". This effectively disables the Automatic Addressing mode and allows the microcontroller to use standard 80C51 type UART drivers which do not make use of this feature.

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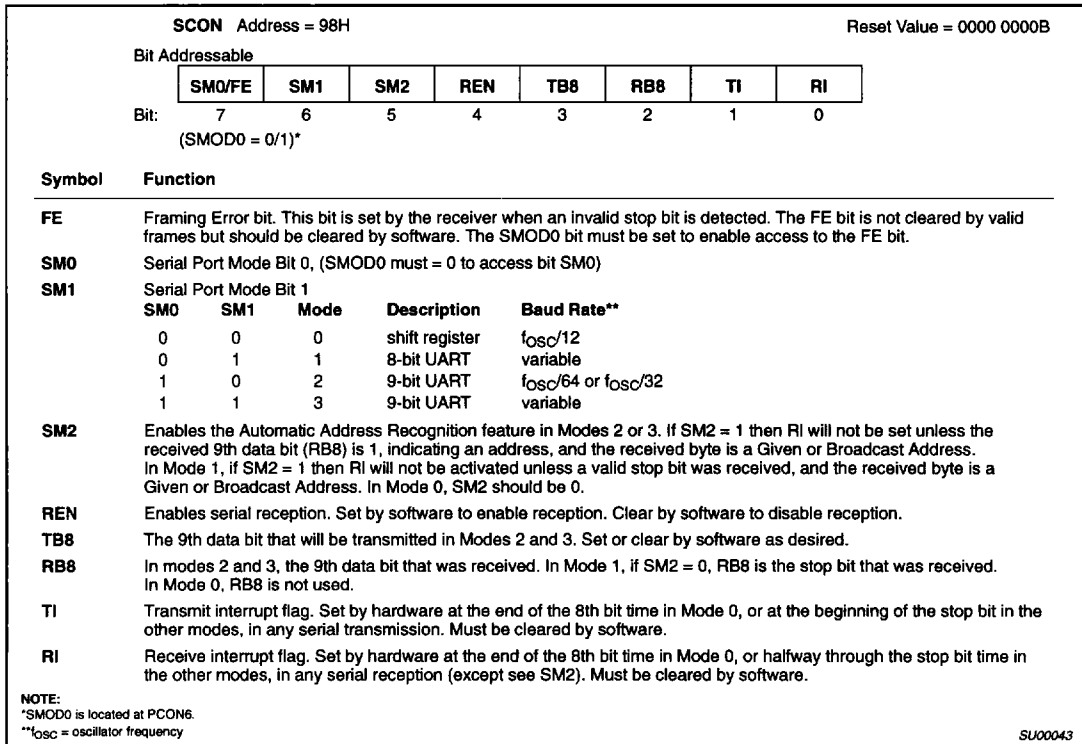


Figure 7. SCON: Serial Port Control Register

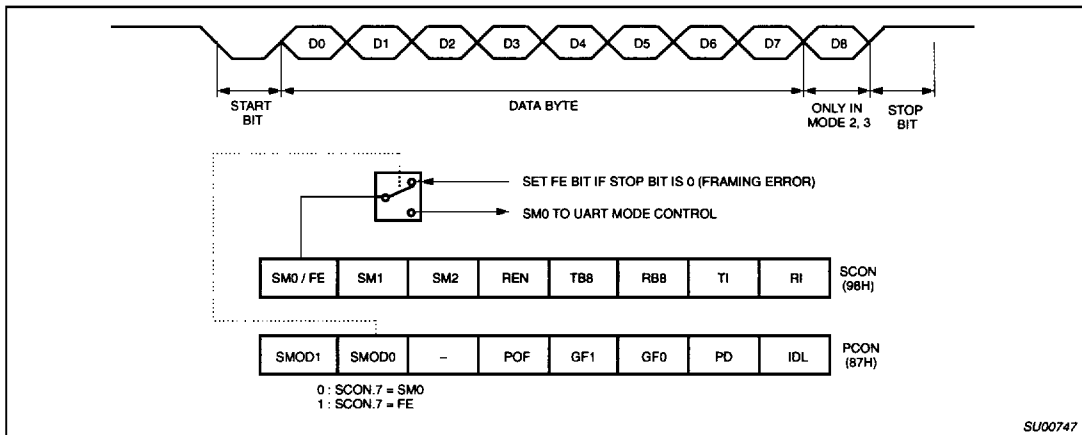


Figure 8. UART Framing Error Detection

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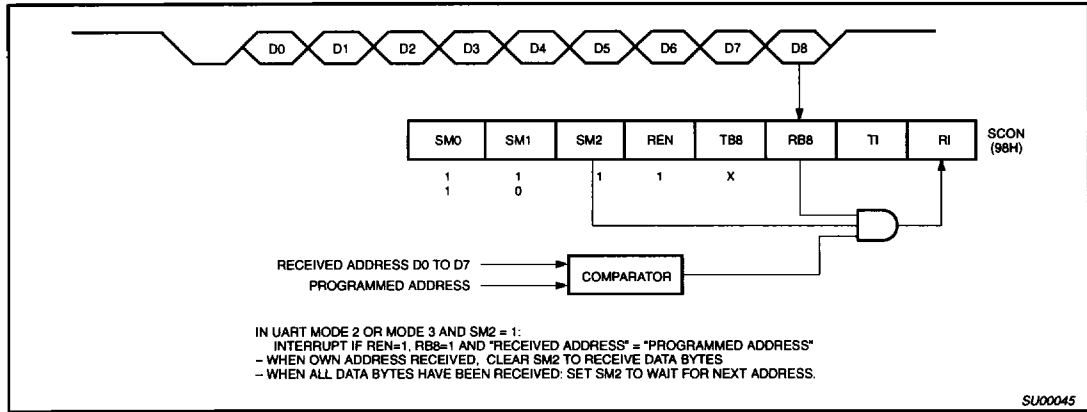


Figure 9. UART Multiprocessor Communication, Automatic Address Recognition

Interrupt Priority Structure

The 80C52/54/58 has a 6-source four-level interrupt structure. There are 3 SFRs associated with the interrupts on the 80C52/54/58. They are the IE and IP. (See Figures 10 and 11.) In addition, there is the IPH (Interrupt Priority High) register that makes the four-level interrupt structure possible. The IPH is located at SFR address B7H. The structure of the IPH register and a description of its bits is shown below:

IPH (Interrupt Priority High) (B7H)

7	6	5	4	3	2	1	0
-	-	PT2H	PSH	PT1H	PX1H	PT0H	PX0H

- IPH.0 PX0H External interrupt 0 priority high
- IPH.1 PT0H Timer 0 interrupt priority high
- IPH.2 PX1H External interrupt 1 priority high
- IPH.3 PT1H Timer 1 interrupt priority high
- IPH.4 PSH Serial Port interrupt high
- IPH.5 PT2H Timer 2 interrupt priority high
- IPH.6 — Not implemented
- IPH.7 — Not implemented

The function of the IPH SFR is simple and when combined with the IP SFR determines the priority of each interrupt. The priority of each interrupt is determined as shown in the following table:

PRIORITY BITS		INTERRUPT PRIORITY LEVEL
IPH.x	IP.x	
0	0	Level 0 (lowest priority)
0	1	Level 1
1	0	Level 2
1	1	Level 3 (highest priority)

The priority scheme for servicing the interrupts is the same as that for the 80C51, except there are four interrupt levels on the 80C52/54/58 rather than two as on the 80C51. An interrupt will be serviced as long as an interrupt of equal or higher priority is not already being serviced. If an interrupt of equal or higher level priority is being serviced, the new interrupt will wait until it is finished before being serviced. If a lower priority level interrupt is being serviced, it will be stopped and the new interrupt serviced. When the new interrupt is finished, the lower priority level interrupt that was stopped will be completed.

Table 7. Interrupt Table

SOURCE	POLLING PRIORITY	REQUEST BITS	HARDWARE CLEAR?	VECTOR ADDRESS
X0	1	IE0	N (L) ¹ Y (T) ²	03H
T0	2	TP0	Y	0BH
X1	3	IE1	N (L) Y (T)	13H
T1	4	TF1	Y	1BH
SP	5	R1, T1	N	23H
T2	6	TF2, EXF2	N	2BH
PCA	7	CF, CCFn n = 0-4	N	33H

NOTES:

- 1. L = Level activated
- 2. T = Transition activated

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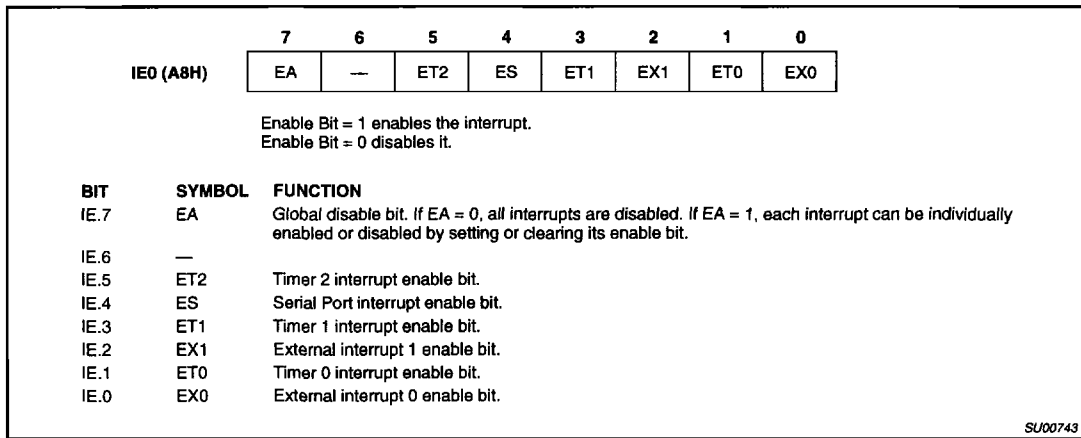


Figure 10. IE Registers

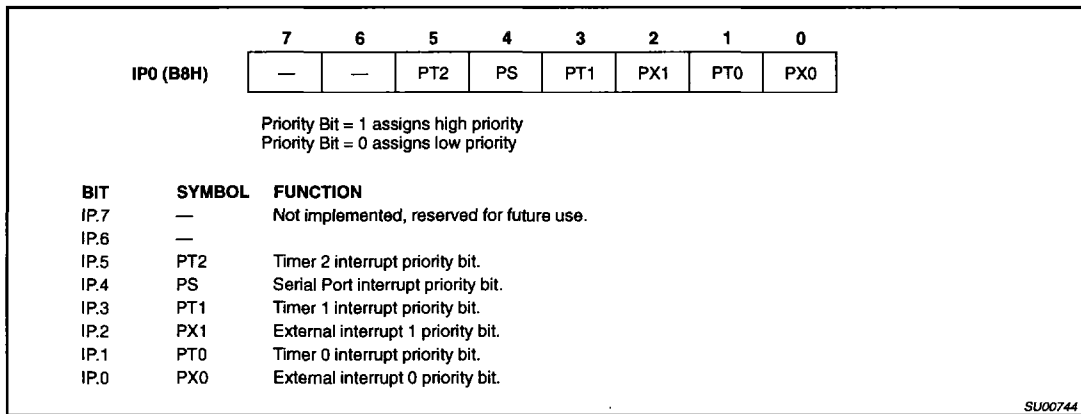


Figure 11. IP Registers

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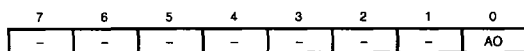
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Reduced EMI Mode

The AO bit (AUXR.0) in the AUXR register when set disables the ALE output.

80C52/80C54/80C58 Reduced EMI Mode

AUXR (8EH)

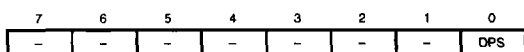


AO: Turns off ALE output.

Dual Data Pointer Register (DPTR)

The dual DPTR structure (see Figure 12) is a way by which the 80C52/54/58 will specify the address of an external data memory location. There are two 16-bit DPTR registers that address the external memory, and a single bit called DPS = AUXR1/bit0 that allows the program code to switch between them.

- Register Name: AUXR1#
- SFR Address: A2H
- Reset Value: xxxxxx0B



Where:

DPS = AUXR1/bit0 = Switches between DPTR0 and DPTR1.

Select Reg	DPS
DPTR0	0
DPTR1	1

The DPS bit status should be saved by software when switching between DPTR0 and DPTR1.

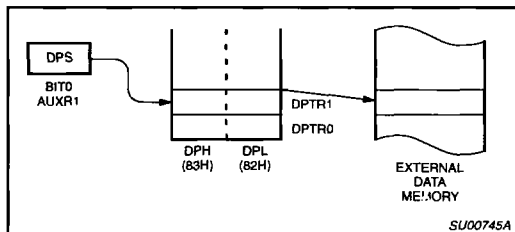


Figure 12. DPTR Structure

DPTR Instructions

The instructions that refer to DPTR refer to the data pointer that is currently selected using the AUXR1/bit 0 register. The six instructions that use the DPTR are as follows:

INC DPTR	DPTR	Increments the data pointer by 1
MOV DPTR, #data16	DPTR	Loads the DPTR with a 16-bit constant
MOV A, @ A+DPTR	DPTR	Move code byte relative to DPTR to ACC
MOVX A, @ DPTR	DPTR	Move external RAM (16-bit address) to ACC
MOVX @ DPTR, A	DPTR	Move ACC to external RAM (16-bit address)
JMP @ A + DPTR	DPTR	Jump indirect relative to DPTR

The data pointer can be accessed on a byte-by-byte basis by specifying the Low or High byte in an instruction which accesses the SFRs. See application note AN458 for detailed operation

ABSOLUTE MAXIMUM RATINGS^{1, 2, 3}

PARAMETER	RATING	UNIT
Operating temperature under bias	0 to +70 or -40 to +85	°C
Storage temperature range	-65 to +150	°C
Voltage on EA/V _{PP} pin to V _{SS}	0 to +13.0	V
Voltage on any other pin to V _{SS}	-0.5 to +6.5	V
Maximum I _{OL} per I/O pin	15	mA
Power dissipation (based on package heat transfer limitations, not device power consumption)	1.5	W

NOTES:

1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any conditions other than those described in the AC and DC Electrical Characteristics section of this specification is not implied.
2. This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying greater than the rated maxima.
3. Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to V_{SS} unless otherwise noted.

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DC ELECTRICAL CHARACTERISTICS

 $T_{amb} = 0^{\circ}\text{C}$ to $+70^{\circ}\text{C}$ or -40°C to $+85^{\circ}\text{C}$, $V_{CC} = 5.0\text{V} \pm 10\%$; $V_{SS} = 0\text{V}$

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP ¹	MAX	
V_{IL}	Input low voltage	$4.5\text{V} < V_{CC} < 5.5\text{V}$	-0.5		$0.2V_{CC}-0.1$	V
V_{IH}	Input high voltage (ports 0, 1, 2, 3, EA)		$0.2V_{CC}+0.9$		$V_{CC}+0.5$	V
V_{IH1}	Input high voltage, XTAL1, RST		$0.7V_{CC}$		$V_{CC}+0.5$	V
V_{OL}	Output low voltage, ports 1, 2, 3 ⁸	$V_{CC} = 4.5\text{V}$ $I_{OL} = 1.6\text{mA}^2$			0.4	V
V_{OL1}	Output low voltage, port 0, ALE, PSEN ^{8, 7}	$V_{CC} = 4.5\text{V}$ $I_{OL} = 3.2\text{mA}^2$			0.4	V
V_{OH}	Output high voltage, ports 1, 2, 3 ³	$V_{CC} = 4.5\text{V}$ $I_{OH} = -30\mu\text{A}$	$V_{CC} - 0.7$			V
V_{OH1}	Output high voltage (port 0 in external bus mode), ALE ⁹ , PSEN ³	$V_{CC} = 4.5\text{V}$ $I_{OH} = -3.2\text{mA}$	$V_{CC} - 0.7$			V
I_{IL}	Logical 0 input current, ports 1, 2, 3	$V_{IN} = 0.4\text{V}$	-1		-50	μA
I_{TL}	Logical 1-to-0 transition current, ports 1, 2, 3 ⁶	$V_{IN} = 2.0\text{V}$ See note 4			-650	μA
I_{LI}	Input leakage current, port 0	$0.45 < V_{IN} < V_{CC} - 0.3$			± 10	μA
I_{CC}	Power supply current (see Figure 20): Active mode @ 16MHz ⁵ Idle mode @ 16MHz ⁵ Power-down mode	See note 5 $T_{amb} = 0$ to $+70^{\circ}\text{C}$ $T_{amb} = -40$ to $+85^{\circ}\text{C}$		3	16 4 50 75	mA mA μA μA
R_{RST}	Internal reset pull-down resistor		40		225	k Ω
C_{IO}	Pin capacitance ¹⁰ (except EA)				15	pF

NOTES:

- Typical ratings are not guaranteed. The values listed are at room temperature, 5V.
- Capacitive loading on ports 0 and 2 may cause spurious noise to be superimposed on the V_{OL} s of ALE and ports 1 and 3. The noise is due to external bus capacitance discharging into the port 0 and port 2 pins when these pins make 1-to-0 transitions during bus operations. In the worst cases (capacitive loading > 100pF), the noise pulse on the ALE pin may exceed 0.8V. In such cases, it may be desirable to qualify ALE with a Schmitt Trigger, or use an address latch with a Schmitt Trigger STROBE input. I_{OL} can exceed these conditions provided that no single output sinks more than 5mA and no more than two outputs exceed the test conditions.
- Capacitive loading on ports 0 and 2 may cause the V_{OH} on ALE and PSEN to momentarily fall below the ($V_{CC}-0.7$) specification when the address bits are stabilizing.
- Pins of ports 1, 2 and 3 source a transition current when they are being externally driven from 1 to 0. The transition current reaches its maximum value when V_{IN} is approximately 2V.
- See Figures 21 through 24 for I_{CC} test conditions.
Active Mode: $I_{CC} = 0.9 \times \text{FREQ} + 1.1$;
Idle Mode: $I_{CC} = 0.18 \times \text{FREQ} + 1.0$; See Figure 20.
- This value applies to $T_{amb} = 0^{\circ}\text{C}$ to $+70^{\circ}\text{C}$. For $T_{amb} = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $I_{TL} = -750\mu\text{A}$.
- Load capacitance for port 0, ALE, and PSEN = 100pF, load capacitance for all other outputs = 80pF.
- Under steady state (non-transient) conditions, I_{OL} must be externally limited as follows:
Maximum I_{OL} per port pin: 15mA (*NOTE: This is 85°C specification.)
Maximum I_{OL} per 8-bit port: 26mA
Maximum total I_{OL} for all outputs: 71mA
If I_{OL} exceeds the test condition, V_{OL} may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.
- ALE is tested to V_{OH1} , except when ALE is off then V_{OH} is the voltage specification.
- Pin capacitance is characterized but not tested. Pin capacitance is less than 25pF. Pin capacitance of ceramic package is less than 15pF (except EA it is 25pF).

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AC ELECTRICAL CHARACTERISTICS

T_{amb} = 0°C to +70°C or -40°C to +85°C, V_{CC} = 5V ±10%, V_{SS} = 0V^{1, 2, 3}

SYMBOL	FIGURE	PARAMETER	16MHz CLOCK		VARIABLE CLOCK		UNIT
			MIN	MAX	MIN	MAX	
t _{CLCL}	13	Oscillator frequency Speed versions : E			3.5	16	MHz
t _{LHLL}	13	ALE pulse width	85		2t _{CLCL} -40		ns
t _{AVLL}	13	Address valid to ALE low	22		t _{CLCL} -40		ns
t _{LLAX}	13	Address hold after ALE low	32		t _{CLCL} -30		ns
t _{LLIV}	13	ALE low to valid instruction in		150		4t _{CLCL} -100	ns
t _{LLPL}	13	ALE low to PSEN low	32		t _{CLCL} -30		ns
t _{PLPH}	13	PSEN pulse width	142		3t _{CLCL} -45		ns
t _{PLIV}	13	PSEN low to valid instruction in ⁴		82		3t _{CLCL} -105	ns
t _{PIX}	13	Input instruction hold after PSEN	0		0		ns
t _{PIXZ}	13	Input instruction float after PSEN		37		t _{CLCL} -25	ns
t _{AVIV}	13	Address to valid instruction in ⁴		207		5t _{CLCL} -105	ns
t _{PLAZ}	13	PSEN low to address float		10		10	ns
Data Memory							
t _{RLRH}	14, 15	RD pulse width	275		6t _{CLCL} -100		ns
t _{WLWH}	14, 15	WR pulse width	275		6t _{CLCL} -100		ns
t _{RLDV}	14, 15	RD low to valid data in		147		5t _{CLCL} -165	ns
t _{RHDX}	14, 15	Data hold after RD	0		0		ns
t _{RHDZ}	14, 15	Data float after RD		65		2t _{CLCL} -60	ns
t _{LLDV}	14, 15	ALE low to valid data in		350		8t _{CLCL} -150	ns
t _{AVDV}	14, 15	Address to valid data in		397		9t _{CLCL} -165	ns
t _{LLWL}	14, 15	ALE low to RD or WR low	137	239	3t _{CLCL} -50	3t _{CLCL} +50	ns
t _{AVWL}	14, 15	Address valid to WR low or RD low	122		4t _{CLCL} -130		ns
t _{QVWX}	14, 15	Data valid to WR transition	13		t _{CLCL} -50		ns
t _{WHQX}	14, 15	Data hold after WR	13		t _{CLCL} -50		ns
t _{QVWH}	15	Data valid to WR high	287		7t _{CLCL} -150		ns
t _{RLAZ}	14, 15	RD low to address float		0		0	ns
t _{WHLH}	14, 15	RD or WR high to ALE high	23	103	t _{CLCL} -40	t _{CLCL} +40	ns
External Clock							
t _{CHCX}	17	High time	20		20	t _{CLCL} -t _{CLCX}	ns
t _{CLCX}	17	Low time	20		20	t _{CLCL} -t _{CHCX}	ns
t _{CLCH}	17	Rise time		20		20	ns
t _{CHCL}	17	Fall time		20		20	ns
Shift Register							
t _{XLXL}	16	Serial port clock cycle time	750		12t _{CLCL}		ns
t _{QVXH}	16	Output data setup to clock rising edge	492		10t _{CLCL} -133		ns
t _{XHQX}	16	Output data hold after clock rising edge	8		2t _{CLCL} -117		ns
t _{XHDX}	16	Input data hold after clock rising edge	0		0		ns
t _{XHDV}	16	Clock rising edge to input data valid		492		10t _{CLCL} -133	ns

NOTES:

- Parameters are valid over operating temperature range unless otherwise specified.
- Load capacitance for port 0, ALE, and PSEN = 100pF, load capacitance for all other outputs = 80pF.
- Interfacing the 80C52/54/58 to devices with float times up to 45ns is permitted. This limited bus contention will not cause damage to Port 0 drivers.
- See application note AN457 for external memory interfacing.

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AC ELECTRICAL CHARACTERISTICS
 $T_{amb} = 0^{\circ}\text{C}$ to $+70^{\circ}\text{C}$ or -40°C to $+85^{\circ}\text{C}$, $V_{CC} = 5\text{V} \pm 10\%$, $V_{SS} = 0\text{V}^{1,2,3}$

SYMBOL	FIGURE	PARAMETER	24MHz CLOCK		VARIABLE CLOCK ⁴		33MHz CLOCK		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f_{CLCL}	13	Oscillator frequency Speed versions : I (24MHz) : N (33MHz)	3.5	24	3.5	33	3.5	33	MHz
t_{LHLL}	13	ALE pulse width	43		$2t_{\text{CLCL}}-40$		21		ns
t_{AVLL}	13	Address valid to ALE low	17		$t_{\text{CLCL}}-25$		5		ns
t_{LLAX}	13	Address hold after ALE low	17		$t_{\text{CLCL}}-25$				ns
t_{LLIV}	13	ALE low to valid instruction in		102		$4t_{\text{CLCL}}-65$		55	ns
t_{LLPL}	13	ALE low to PSEN low	17		$t_{\text{CLCL}}-25$		5		ns
t_{PLPH}	13	PSEN pulse width	80		$3t_{\text{CLCL}}-45$		45		ns
t_{PLIV}	13	PSEN low to valid instruction in		65		$3t_{\text{CLCL}}-60$		30	ns
t_{PXIX}	13	Input instruction hold after PSEN	0		0		0		ns
t_{PXIZ}	13	Input instruction float after PSEN		17		$t_{\text{CLCL}}-25$		5	ns
t_{AVIV}	13	Address to valid instruction in		128		$5t_{\text{CLCL}}-80$		70	ns
t_{PLAZ}	13	PSEN low to address float		10		10		10	ns
Data Memory									
t_{RLRH}	14, 15	RD pulse width	150		$6t_{\text{CLCL}}-100$		82		ns
t_{WLWH}	14, 15	WR pulse width	150		$6t_{\text{CLCL}}-100$		82		ns
t_{RLDV}	14, 15	RD low to valid data in		118		$5t_{\text{CLCL}}-90$		60	ns
t_{RHDX}	14, 15	Data hold after RD	0		0		0		ns
t_{RHDX}	14, 15	Data float after RD		55		$2t_{\text{CLCL}}-28$		32	ns
t_{LLDV}	14, 15	ALE low to valid data in		183		$8t_{\text{CLCL}}-150$		90	ns
t_{AVDV}	14, 15	Address to valid data in		210		$9t_{\text{CLCL}}-165$		105	ns
t_{LLWL}	14, 15	ALE low to RD or WR low	75	175	$3t_{\text{CLCL}}-50$	$3t_{\text{CLCL}}+50$	40	140	ns
t_{AVWL}	14, 15	Address valid to WR low or RD low	92		$4t_{\text{CLCL}}-75$		45		ns
t_{QVWX}	14, 15	Data valid to WR transition	12		$t_{\text{CLCL}}-30$		0		ns
t_{WHQX}	14, 15	Data hold after WR	17		$t_{\text{CLCL}}-25$		5		ns
t_{QVWH}	15	Data valid to WR high	162		$7t_{\text{CLCL}}-130$		80		ns
t_{RLAZ}	14, 15	RD low to address float		0		0		0	ns
t_{WHLH}	14, 15	RD or WR high to ALE high	17	67	$t_{\text{CLCL}}-25$	$t_{\text{CLCL}}+25$	5	55	ns
External Clock									
t_{CHCX}	17	High time	17		17	$t_{\text{CLCL}}-t_{\text{CLCX}}$			ns
t_{CLCX}	17	Low time	17		17	$t_{\text{CLCL}}-t_{\text{CHCX}}$			ns
t_{CLCH}	17	Rise time		5		5			ns
t_{CHCL}	17	Fall time		5		5			ns
Shift Register									
t_{XLXL}	16	Serial port clock cycle time	505		$12t_{\text{CLCL}}$		360		ns
t_{QVXH}	16	Output data setup to clock rising edge	283		$10t_{\text{CLCL}}-133$		167		ns
t_{XHDX}	16	Output data hold after clock rising edge	3		$2t_{\text{CLCL}}-80$				ns
t_{XHDX}	16	Input data hold after clock rising edge	0		0		0		ns
t_{XHDX}	16	Clock rising edge to input data valid		283		$10t_{\text{CLCL}}-133$		167	ns

NOTES:

- Parameters are valid over operating temperature range unless otherwise specified.
- Load capacitance for port 0, ALE, and PSEN = 100pF, load capacitance for all other outputs = 80pF.
- Interfacing the 80C52/54/58 to devices with float times up to 45ns is permitted. This limited bus contention will not cause damage to Port 0 drivers.
- Variable clock is specified for oscillator frequencies greater than 16MHz to 33MHz. For frequencies equal or less than 16MHz, see 16MHz "AC Electrical Characteristics", page 3-206.

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EXPLANATION OF THE AC SYMBOLS

Each timing symbol has five characters. The first character is always 't' (= time). The other characters, depending on their positions, indicate the name of a signal or the logical status of that signal. The designations are:

- A – Address
- C – Clock
- D – Input data
- H – Logic level high
- I – Instruction (program memory contents)
- L – Logic level low, or ALE

- P – PSEN
- Q – Output data
- R – RD signal
- t – Time
- V – Valid
- W – WR signal
- X – No longer a valid logic level
- Z – Float

Examples: t_{AVLL} = Time for address valid to ALE low.
 t_{LLPL} = Time for ALE low to PSEN low.

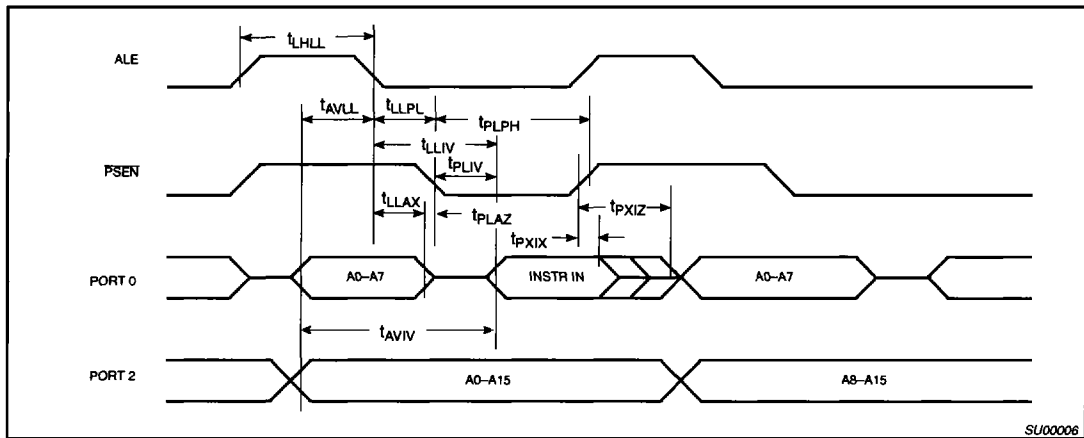


Figure 13. External Program Memory Read Cycle

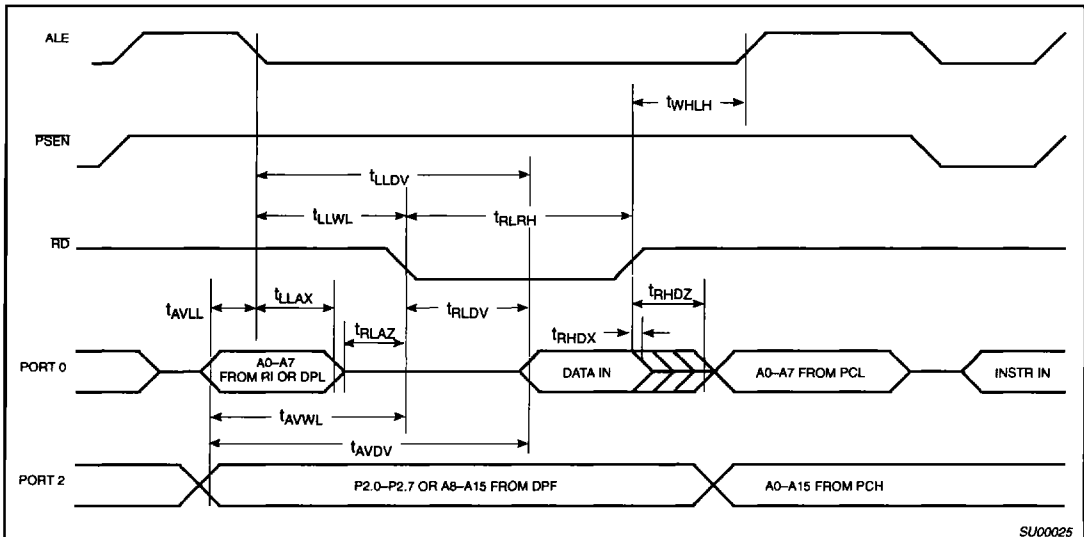


Figure 14. External Data Memory Read Cycle

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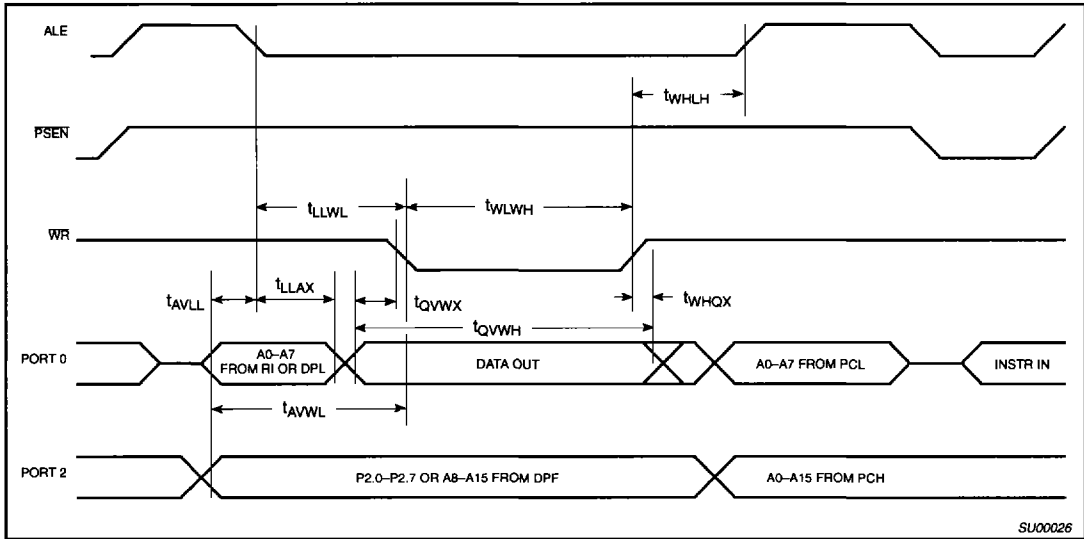


Figure 15. External Data Memory Write Cycle

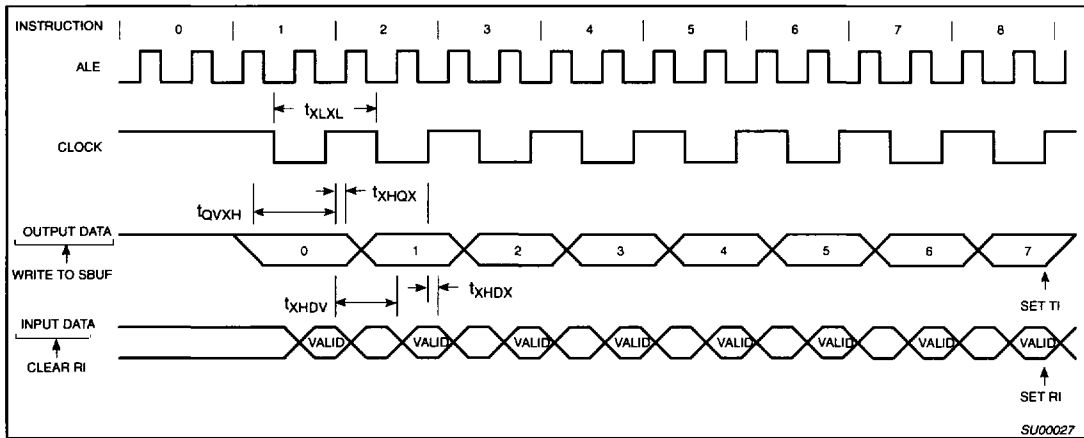


Figure 16. Shift Register Mode Timing

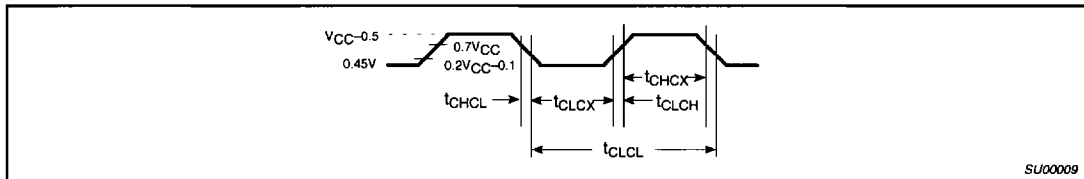


Figure 17. External Clock Drive

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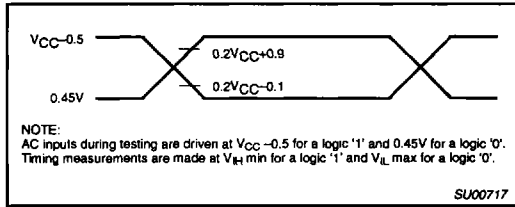


Figure 18. AC Testing Input/Output

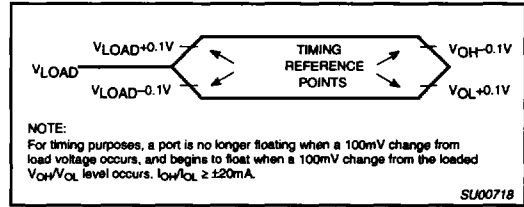


Figure 19. Float Waveform

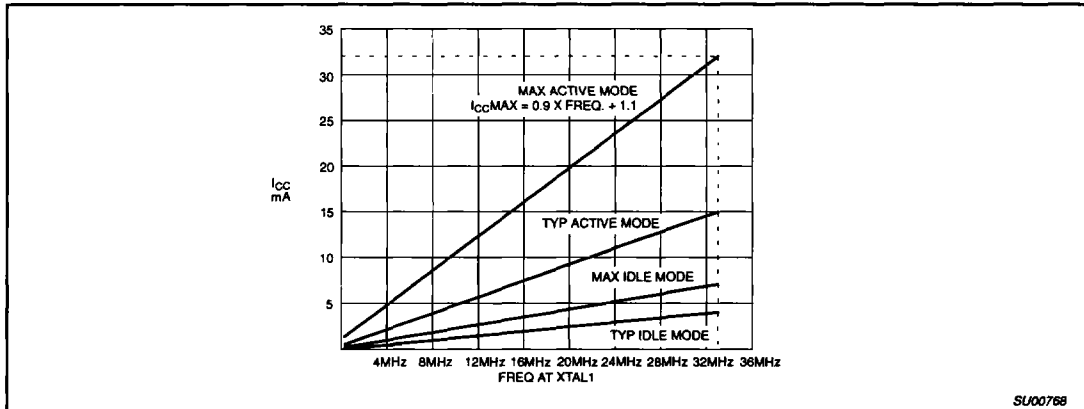


Figure 20. I_{CC} vs. FREQ
Valid only within frequency specifications of the device under test

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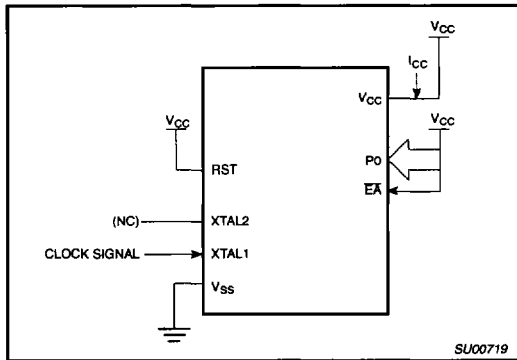


Figure 21. I_{CC} Test Condition, Active Mode
All other pins are disconnected

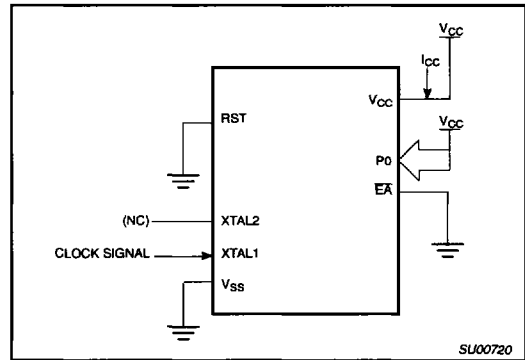


Figure 22. I_{CC} Test Condition, Idle Mode
All other pins are disconnected

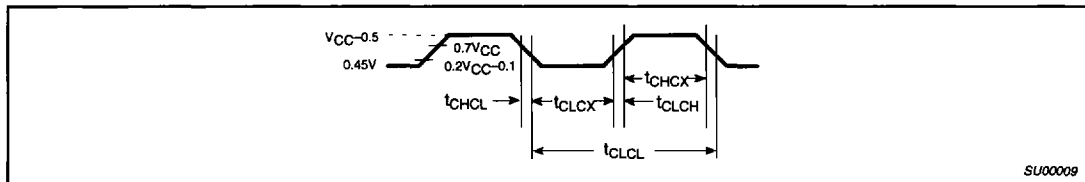


Figure 23. Clock Signal Waveform for I_{CC} Tests in Active and Idle Modes
 $t_{CLCH} = t_{CHCL} = 5\text{ns}$

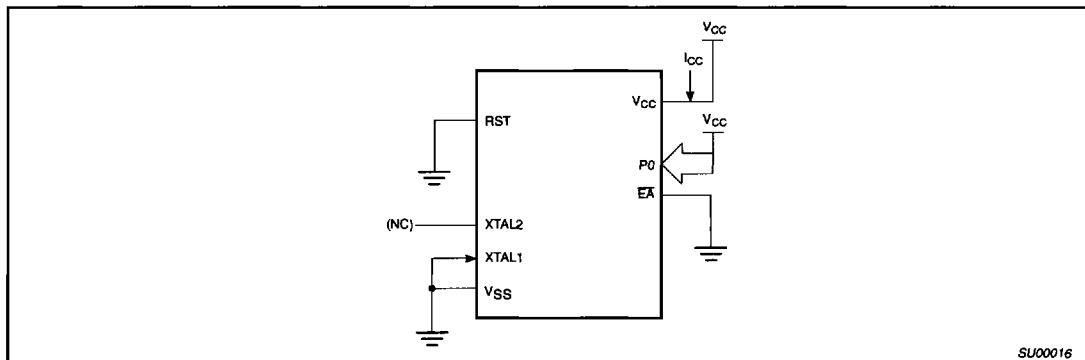


Figure 24. I_{CC} Test Condition, Power Down Mode
All other pins are disconnected. $V_{CC} = 2\text{V to } 5.5\text{V}$

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Security Bits

With none of the security bits programmed the code in the program memory can be verified. If the encryption table is programmed, the code will be encrypted when verified. When only security bit 1 (see Table 8) is programmed, MOVC instructions executed from external program memory are disabled from fetching code bytes from the

internal memory, \overline{EA} is latched on Reset and all further programming of the EPROM is disabled. When security bits 1 and 2 are programmed, in addition to the above, verify mode is disabled.

Encryption Array

64 bytes of encryption array are initially unprogrammed (all 1s).

Table 8. Program Security Bits

PROGRAM LOCK BITS ^{1, 2}			PROTECTION DESCRIPTION
	SB1	SB2	
1	U	U	No Program Security features enabled. (Code verify will still be encrypted by the Encryption Array if programmed.)
2	P	U	MOVC instructions executed from external program memory are disabled from fetching code bytes from internal memory, \overline{EA} is sampled and latched on Reset, and further programming of the EPROM is disabled.

NOTES:

1. P – programmed. U – unprogrammed.
2. Any other combination of the security bits is not defined.

80C52 ROM CODE SUBMISSION

When submitting ROM code for the 80C52, the following must be specified:

1. 8k byte user ROM data
2. 64 byte ROM encryption key
3. ROM security bits.

ADDRESS	CONTENT	BIT(S)	COMMENT
0000H to 1FFFH	DATA	7:0	User ROM Data
2000H to 201FH	KEY	7:0	ROM Encryption Key FFH = no encryption
2020H	SEC	0	ROM Security Bit 1 0 = enable security 1 = disable security
2020H	SEC	1	ROM Security Bit 2 0 = enable security 1 = disable security

Security Bit 1: When programmed, this bit has two effects on masked ROM parts:

1. External MOVC is disabled, and
2. \overline{EA} is latched on Reset.

Security Bit 2: When programmed, this bit inhibits Verify User ROM.

If the ROM Code file does not include the options, the following information must be included with the ROM code.

For each of the following, check the appropriate box, and send to Philips along with the code:

- Security Bit #1: Enabled Disabled
- Security Bit #2: Enabled Disabled
- Encryption: No Yes If Yes, must send key file.

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80C54 ROM CODE SUBMISSION

When submitting ROM code for the 80C54, the following must be specified:

1. 16k byte user ROM data
2. 64 byte ROM encryption key
3. ROM security bits.

ADDRESS	CONTENT	BIT(S)	COMMENT
0000H to 3FFFH	DATA	7:0	User ROM Data
4000H to 401FH	KEY	7:0	ROM Encryption Key FFH = no encryption
4020H	SEC	0	ROM Security Bit 1 0 = enable security 1 = disable security
4020H	SEC	1	ROM Security Bit 2 0 = enable security 1 = disable security

Security Bit 1: When programmed, this bit has two effects on masked ROM parts:

1. External MOV_C is disabled, and
2. EA is latched on Reset.

Security Bit 2: When programmed, this bit inhibits Verify User ROM.

If the ROM Code file does not include the options, the following information must be included with the ROM code.

For each of the following, check the appropriate box, and send to Philips along with the code:

- Security Bit #1: Enabled Disabled
- Security Bit #2: Enabled Disabled
- Encryption: No Yes If Yes, must send key file.

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80C58 ROM CODE SUBMISSION

When submitting ROM code for the 80C58, the following must be specified:

1. 32k byte user ROM data
2. 64 byte ROM encryption key
3. ROM security bits.

If submitting a file, the format is as follows:

ADDRESS	CONTENT	BIT(S)	COMMENT
0000H to 7FFFH	DATA	7:0	User ROM Data
8000H to 801FH	KEY	7:0	ROM Encryption Key FFH = no encryption
8020H	SEC	0	ROM Security Bit 1 0 = enable security 1 = disable security
8020H	SEC	1	ROM Security Bit 2 0 = enable security 1 = disable security

Security Bit 1: When programmed, this bit has two effects on masked ROM parts:

1. External MOVC is disabled, and
2. EA is latched on Reset.

Security Bit 2: When programmed, this bit inhibits Verify User ROM.

If the ROM code file does not include the options, the following information must be included with the ROM code.

For each of the following check the appropriate box and send to Philips along with the code:

- Security Bit #1: Enabled Disabled
- Security Bit #2: Enabled Disabled
- Encryption: No Yes If Yes, must send key file.