Signetics

74LS764
DRAM Controller

DRAM Dual-Ported Controller
Product Specification

Logic Products

FEATURES

- **Allows two microprocessors to access the same bank of DRAM**
- **Replaces 25 TTL devices to perform arbitration, signal timing, multiplexing, and refresh generation**
- **9 address output pins allow control of up to 256K DRAMS**
- **Separate refresh clock allows adjustable refresh timing**
- **On-board 18-bit address input latch**
- **30MHz Maximum Clock rate**

DESCRIPTION

The 74LS764 DRAM Dual-Ported Controller is a high speed, clocked dual port arbiter and timing generator that allows two microprocessors, microcontrollers, or any other memory accessing devices to share the same block of memory. The device performs arbitration, signal timing, address multiplexing and refresh, replacing up to 25 discrete TTL devices.

The 'LS764 contains an on-board 18-bit address input latch which latches the address inputs at the start of an access cycle.

The device is available in a 40-pin plastic DIP or 44 pin PLCC with pinouts designed to allow convenient placement of microprocessors, DRAMs, and other support chips.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74LS764	45ns	215mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V ±5%; T_A = 0°C to +70°C
Plastic DIP	N74LS764N
PLCC-44	N74LS764A

NOTE:
For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74LS
$\overline{REQ}_1$, $\overline{REQ}_2$	Request inputs (active LOW)	1LSUL
CP	Clock input	1LSUL
RCP	Refresh clock input	1LSUL
A1 – A18	Address inputs	1LSUL
GNT	Grant output	60LSUL
$\overline{SEL}_1$, $\overline{SEL}_2$	Select outputs (active LOW)	60LSUL
DTACK	Data transfer acknowledge output	60LSUL
$\overline{RAS}$	Row address strobe (output active LOW)	60LSUL
WG	Write gate output	60LSUL
$\overline{CASEN}$	Column address strobe enable output (active LOW)	60LSUL
MA0 – MA8	Address outputs	60LSUL

NOTE:
One 74LS Unit Load (LSUL) is defined as: 20μA in the HIGH state and 0.4mA in the LOW state.

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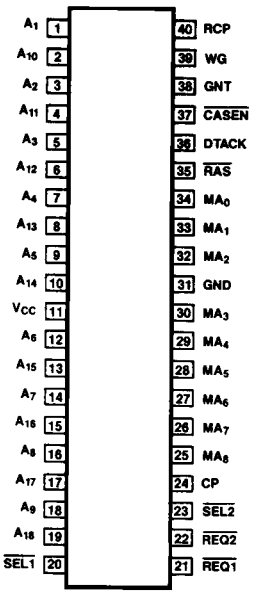
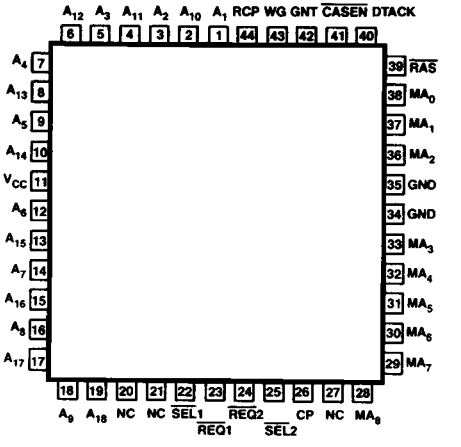
DRAM Controller

74LS764

PIN CONFIGURATION

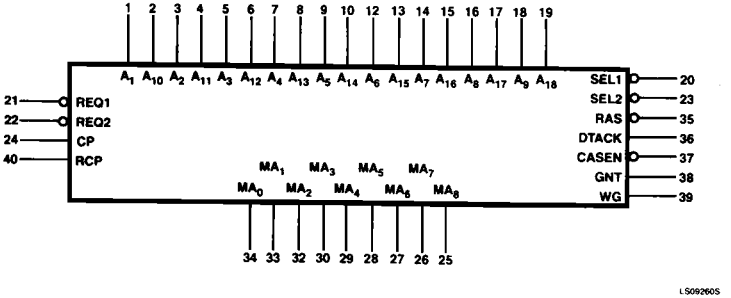


CD07460S



CD07450S

LOGIC SYMBOL



LS09260S

PIN DESCRIPTION

SYMBOL	PINS		TYPE	NAME AND FUNCTION
	DIP	PLCC		
A1	1	1	I	Address inputs used to generate memory row address.
A2	3	3	I	
A3	5	5	I	
A4	7	7	I	
A5	9	9	I	
A6	11	12	I	
A7	13	14	I	
A8	15	16	I	
A9	17	18	I	
A10	2	2	I	Address inputs used to generate memory column address.
A11	4	4	I	
A12	6	6	I	
A13	8	8	I	
A14	10	10	I	
A15	12	13	I	
A16	14	15	I	
A17	16	17	I	
A18	18	19	I	
$\overline{REQ_1}$	21	23	I	Memory access request from microprocessor one.
$\overline{REQ_2}$	22	24	I	Memory access request from microprocessor two.
CP	24	26	I	Clock input which determines the master timing and arbitration rates.
RCP	40	44	I	Refresh Clock determines the period of refresh for each row after it is internally divided by 64.
$\overline{SEL_1}$	20	22	O	Select signal is activated in response to the active $\overline{REQ_1}$ input, indicating that access will be granted to microprocessor one.
V_{CC}	11	11		Power supply +5V ±5%
GND	31	34 35		Ground
$\overline{SEL_2}$	20	25	O	Select signal is activated in response to the active $\overline{REQ_2}$ input, indicating that access will be granted to microprocessor two.
MA0	34	38	O	Memory address output pins, designed to drive the address lines of a DRAM.
MA1	33	37	O	
MA2	32	36	O	
MA3	30	33	O	
MA4	29	32	O	
MA5	28	31	O	
MA6	27	30	O	
MA7	26	29	O	
MA8	25	28	O	
GNT	38	42	O	Grant output internally activated upon start of memory access cycle.
$\overline{RAS}$	35	39	O	Row address strobe is used to latch the row address into the bank of DRAM(to be connected directly to the $\overline{RAS}$ inputs of the DRAMs).
WG	39	43	O	When activated, the "Write Gate" signal from the device could be gated with the microprocessor's write strobe to perform an "Early Write".
$\overline{CASEN}$	37	41	O	Column Address Strobe Enable is used to latch the column address into the bank of DRAMs.
DTACK	36	40	O	Data Transfer Acknowledge indicates that data on the DRAM output lines is valid or the proper access time has occurred.

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ARCHITECTURE

The 'LS764 arbitration logic is divided into two stages. The first stage controls which one of the two $\overline{REQ}$ inputs will be serviced by activating the corresponding $\overline{SEL}$ output. The $\overline{SEL}$ output signals have been provided for use as look-ahead enables for 3-state address lines from each of the microprocessors connected to the address inputs of the 'LS764.

The second arbitration stage controls arbitration between the $\overline{SEL}$ signals and refresh requests. Refresh always has priority and is serviced immediately after the current cycle is completed (if needed). This arbitration stage also indicates the start of an access cycle via the GNT output signal. GNT is provided to indicate to the requesting microprocessor that its access cycle has begun. The GNT and $\overline{SEL}$ outputs can be used to generate wait states.

The 'LS764 has an 18-bit internal latch which latches the address inputs, A1 – A18, at the start of the access cycle. The latched address inputs are propagated to the MA0 – MA8 address outputs via an internal 18-bit MUX, which multiplexes the 18 address inputs to 9 row address and 9 column address signals, giving the 'LS764 the capability to interface 256K DRAMs to the masters.

The internal refresh row counter has 9 outputs, allowing the 'LS764 to refresh up to 512 row DRAMs.

The generation of $\overline{RAS}$, $\overline{CASEN}$, Write Gate (WG), and Data Transfer Acknowledge (DTACK) outputs is controlled by on chip timing logic.

FUNCTIONAL DESCRIPTION

The speed at which the 'LS764 operates is determined by the CP input, with a maximum limit of 30MHz. All internal signal timing and control is based on this input.

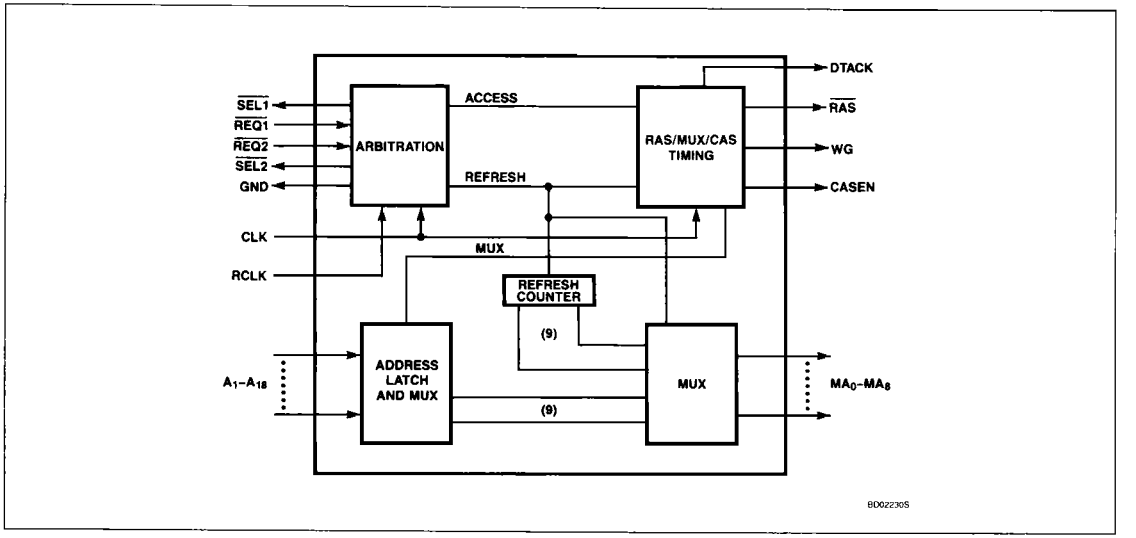
A microprocessor requests access to the DRAM by activating the appropriate $\overline{REQ}$ input. If a refresh cycle is not in process and the other request input is not active, the $\overline{SEL}$ output corresponding to the active $\overline{REQ}$ input will go LOW to indicate that access will be granted. The GNT output then goes HIGH (by the LOW-to-HIGH transition) indicating that a memory access cycle is now commencing. If an access or refresh cycle is in process, and the other microprocessor has not requested access, the $\overline{SEL}$ output corresponding to the active $\overline{REQ}$ input will go LOW to indicate that access will be granted, but GNT will not go HIGH until the current cycle is completed. After completion of current cycle, and followed by a synchronization period, GNT will automatically become active.

If access to the DRAM is requested by both microprocessors, the initial arbitration stage will determine which processor will be serviced by activating the corresponding $\overline{SEL}$ output. This arbitration takes place irrespective of whether or not a refresh cycle is in progress at the time access is requested. $\overline{REQ}$ contention is arbitrated by internal circuitry sampling the $\overline{REQ}_1$ and $\overline{REQ}_2$ inputs on different edges of the CP input: $\overline{REQ}_1$ is sampled on the rising edge of the clock and $\overline{REQ}_2$ is sampled on the falling edge of the same clock. Specially designed CTL flip-flops have been used in this circuitry to eliminate meta-stable states. Again, if a refresh cycle is in progress, the GNT output will not become active until the refresh cycle is completed.

When GNT becomes true on the 'LS764, the A1 – A18 address input signals are latched internally and the A1 – A9 signals are propagated to the MA0 – MA8 output pins. One-half clock cycle is allowed for the address signals to propagate through to the outputs, after which the $\overline{RAS}$ output is brought valid.

At the next half clock cycle, the A10 – A18 latch outputs on the 'LS764 are selected and propagated to the MA0 – MA9 outputs. The write gate (WG) output becomes valid at this time to indicate the proper time to gate the WRITE signal from the selected processor to the DRAM to perform an EARLY WRITE cycle. One-half clock cycle is again allowed for the A10 – A18 signals to propagate and stabilize. $\overline{CASEN}$ then becomes valid. $\overline{CASEN}$ can be used as a CAS output or decoded with higher-order address signals to produce multiple CAS signals. Once $\overline{CASEN}$ is valid, the controller will wait three clock cycles before negating $\overline{RAS}$, making a total $\overline{RAS}$ pulse width of 4 clock cycles. At the time $\overline{RAS}$ becomes inactive, the DTACK output becomes true to indicate that data on the DRAM data lines is valid, or that the proper access time has been met. DTACK can be used to indicate a valid data transfer acknowledge for processors requiring this signal. All controller output signals will be held in this

BLOCK DIAGRAM

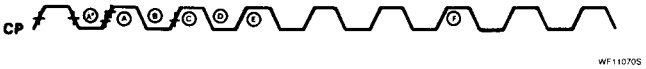


final state until the selected processor withdraws its request by driving its $\overline{REQ}$ input HIGH. When the request is withdrawn, internal synchronization takes place, the controller output signals become inactive, and any pending access or refresh cycles are serviced.

The refresh cycle commences from internally generated refresh requests. RCP is divided by 64 to produce a refresh request internally. Refresh requests are arbitrated with $\overline{SEL}$ outputs in the second stage of arbitration. Refresh always has priority and will be serviced immediately or upon completion of the current access cycle. At the start of a refresh grant, the 9 refresh counter address signals are allowed to propagate to the MA0 – MA8 outputs for one-half clock, at which time the $\overline{RAS}$ signal becomes active for 4 clock cycles, then inactive for 3 clock cycles to meet the $\overline{RAS}$ precharge requirement of the DRAMs, at which time the refresh cycle is terminated.

All signal outputs on the 'LS764 have 48mA drivers and proprietary positive edge rate controlling circuitry to reduce reflections when driving DRAMs on a PC board. The outputs are specified to handle up to 256pF without degradation of control and minimal degradation of access time, allowing any one pin to drive 32 devices (8pF load per input).

AC WAVEFORM FOR IMMEDIATE ACCESS (Sequence of events for $\overline{REQ}_1$ access when no refresh or $\overline{REQ}_2$ access)



WF11070S

A' $\overline{REQ}_2$ sampled

A $\overline{REQ}_1$ sampled
$\overline{SEL}_1$ triggered ($\overline{SEL}_1$ triggered by $\overline{REQ}_1$ sample circuitry)

B GNT triggered ($\overline{SEL}_1$ and GNT propagation paths are the same)
A1 – A18 latched (Input address latch triggered by GNT circuitry)
A1 – A9 propagate to MA outputs

C $\overline{RAS}$ triggered

D WG triggered
A10 – A18 selected and progagated to MA outputs

E $\overline{CASEN}$ triggered

F $\overline{RAS}$ negated
DTACK triggered

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SYSTEM CYCLES

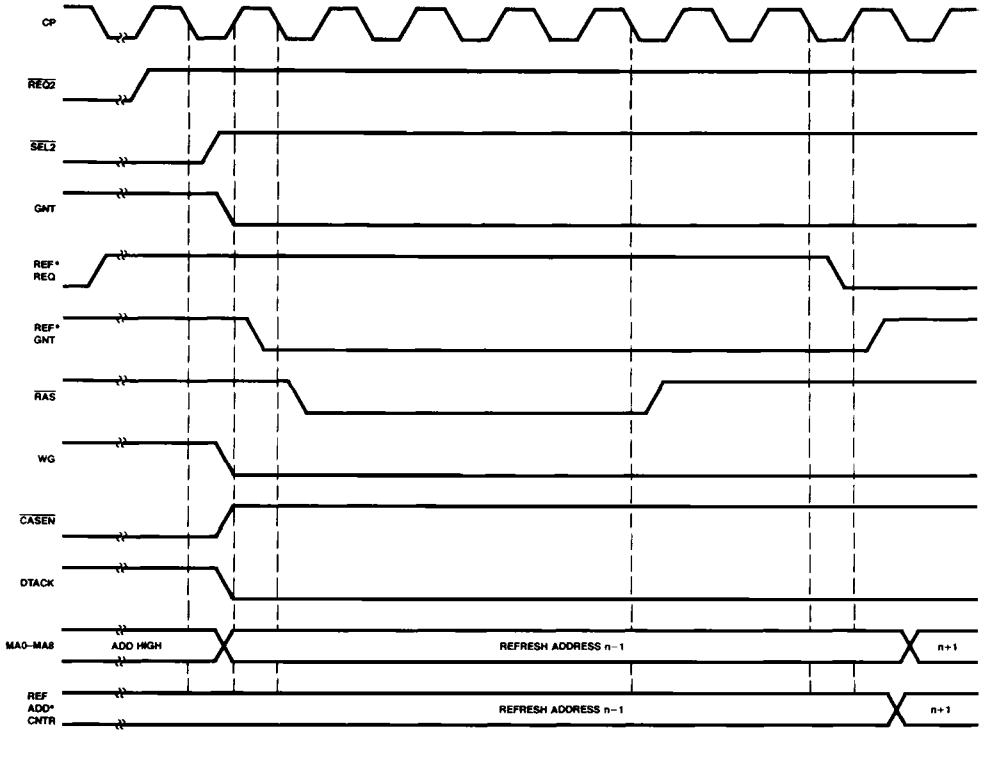
The 74LS764 is always in one of the following cycles.

A. IDLE — There is no request pending and the refresh clock has not completed 64 clock cycles since the last refresh request.

B. REFRESH — A refresh request is initiated every 64 refresh clock cycles, unless there is a refresh cycle already in progress. It is a $\overline{RAS}$ only refresh cycle, derived from the clock (CP).

C. REQUEST$_1$ — This is a memory access cycle for processor 1. It can only be initiated when there is no refresh or request 2 cycle in progress.

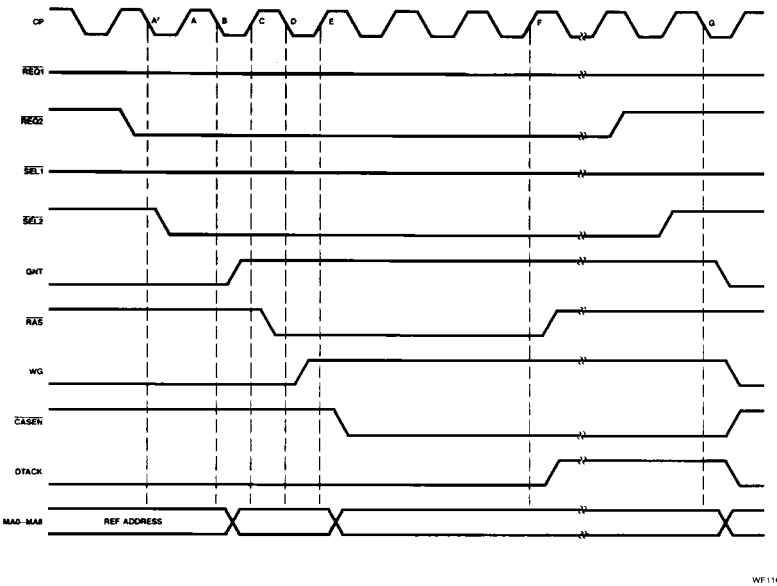
D. REQUEST$_2$ — This is a memory access cycle for processor 2. It can only be initiated when there is no refresh or request 1 cycle in progress.



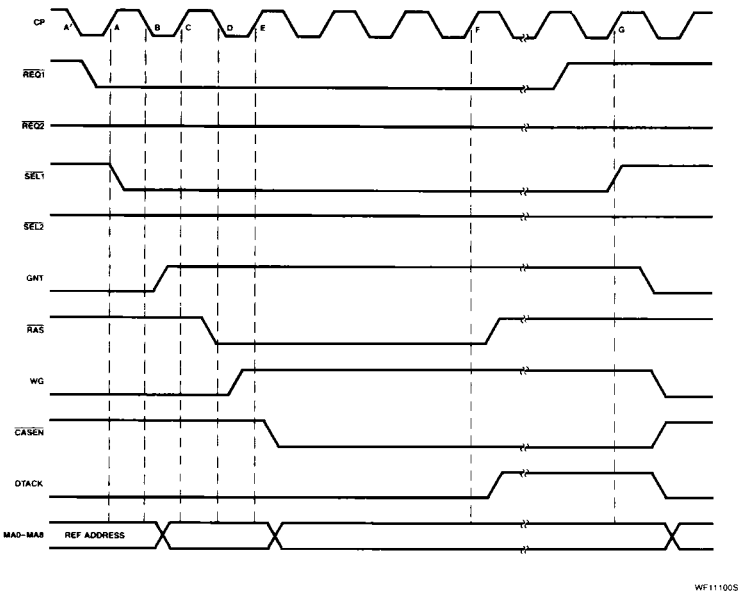
NOTE:
* These are internal signals only.

Refresh Cycle

SYSTEM CYCLES



Request 1 Cycle



Request 2 Cycle

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TYPICAL APPLICATION WITH 74LS764

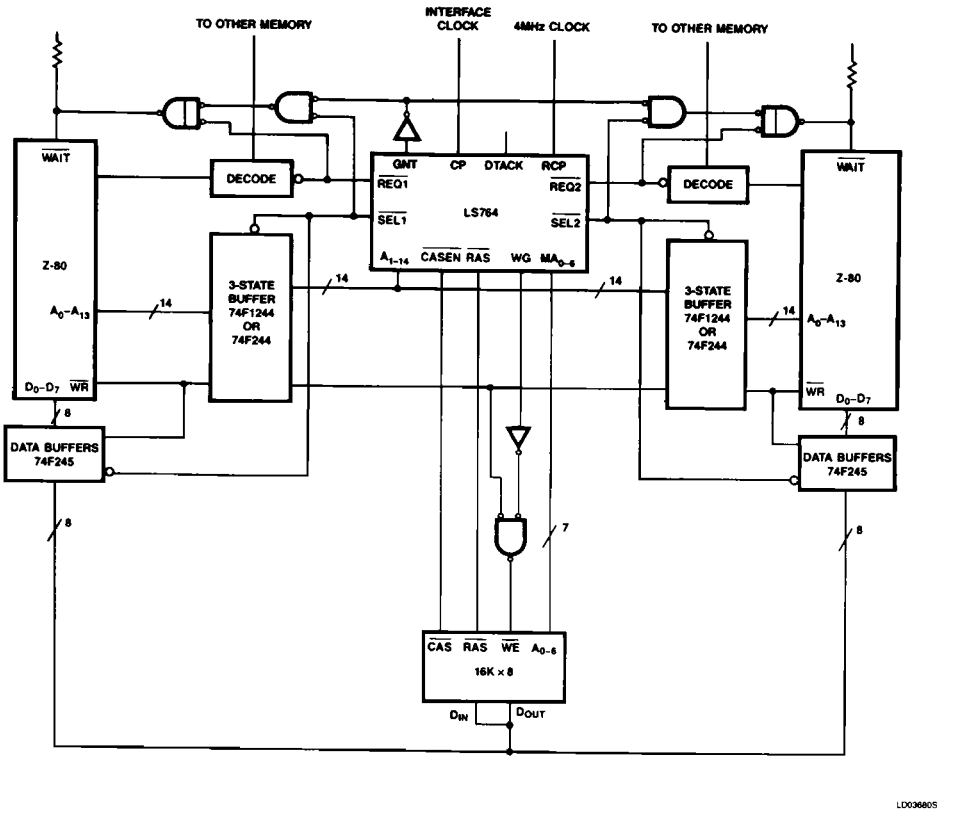

Figure 1. TWO Z-80s sharing 16K RAM

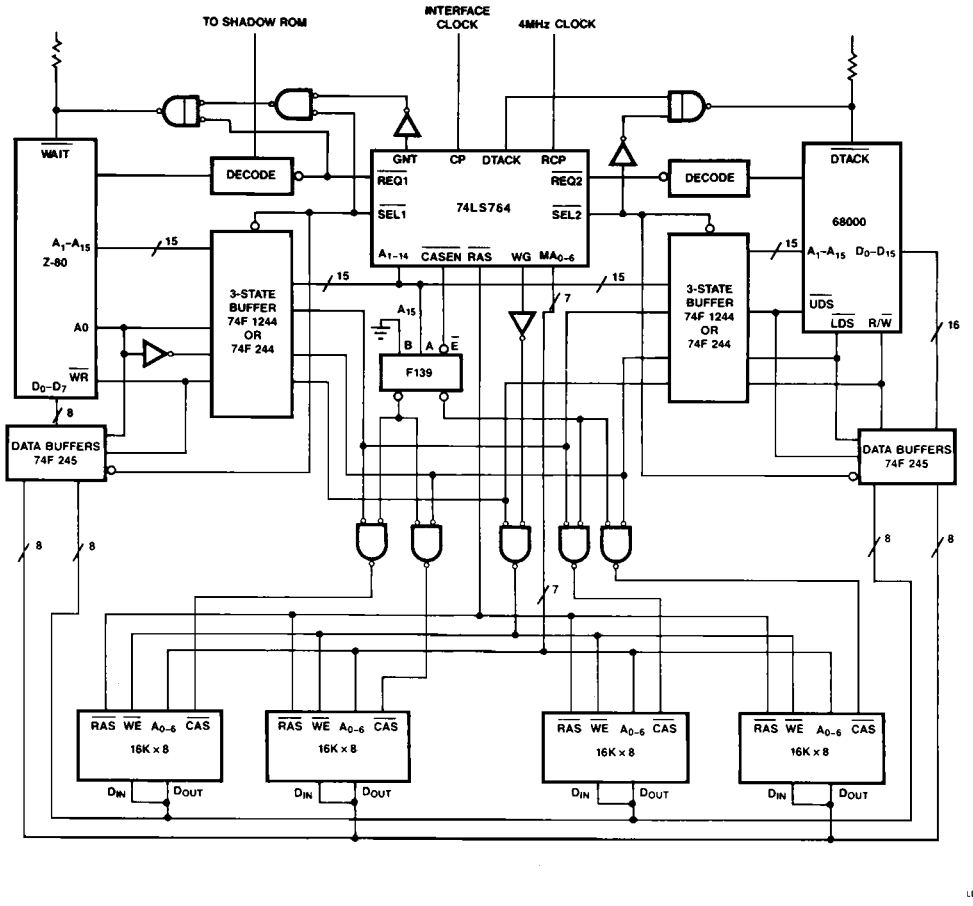

Figure 2. 68000 with Z-80 sharing 64K RAM

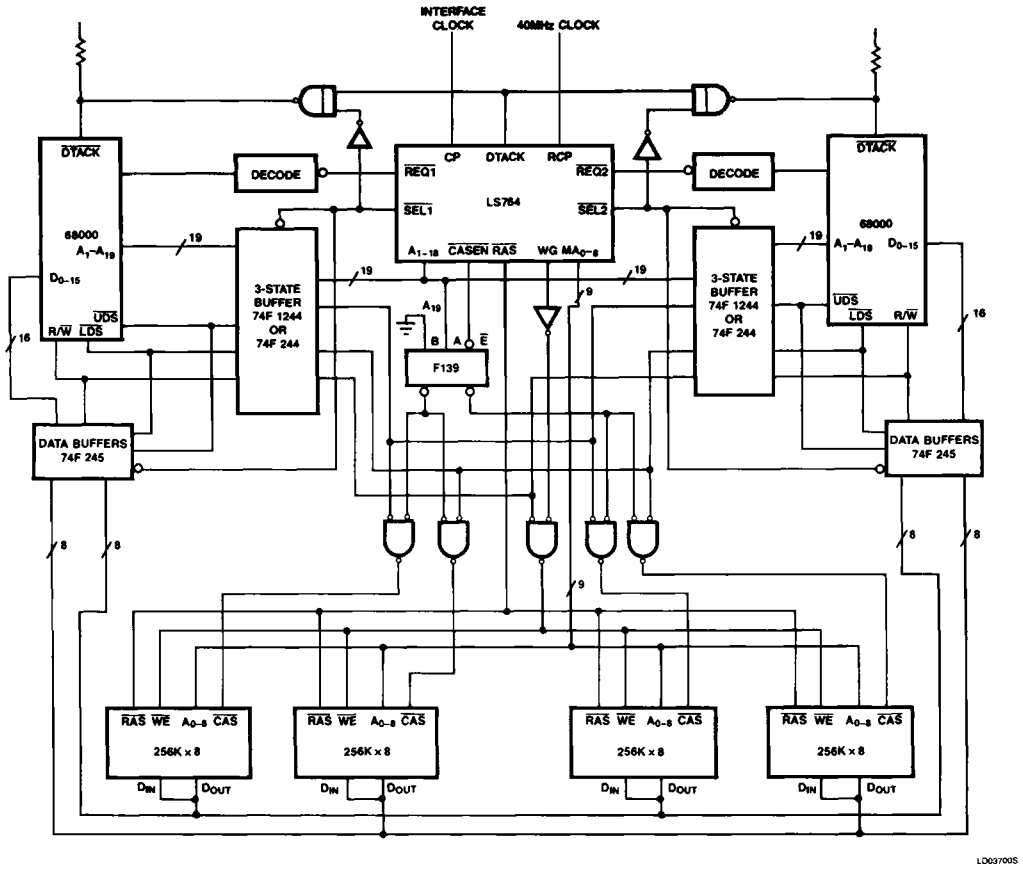

Figure 3. TWO 68000 Processors with 1 Mbyte RAM

ABSOLUTE MAXIMUM RATINGS (Over the operating free-air temperature range unless otherwise noted.)

PARAMETER		74LS764	UNIT
V_{CC}	Supply voltage	7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in LOW output state	96	mA
T_A	Operating free-air temperature range	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER			74LS764			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage		4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			V
V_{IL}	LOW-level input voltage				+0.7	V
I_{IK}	Input clamp current				−18	mA
I_{OH}	HIGH-level output current				−400	μA
I_{OL}	LOW-level output current	V_{OL} = 450mV			24	mA
		V_{OL} = 650mV			48	mA
T_A	Operating free-air temperature		0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]			74LS764			UNIT
					Min	Typ[2]	Max	
V_{OH}	HIGH-level output current	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = −35mA	±10%V_{CC}	2.4	3.2		V
				±5%V_{CC}	2.7	3.4		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = 60mA	±10%V_{CC}		.35	.50	V
				±5%V_{CC}		.35	.50	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}				−0.7	−1.5	V
I_I	Input current at maximum input voltage	V_{CC} = 0.0V, V_I = 7.0V					100	μA
I_{IH}	HIGH-level input current	V_{CC} = MAX, V_I = 2.7V					20	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.5V				−0.4	−0.6	mA
I_{RH}[3]	HIGH-level reflection current	V_{CC} = MIN, force 2.4V					−35	mA
I_{RL}[4]	LOW-level reflection current	V_{CC} = MIN, force 0.8V			60			mA
I_{CC}	Supply current (total)	V_{CC} = MAX				175	200	mA

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. I_{RH} is the current necessary to guarantee the LOW to HIGH transition in a 70Ω transmission line. This output condition results in a current that is approximately one half of the short circuit output current (I_{OS}).
4. I_{RL} is the current necessary to guarantee the HIGH to LOW transition in a 70Ω transmission line.

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AC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_{CC} = 5.0V \pm 5\%$

PARAMETER		TEST CONDITIONS	74LS764 $C_L = 300pF$, $R_L = 70\Omega$			UNIT
			Min	Typ	Max	
f_{MAX}	Maximum Clock Frequency		30	32		MHz
t_{PLH} t_{PHL}	Propagation delay CP(↑) to $\overline{SEL_1}$	AC Waveforms	18 18	30 30	38 38	ns
t_{PLH} t_{PHL}	Propagation delay CP(↓) to $\overline{SEL_2}$		18 18	30 30	38 38	ns
t_{PLH}	Propagation delay CP(B) to GNT		18	30	38	ns
t_{PHL}	Propagation delay (Note 1)		18	35	45	ns
t_{PLH} t_{PHL}	Propagation delay CP(B) to MA(Row Address)		15 15	32 32	40 40	ns
t_{PLH}	Propagation delay CP(F) to $\overline{RAS}$		15	30	40	ns
t_{PHL}	Propagation delay CP(C) to $\overline{RAS}$		15	32	42	ns
t_{PLH}	Propagation delay CP(D) to WG		15	28	38	ns
t_{PHL}	Propagation delay (Note 1)		32	52	62	ns
t_{PLH} t_{PHL}	Propagation delay CP(D) to MA(Column Address)		15 15	30 30	42 42	ns
t_{PLH}	Propagation delay (Note 1)		30	48	60	ns
t_{PHL}	Propagation delay CP(E) to $\overline{CASEN}$		15	32	42	ns
t_{PLH}	Propagation delay CP(F) to DTACK		15	32	40	ns
t_{PHL}	Propagation delay (Note 1)		34	50	62	ns
t_{PLH} t_{PHL}	Propagation delay CP(transition) to MA(Refresh)		28 28	50 50	62 62	ns

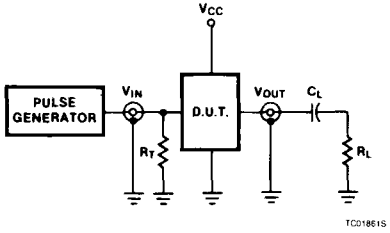
NOTE:
These delays are with respect to clock edge "G" of the $\overline{REQ_1}$ or $\overline{REQ_2}$ access cycle shown on the AC Waveforms.

AC SET-UP AND HOLD REQUIREMENTS

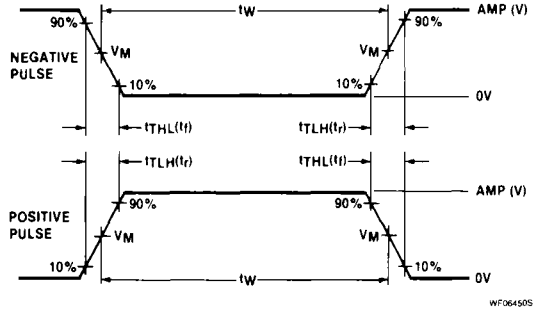
PARAMETER		TEST CONDITIONS	74LS764 $C_L = 300pF$, $R_L = 70\Omega$		UNIT
			Min	Max	
$t_s(H)$ $t_s(L)$	Set-up time, HIGH or LOW $\overline{REQ_1}$, $\overline{REQ_2}$ to CP	AC Waveforms	3 3		ns
$t_h(H)$ $t_h(L)$	Hold time, HIGH or LOW CP to $\overline{REQ_1}$, $\overline{REQ_2}$		5 5		ns
$t_s(H)$ $t_s(L)$	Set-up time, HIGH or LOW $A_1 - A_{18}$ to CP(falling edge)		-8** -8**		ns
$t_h(H)$ $t_h(L)$	Hold time, HIGH or LOW CP(falling edge) to $A_1 - A_{18}$		14 14		ns
$t_w(H)$ $t_w(L)$	CP pulse width, HIGH or LOW		19 18		ns
$t_w(H)$ $t_w(L)$	RCP pulse width, HIGH or LOW		10 12		ns

NOTES:
** These numbers indicate that the address inputs have a negative set-up time and could be valid 8ns after the falling edge of the CP clock. It is suggested that $\overline{SEL_2}$ be used to enable Address Bus 2 and the opposite polarity of the same be used, instead of SEL1 to enable Address Bus 1. This will insure that set-up time for Address Bus 1 is not violated.

TEST CIRCUITS AND WAVEFORMS



Test Circuit Simulating RAM Boards



V_M = 1.3V for 74LS; V_M = 1.5V for all other TTL families.

Input Pulse Definition

DEFINITIONS

R_L = Load resistor to GND; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

D = DIODES are IN916, IN3064, or equivalent.

t_{TLH}, t_{THL} values should be less than or equal to the table entries.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74LS	3.0V	1MHz	500ns	15ns	6ns

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