FIFO

512 x 9 FIFO

FEATURES

- Very high speed: 15, 20, 25 and 35ns access
- High-performance, low-power CMOS process
- Single +5V ±10% supply
- Low power: 5mW typ. (standby); 350mW typ. (active)
- TTL compatible inputs and outputs
- Asynchronous READ and WRITE
- Empty, Half-Full and Full Flags
- Half-Full Flag in STAND ALONE mode
- Auto-retransmit capability
- Fully expandable by width and depth
- Pin and function compatible with higher density standard FIFOs

OPTIONS MARKING

- Timing

15ns access time	-15
20ns access time	-20
25ns access time	-25
35ns access time	-35

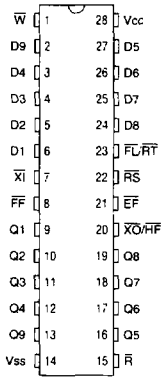
- Packages

Plastic DIP (300 mil)	None
Plastic DIP (600 mil)	W
PLCC	EJ
SOJ (300 mil)	DJ

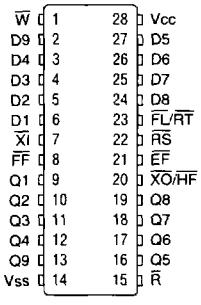
Available in ceramic packages tested to meet military specifications. Please refer to Micron's ***Military Data Book.***

PIN ASSIGNMENT (Top View)

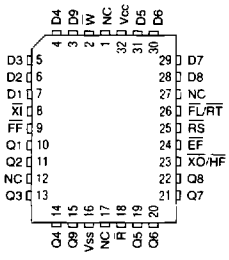
28-Pin DIP
(A-9, A-11)



28-Pin SOJ
(E-8)



32-Pin PLCC
(D-2)



GENERAL DESCRIPTION

The Micron FIFO family employs high-speed, low-power CMOS designs using a true dual port, six-transistor memory cell with resistor loads.

These devices are written and read in a first-in-first-out (FIFO) sequence. Dual read and write pointers handle the internal addressing, so no external address generation is required. Information can be written to and read from the FIFO asynchronously and independently at the input and output ports. This allows information to be transferred independently in and out of the FIFO at varying data rates. Visibility of the memory volume is given through empty, half-full and full flags. While the full flag is asserted, attempted writes are inhibited. Likewise, while the empty flag is asserted, further reads are inhibited and the outputs remain in High-Z. Expansion out, expansion in, and first load pins are provided to expand the depth of the FIFO memory array, with no performance degradation. A retransmit pin allows data to be re-sent on the receiver's request when the FIFO is in the STAND ALONE mode.

The depth and/or width of the FIFO can be expanded by cascading multiple devices. Also, the MT52C9005 is speed, function and pin compatible with higher density FIFOs from Micron. This upward compatibility with 1K and 2K FIFOs provides a single-chip, depth-expansion solution.

FIFO

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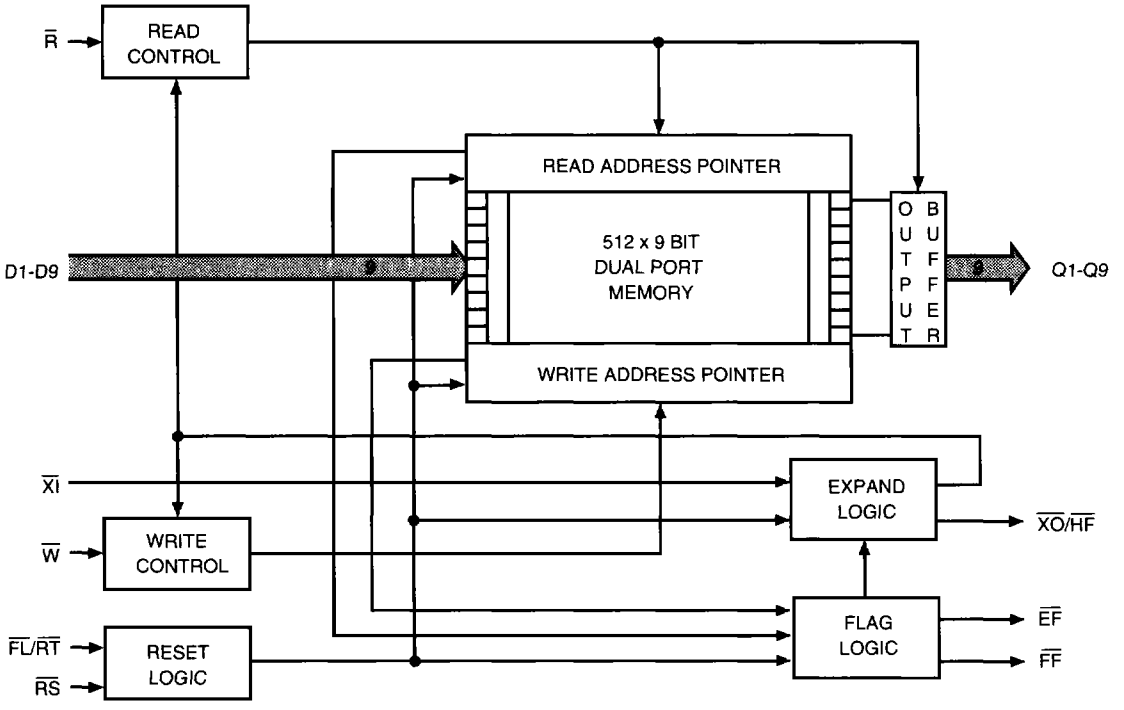
FUNCTIONAL BLOCK DIAGRAM



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PIN DESCRIPTIONS

LCC PIN NUMBER(S)	DIP PIN NUMBER(S)	SYMBOL	TYPE	DESCRIPTION
25	22	$\overline{RS}$	Input	Reset: Taking $\overline{RS}$ LOW will reset the FIFO by initializing the read and write pointers and all flags. After the device is powered up, it must be reset before any writes can take place.
2	1	$\overline{W}$	Input	Write Strobe: $\overline{W}$ is taken LOW to write data from the input port (D1-D9) into the FIFO memory array.
18	15	$\overline{R}$	Input	Read Strobe: $\overline{R}$ is taken LOW to read data from the FIFO memory array to the output port (Q1-Q9).
8	7	$\overline{XI}$	Input	Expansion In: This pin is used for DEPTH EXPANSION mode. In SINGLE DEVICE mode, it should be grounded. In EXPANDED mode, it should be connected to Expansion-Out ($\overline{XO}$)of the previous device in the daisy chain.
26	23	$\overline{FL}/\overline{RT}$	Input	First Load: Acts as first load signal in DEPTH EXPANSION mode. $\overline{FL}$, if low, will enable the device as the first to be loaded (enables read and write pointers). $\overline{FL}$ should be tied LOW for the first FIFO in the chain, tied HIGH for all other FIFOs in the chain. Retransmit: Acts as retransmit signal in STAND ALONE mode. $\overline{RT}$ is used to enable the RETRANSMIT cycle. When taken LOW, $\overline{RT}$ resets the read pointer to the first data location and the FIFO is then ready to retransmit data on the following READ operation(s). The flags will be affected according to specific data conditions.
7, 6, 5, 4, 31, 30, 29, 28, 3	6, 5, 4, 3, 27 26, 25, 24, 2	D1-D9	Input	Data Inputs
24	21	$\overline{EF}$	Output	Empty Flag: Indicates empty FIFO memory when LOW, inhibiting further READ cycles.
9	8	$\overline{FF}$	Output	Full Flag: Indicates full FIFO memory when LOW, inhibiting further WRITE cycles.
23	20	$\overline{XO}/\overline{HF}$	Output	Expansion Out: Acts as expansion out pin in DEPTH EXPANSION mode. $\overline{XO}$ will pulse LOW on the last physical WRITE or the last physical READ. $\overline{XO}$ should be connected to $\overline{XI}$ of the next FIFO in the daisy chain. Half-Full Flag: Acts as Half-Full Flag in STAND ALONE mode. $\overline{HF}$ goes LOW when the FIFO becomes more than Half-full; will stay LOW until the FIFO becomes Half-full or less.
10, 11, 13, 14, 19, 20, 21, 22, 15	9, 10, 11, 12, 16 17, 18, 19, 13	Q1-Q9	Output	Data Output: Output or High-Z.
32	28	Vcc	Supply	Power Supply: +5V ±10%
16	14	Vss	Supply	Ground

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FUNCTIONAL DESCRIPTION

The MT52C9005 uses a dual port SRAM memory cell array with separate read and write pointers. This results in a flexible length FIFO buffer memory, with independent, asynchronous READ and WRITE capabilities and with no fall-through or bubble-through time constraints.

Note: *For dual-function pins, the function that is not being discussed will be surrounded by parentheses. For example, when discussing the half-full flag, the* $\overline{XO}/\overline{HF}$ *pin will be shown as* $(\overline{XO})/\overline{HF}$.

RESET

After Vcc is stable, RESET ($\overline{RS}$) must be taken LOW to initialize the read and write pointers and flags. During the reset pulse, the state of the $\overline{XI}$ pin will determine if the FIFO will operate in the STAND ALONE or DEPTH EXPANSION mode. The STAND ALONE mode is entered if $\overline{XI}$ is LOW. If $\overline{XI}$ is connected to $\overline{XO}$ of another FIFO, the DEPTH EXPANSION mode is selected.

WRITING THE FIFO

Data is written into the FIFO when the write strobe ($\overline{W}$) pin is taken LOW, while $\overline{FF}$ is HIGH. The WRITE cycle is initiated by the falling edge of $\overline{W}$ and data on the D1-D9 pins are latched on the rising edge. If the location to be written is the last empty location in the FIFO, the $\overline{FF}$ will be asserted (LOW) after the falling edge of $\overline{W}$. While $\overline{FF}$ is LOW, any attempted writes will be inhibited, with no loss of data already stored in the FIFO. When a device is used in the STAND ALONE mode, $(\overline{XO})/\overline{HF}$ is asserted when the half-full-plus-one location (512/2 + 1) is written. It will stay asserted until the FIFO becomes half-full or less. The first WRITE to an empty FIFO will cause $\overline{EF}$ to go HIGH after the rising edge of $\overline{W}$. When operating in the DEPTH EXPANSION mode, the last location write to a FIFO will cause $\overline{XO}/(\overline{HF})$ to pulse LOW. This will enable writes to the next FIFO in the chain.

READING THE FIFO

Information is read from the FIFO when the read strobe ($\overline{R}$) pin is taken LOW and the FIFO is not empty ($\overline{EF}$ is HIGH). The data-out (Q1-Q9) pins will go active (Low-Z) ^tRLZ after the falling edge of $\overline{R}$ and valid data will appear ^tA after the falling edge of $\overline{R}$. After the last available data word is read, $\overline{EF}$ will go LOW upon the falling edge of $\overline{R}$. While $\overline{EF}$ is asserted LOW, any attempted reads will be inhibited and the outputs will stay inactive (High-Z). When the FIFO is being used in the SINGLE DEVICE mode and the half-full-plus-one location is read, $(\overline{XO})/\overline{HF}$ will go HIGH after the rising edge of $\overline{R}$. When the FIFO is full ($\overline{FF}$ LOW) and a read is initiated, $\overline{FF}$ will go HIGH after the rising edge of $\overline{R}$. When operating in the EXPANDED mode, the last location read to a FIFO will cause $\overline{XO}/\overline{HF}$ to pulse LOW. This will enable further reads from the next FIFO in the chain.

RETRANSMIT

In the STAND ALONE mode, the MT52C9005 allows the receiving device to request that the data read earlier from the FIFO to be repeated, when less than 512 writes have been performed between resets. When the $(\overline{FL})/\overline{RT}$ pin is taken LOW, the read pointer is reset to the first location while the write pointer is not affected. The receiver may again start reading the data from the beginning of the FIFO ^tRTR after $(\overline{FL})/\overline{RT}$ is taken HIGH. The empty, half-full and full flags will be affected as specified for the data volume.

DATA FLOW-THROUGH

Data flow-through is a method of writing and reading the FIFO at its full and empty boundaries, respectively. By holding $\overline{W}$ LOW when the FIFO is full, a WRITE can be initiated from the next ensuing READ pulse. This is referred to as a FLOW-THROUGH WRITE. FLOW-THROUGH WRITEs are initiated from the rising edge of $\overline{R}$. When the FIFO is empty, a FLOW-THROUGH READ can be done by holding $\overline{R}$ LOW and letting the next WRITE initiate the READ. FLOW-THROUGH READs are initiated from the rising edge of $\overline{W}$ and access time is measured from the rising edge of $\overline{EF}$.

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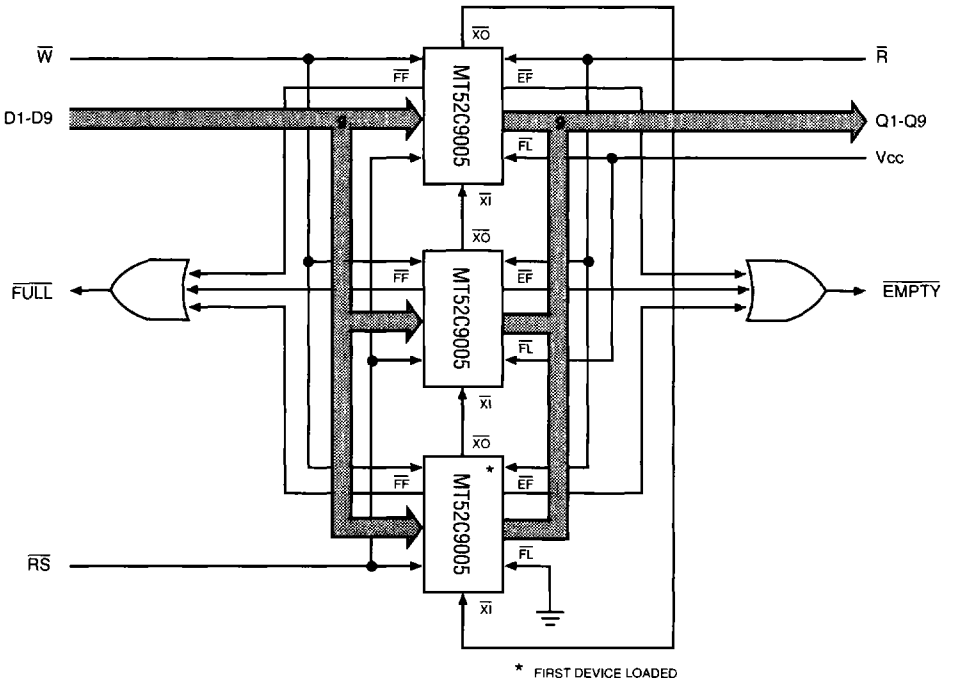

Figure 1
DEPTH EXPANSION

WIDTH EXPANSION

The FIFO word width can be expanded, in increments of 9 bits, using either the stand alone or groups of expanded-depth mode FIFOs. Expanded-width operation is achieved by tying devices together with all control lines ($\overline{W}$, $\overline{R}$, etc.) in common. The flags are monitored from one device or one expanded-depth group (Figure 1) when expanding depth and width.

DEPTH EXPANSION

Multiple MT52C9005s may be cascaded to expand the depth of the FIFO buffer. Three pins are used to expand the memory depth, $\overline{XI}$, $\overline{XO}/(\overline{HF})$ and $\overline{FL}/(\overline{RT})$. Figure 1 illustrates a typical three-device expansion. The DEPTH EXPANSION mode is entered during a RESET cycle, by tying the $\overline{XO}/(\overline{HF})$ pin of each device to the $\overline{XI}$ pin of the next device in the chain. The first device to be loaded will have its $\overline{FL}/(\overline{RT})$ pin grounded. The remaining devices in the chain will have $\overline{FL}/(\overline{RT})$ tied HIGH. During RESET cycle, $\overline{XO}/(\overline{HF})$ of each device is held HIGH, disabling reads and writes to all FIFOs, except the first load device. When the last physical location of the first device is written, the $\overline{XO}/(\overline{HF})$ pin will pulse LOW on the falling edge of $\overline{W}$. This will "pass" the write pointer to the next device in the chain, enabling writes to that device and disabling writes to the first MT52C9005. The writes will continue to go to the second device until last location WRITE. Then it will "pass" the write pointer to the third device.

The full condition of the entire FIFO array is signaled by "OR-ing" all the $\overline{FF}$ pins. On the last physical READ of the first device, its $\overline{XO}/(\overline{HF})$ will pulse again. On the falling edge of $\overline{R}$, the read pointer is "passed" to the second device. The read pointer will, in effect, "chase" the write pointer through the extended FIFO array. The read pointer never overtakes the write pointer. An empty condition is signaled by OR-ing all of the $\overline{EF}$ pins. This inhibits further reads. While in the DEPTH EXPANSION mode, the half-full flag and retransmit functions are not available.

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TRUTH TABLE 1
SINGLE-DEVICE CONFIGURATION/WIDTH-EXPANSION MODE

	INPUTS			INTERNAL STATUS		OUTPUTS		
MODE	$\overline{RS}$	$\overline{RT}$	$\overline{XI}$	Read Pointer	Write Pointer	$\overline{EF}$	$\overline{FF}$	$\overline{HF}$
RESET	0	X	0	Location Zero	Location Zero	0	1	1
RETRANSMIT	1	0	0	Location Zero	Unchanged	1	X	X
READ/WRITE	1	1	0	Increment (1)	Increment (1)	X	X	X

NOTE: 1. Pointer will increment if flag is HIGH.

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TRUTH TABLE 2
DEPTH-EXPANSION/COMPOUND-EXPANSION MODE

	INPUTS			INTERNAL STATUS		OUTPUTS	
MODE	$\overline{RS}$	$\overline{FL}$	$\overline{XI}$	Read Pointer	Write Pointer	$\overline{EF}$	$\overline{FF}$
RESET First Device	0	0	(1)	Location Zero	Location Zero	0	1
RESET All Other Devices	0	1	(1)	Location Zero	Location Zero	0	1
READ/WRITE	1	X	(1)	X	X	X	X

NOTE: 1. XI is connected to $\overline{XO}$ of previous device.
$\overline{RS}$ = Reset Input, $\overline{FL}/\overline{RT}$/DIR= First Load/Retransmit, $\overline{EF}$ = Empty Flag Output, $\overline{FF}$ = Full Flag Output, $\overline{XI}$ = Expansion Input, $\overline{HF}$ = Half-Full Flag Output.

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ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to V_{SS} ..... -0.5V to +7.0V
Operating Temperature T_A (ambient) ..... 0°C to 70°C
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C ≤ T_A ≤ 70°C; Vcc = 5V ±10%)

DESCRIPTION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.5	V	1
Input High (Logic 1) Voltage, All Inputs	V_{IH}	2.0	Vcc+1	V	1
Input Low (Logic 0) Voltage, All Inputs	V_{IL}	-0.5	0.8	V	1, 2

DC ELECTRICAL CHARACTERISTICS

(0°C ≤ T_A ≤ 70°C; Vcc = 5V ±10%)

			MAX					
DESCRIPTION	CONDITIONS	SYMBOL	-15	-20	-25	-35	UNITS	NOTES
Power Supply Current: Operating	$\overline{W}$, $\overline{R}$ ≤ V_{IL}; Vcc = MAX Outputs Open	I_{CC}	140	130	120	100	mA	3
Power Supply Current: Standby	W, $\overline{R}$ ≥ V_{IH}; Vcc = MAX	I_{SB1}	15	15	15	15	mA	
	$\overline{W}$, $\overline{R}$ ≥ Vcc -0.2; Vcc = MAX V_{IL} ≤ Vss +0.2 V_{IH} ≥ Vcc -0.2; f = 0	I_{SB2}	5	5	5	5	mA	

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input Leakage Current	0V ≤ V_{IN} ≤ Vcc	I_{LI}	-10	10	µA	
Output Leakage Current	Output(s) Disabled 0V ≤ V_{OUT} ≤ Vcc	I_{LO}	-10	10	µA	
Output High Voltage	I_{OH} = -2.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C, f = 1 MHz Vcc = 5V	C_I	8	pF	4
Output Capacitance		C_O	8	pF	4

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ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

($0°C \le T_A \le 70°C$; V_{CC} = 5V ±10%)

AC CHARACTERISTICS		-15		-20		-25		-35			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Shift frequency	Fs		40		33.3		28.5		22.2	MHz	
Access time	^tA		15		20		25		35	ns	
READ cycle time	^tRC	25		30		35		45		ns	
READ recovery time	^tRR	10		10		10		10		ns	
READ pulse width	^tRPW	15		20		25		35		ns	6
READ LOW to Low-Z	^tRLZ	5		5		5		5		ns	
READ HIGH to High-Z	^tRHZ		15		15		18		20	ns	
Data hold from $\overline{R}$ HIGH	^tOH	5		5		5		5		ns	
WRITE cycle time	^tWC	25		30		35		45		ns	
WRITE pulse width	^tWPW	15		20		25		35		ns	6
WRITE recovery time	^tWR	10		10		10		10		ns	
WRITE HIGH to Low-Z	^tWLZ	5		5		5		5		ns	5
Data setup time	^tDS	10		12		15		18		ns	
Data hold time	^tDH	0		0		0		0		ns	
RESET cycle time	^tRSC	25		30		35		45		ns	
RESET pulse width	^tRSP	15		20		25		35		ns	6
RESET recovery time	^tRSR	10		10		10		10		ns	
READ HIGH to RESET HIGH	^tRRS	15		20		25		35		ns	
WRITE HIGH to RESET HIGH	^tWRS	15		20		25		35		ns	
RETRANSMIT cycle time	^tRTC	25		30		35		45		ns	
RETRANSMIT pulse width	^tRT	15		20		25		35		ns	
RETRANSMIT recovery time	^tRTR	10		10		10		12		ns	
RETRANSMIT setup time	^tRTS	15		20		25		35		ns	
RESET to $\overline{AEF}$, $\overline{EF}$ LOW	^tEFL		25		30		35		45	ns	
RESET to $\overline{AEF}$, $\overline{HF}$, $\overline{FF}$ HIGH	^tHFH, ^tFFH		25		30		35		45	ns	
READ LOW to $\overline{EF}$ LOW	^tREF		20		20		25		30	ns	
READ HIGH to $\overline{FF}$ HIGH	^tRFF		20		20		25		30	ns	
WRITE LOW to $\overline{FF}$ LOW	^tWFF		20		20		25		30	ns	
WRITE HIGH to $\overline{EF}$ HIGH	^tWEF		20		20		25		30	ns	
WRITE LOW to $\overline{HF}$ LOW	^tWHF		25		30		35		45	ns	
READ HIGH to $\overline{HF}$ HIGH	^tRHF		25		30		35		45	ns	
READ HIGH after $\overline{EF}$ HIGH	^tRPE	15		20		25		35		ns	5
WRITE HIGH after $\overline{FF}$ HIGH	^tWPF	15		20		25		35		ns	5
READ/WRITE to $\overline{XO}$ LOW	^tXOL		20		20		25		35	ns	
READ/WRITE to $\overline{XO}$ HIGH	^tXOH		20		20		25		35	ns	
$\overline{XI}$ pulse width	^tXIP	15		20		25		35		ns	
$\overline{XI}$ setup time	^tXIS	10		12		15		15		ns	
$\overline{XI}$ recovery time	^tXIR	10		10		10		10		ns	

FIFO

NOTES

1. All voltages referenced to Vss (GND).
2. -3V for pulse width < 20ns.
3. Icc is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Flow-through mode only.
6. Pulse widths less than minimum are not allowed.

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AC TEST CONDITIONS

Input pulse level	0 to 3.0V
Input rise and fall times	5ns
Input timing reference level	1.5V
Output reference level	1.5V
Output load	See Figure 2

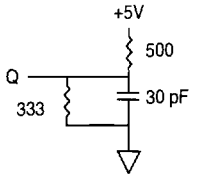
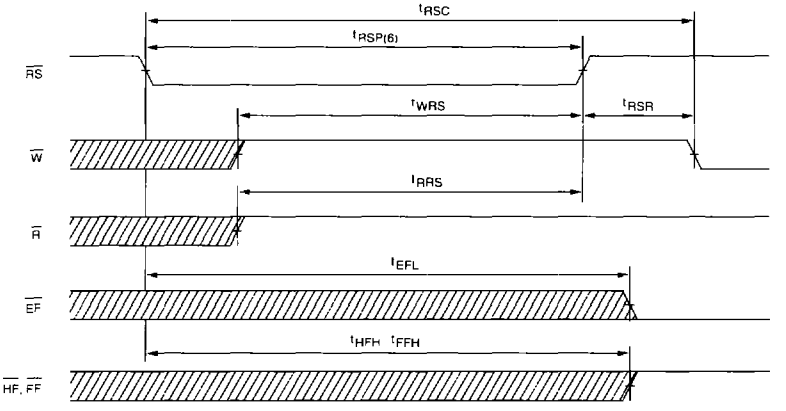
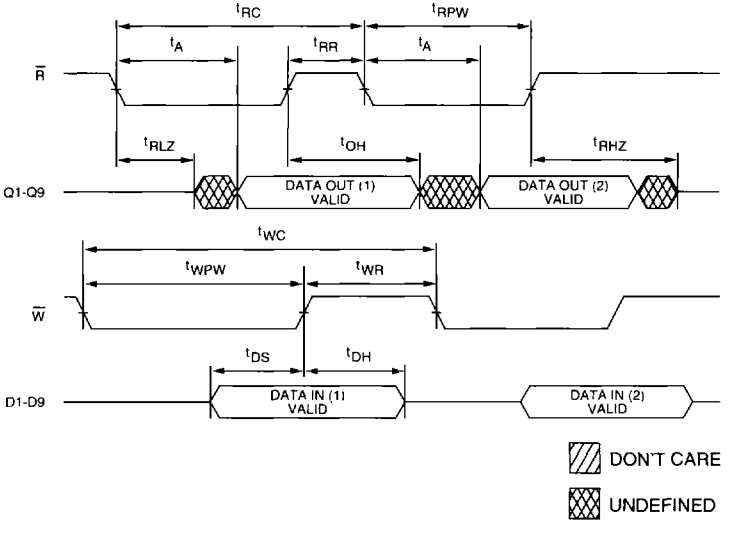


Fig. 2
OUTPUT LOAD EQUIVALENT

RESET



ASYNCHRONOUS READ AND WRITE



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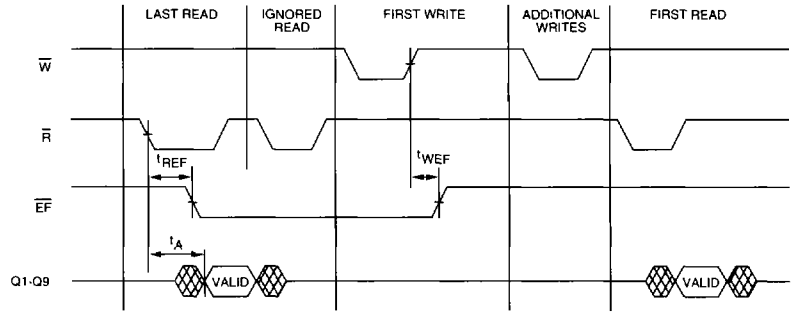
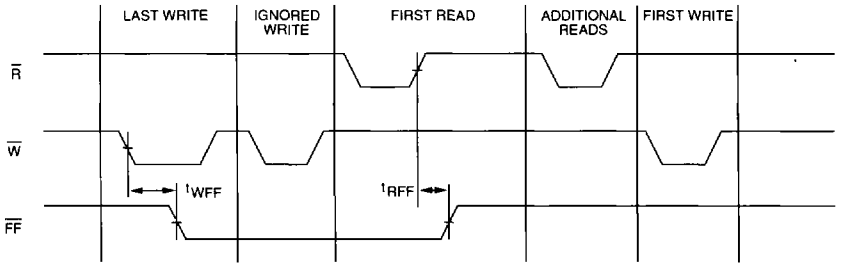
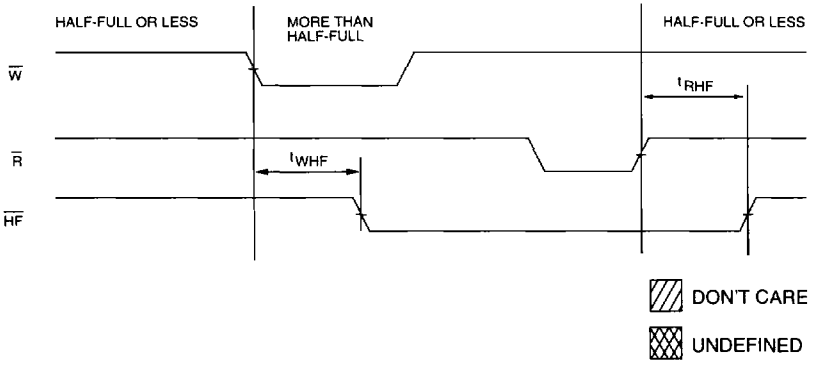
EMPTY FLAG



FULL FLAG



HALF-FULL FLAG



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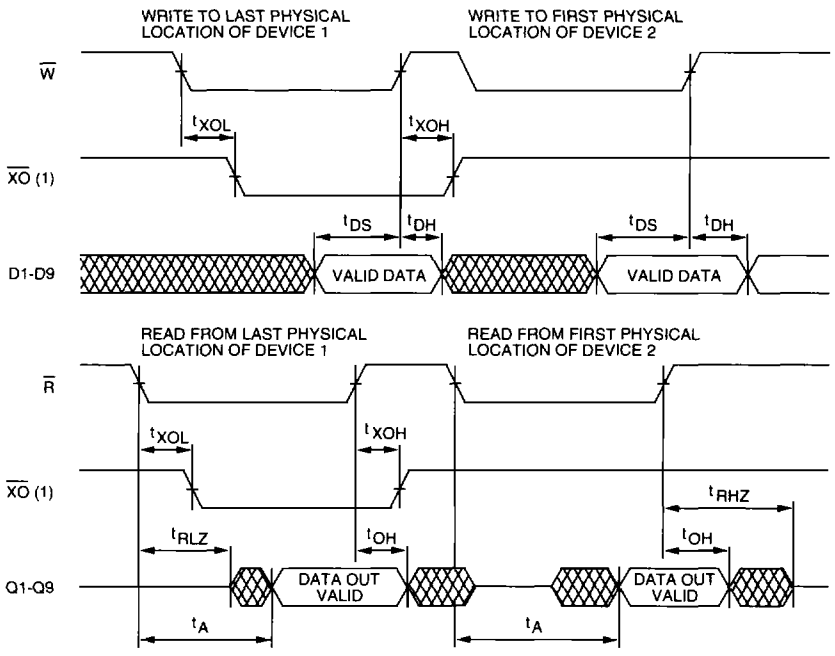
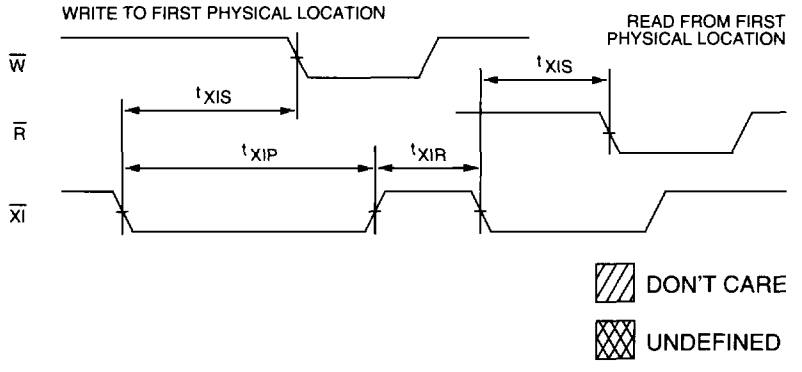
EXPANSION MODE ($\overline{XO}$)



NOTE: $\overline{XO}$ of the Device 1 is connected to $\overline{XI}$ of Device 2.

EXPANSION MODE ($\overline{XI}$)



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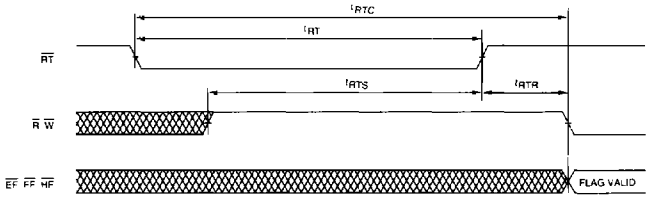
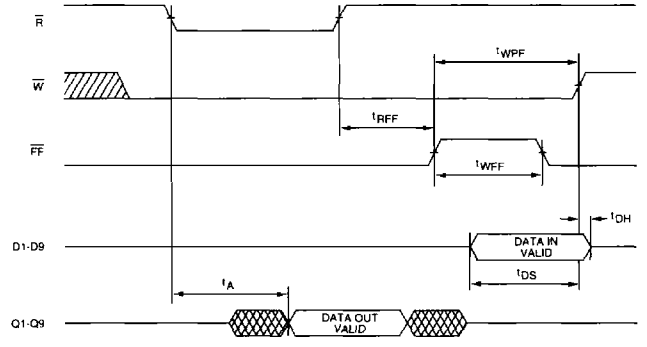
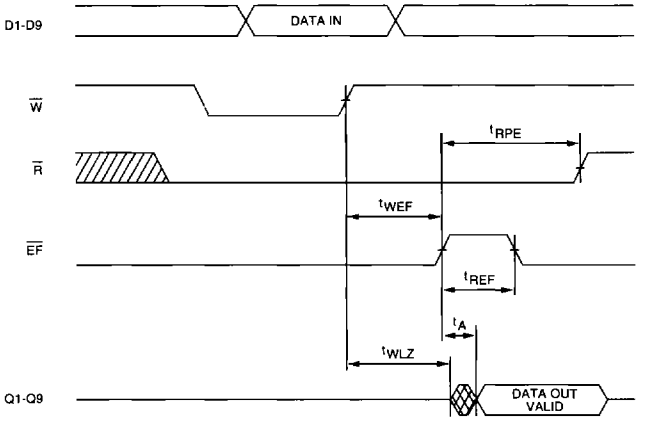
RETRANSMIT



WRITE FLOW-THROUGH



READ FLOW-THROUGH



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