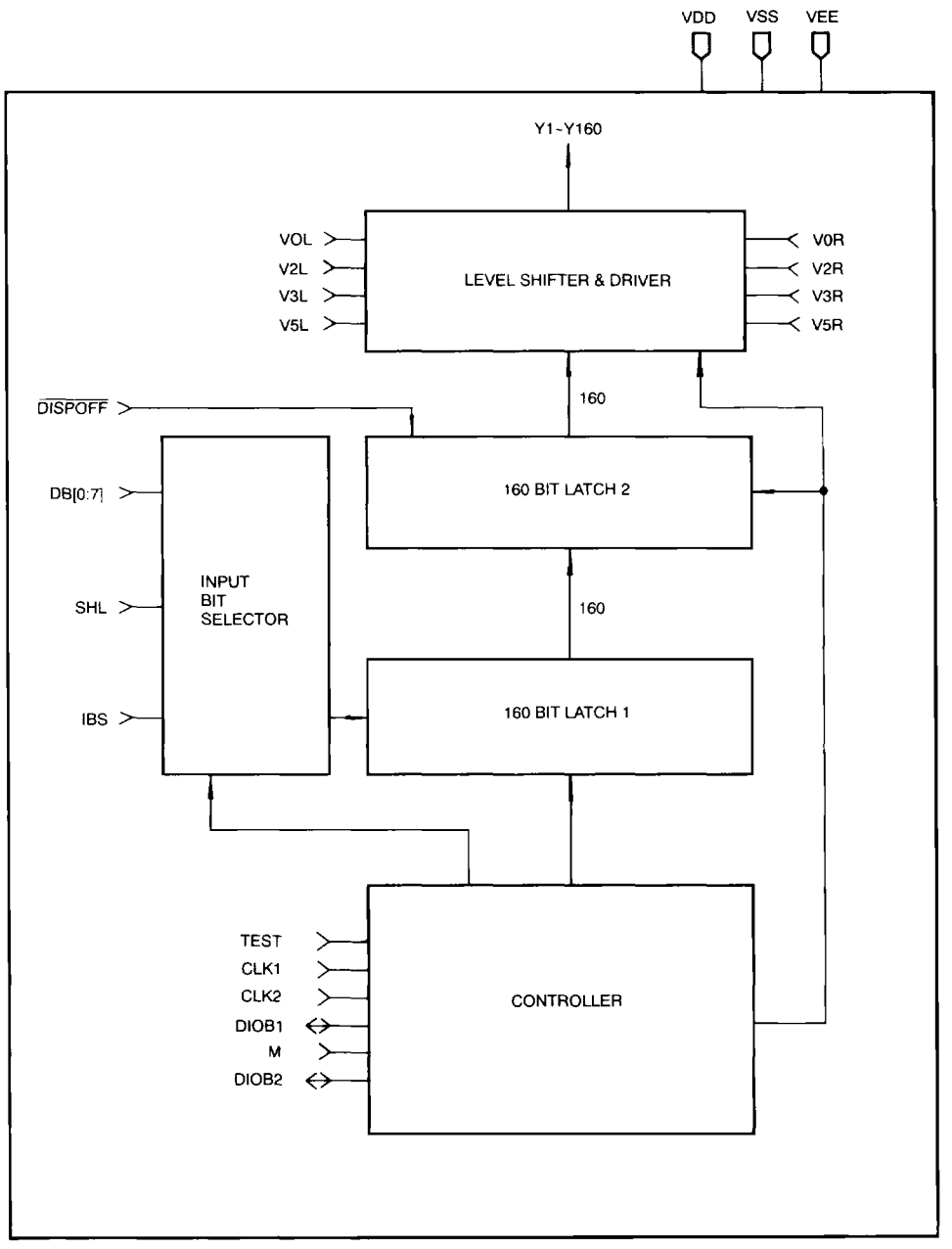
Introduction

KS0787 is a segment driver for dot matrix liquid crystal display system.
It consists of 160 LCD drive circuits, and can drive large area dot matrix display.
It latchs 4 or 8 bits parallel data from a controller. With the stand-by function, only one driver is operated at the same time, and power consumption can be saved.
The duty cycle for LCD driving, is from 1/100 to 1/480 and output bias voltage(VLCD) is from 14V to 37V.
The techology of this device is used high voltage C-MOS Si gate, is packed 191-pin S-TAB(Slim-Tape Automated Bonding).

Features

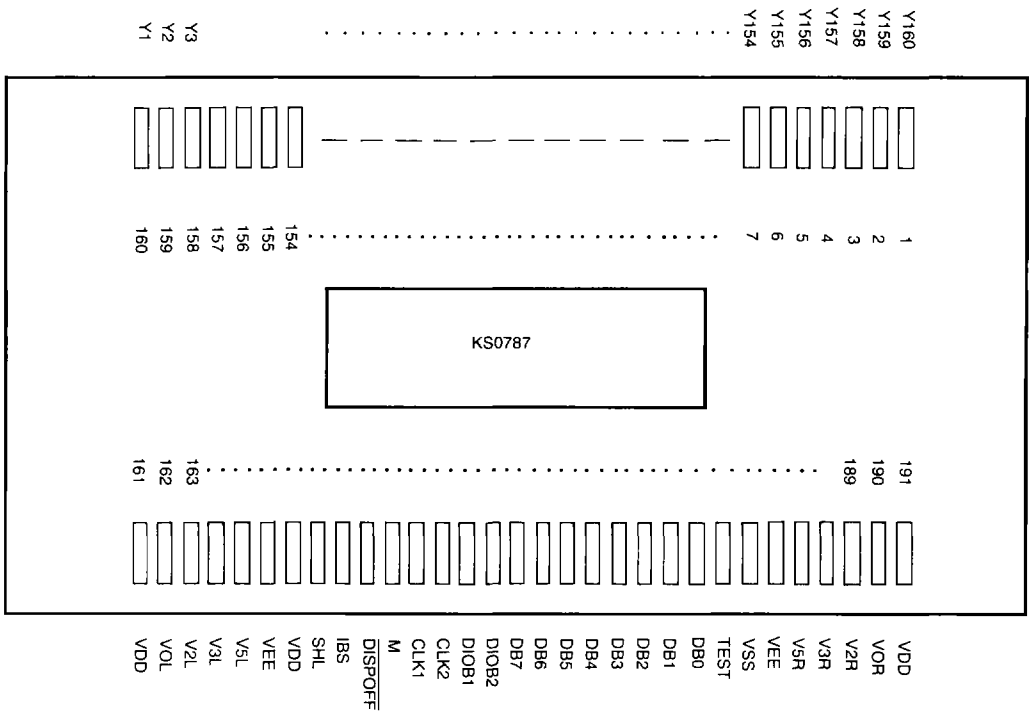
- 4-BIT/8-BIT PARALLEL DATA INPUT FORMAT SELECTABLE
- MULTIPLEXING DUTY RATIO : 1/100~1/480
- LEFT/RIGHT DATA SHIFT DIRECTION SELECTABLE
- INTERNAL AUTOMATIC CHIP ENABLE SIGNAL GENERATOR
- INTERNAL STAND BY FUNCTION
- DISPLAY OFF FUNCTION
- POWER SUPPLY VOLTAGE : INTERNAL LOGIC : 5V ± 10%(3V ± 10%)
  LCD DRIVER VOLTAGE : MAX-32V(-34V)
- OPERATION FREQUENCY : MAX 8MHz (6.5MHz)
- 191-PIN S-TAB(SLIM-TAPE AUTOMATED BONDING)
- C-MOS PROCESS

BLOCK DIAGRAM



PIN DESCRIPTION

1> PIN ASSIGNMENT(TAB)



2> PIN DESCRIPTION

PIN. NO.	PIN NAME	IN/OUT	FUNCTION
161,167,191	VDD	POWER	LOGIC POWER(5V/3V)
185	VSS	POWER	GND.
166, 186	VEE	POWER	LCD DRIVER POWER
162, 190 163, 189 164, 188 165, 187	V0 V2 V3 V5	POWER	LCD DRIVER OUTPUT LEVEL INPUT. V0, V5 : SELECT LEVEL. V2, V3 : NONSELECT LEVEL.
172 173	CLK1 CLK2	INPUT	CLK2 : LATCHS DISPLAY DATA AT THE FALLING EDGE. CLK1 : LATCH2 LATCHS DATA INPUT FROM LATCH1 AT THE FALLING EDGE AND OUTPUTS LATCHED DATA TO DRIVE CIRCUITS.
183~176	DB0~DB7	INPUT	4BIT MODE : DB0~DB3(DB4~DB7=GND) 8BIT MODE : DB0~DB7
169	IBS	INPUT	SELECTS THE NUMBER OF INPUT DATA BITS. IBS=VDD : 8BIT MODE. IBS=VSS : 4BIT MODE.
168	SHL	INPUT	CONTROLS THE SHIFT DIRECTION OF DISPLAY DATA. SHL=VDD : LEFT SHIFT SHL=VSS : RIGHT SHIFT

INPUT DATA SEQUENCE	IBS=VDD		IBS=VSS	
	SHL=VDD	SHL=VSS	SHL=VDD	SHL=VSS
FIRST	DB7-Y160	DB7-Y1	DB3-Y160	DB3-Y1
	DB6-Y159	DB6-Y2	DB2-Y159	DB2-Y2
	DB5-Y158	DB5-Y3	DB1-Y158	DB1-Y3
	DB4-Y157	DB4-Y4	DB0-Y157	DB0-Y4
	DB3-Y156	DB3-Y5		
	DB2-Y155	DB2-Y6		
	DB1-Y154	DB1-Y7		
	DB0-Y153	DB0-Y8		
	≶	≶	≶	≶ ≶
LAST	DB0-Y1	DB0-Y160	DB0-Y1	DB0-Y160

164 165	DIOB1 DIOB2	INPUT / OUTPUT	INPUTS THE ENABLE SIGNAL / OUTPUTS THE ENABLE SIGNAL SHL=VDD : DIOB2=INPUT DIOB1=OUTPUT SHL=VSS : DIOB1=INPUT DIOB2=OUTPUT

<table>
<tr><th>PIN. NO.</th><th>PIN NAME</th><th>IN/OUT</th><th>FUNCTION</th></tr>
<tr><td>171</td><td>M</td><td>INPUT</td><td>ALTERNATED SIGNAL FOR LCD DRIVER OUTPUT
<table>
<tr><th>DATA</th><th>M</th><th>Yi OUT</th><th>OUTPUT LEVEL</th></tr>
<tr><td rowspan="2">H</td><td>H</td><td>V5</td><td>SELECT LOW</td></tr>
<tr><td>L</td><td>V0</td><td>SELECT HIGH</td></tr>
<tr><td rowspan="2">L</td><td>H</td><td>V3</td><td>NONSELECT LOW</td></tr>
<tr><td>L</td><td>V2</td><td>NONSELECT HIGH</td></tr>
</table>
(i=1,2···160)</td></tr>
<tr><td>184</td><td>TEST</td><td>INPUT</td><td>TEST MODE INPUT.
(NORMAL=VSS)</td></tr>
<tr><td>170</td><td>$\overline{\text{DISPOFF}}$</td><td>INPUT</td><td>CONTROLS DISPLAY OFF.
<table>
<tr><th>DISPOFFB</th><th>M</th><th>DISPLAY DATA</th><th>Yi OUT</th></tr>
<tr><td rowspan="4">H</td><td rowspan="2">H</td><td>H</td><td>V5</td></tr>
<tr><td>L</td><td>V3</td></tr>
<tr><td rowspan="2">L</td><td>H</td><td>V0</td></tr>
<tr><td>L</td><td>V2</td></tr>
<tr><td>L</td><td>X</td><td>X</td><td>V0
V0</td></tr>
</table>
(i=1···160)

DISPOFFB=LOW: DISPLAY OFF
DISPOFFB=HIGH: DISPLAY ON</td></tr>
<tr><td>160~1</td><td>Y1-Y160</td><td>OUTPUT</td><td>DISPLAY DATA OUTPUT</td></tr>
</table>

MAXIMUM ABSOLUTE LIMIT (Ta=25 C)

Characteristic	Symbol	Specification	Unit	Remark
Supply voltage	V_{DD}	-0.3 ~+7.0	V	#1
Supply voltage for LCD driving	V_{LCD}	V_{DD}-38~V_{DD}+0.3	V	#1
Input voltage	V_{IN1}	-0.3 ~V_{DD}+0.3	V	#1, #2
Input Voltage	V_{IN2}	V_{EE}-0.3~V_{DD}+0.3	C	#1, #3
Operating Temp.	T_{OPR}	-20 ~+75	C	
Storage Temp.	T_{STG}	-55~+125	C	

#1, REFERENCE POINT VSS.
#2. APPLIES TO INPUT PINS FOR LOGIC INPUT.
#3. APPLIES TO INPUT PINS LCD DRIVER CIRCUIT.

ELECTRICAL CHARACTERISTICS

(V_{DD}=5V(or 3V) ± 10%, V_{SS}=0V, V_{EE}=V_{DD}-37V, Ta=25 C,
V_0=V_{DD}, V_2=V_{DD}-3V, 3V=V_{DD}-3.4V, V_5=V_{EE}=V_{DD}-37V)

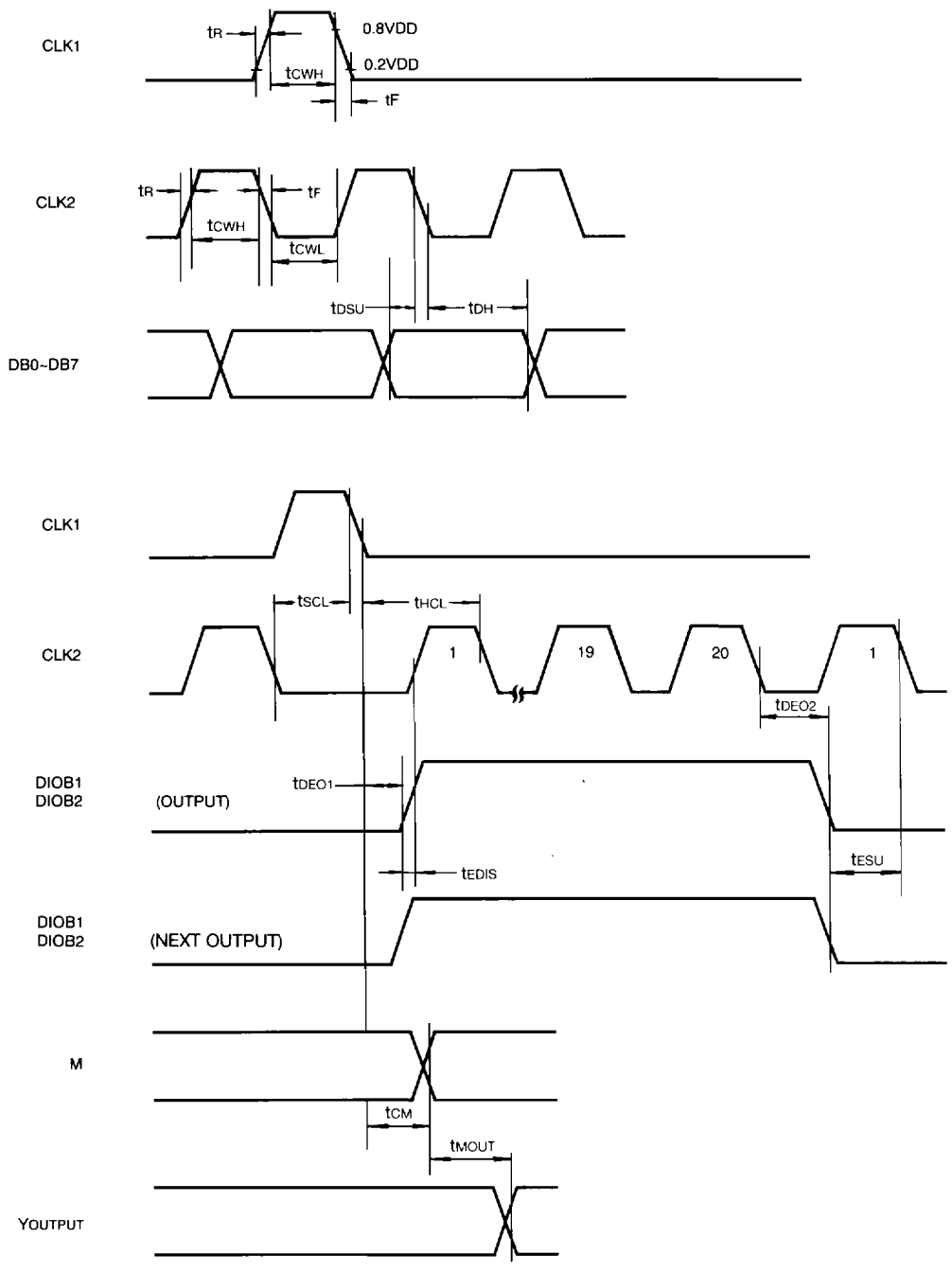
Description		Symbol		Condition / Pin		MIN	TYP	MAX	Unit
Input Voltage		V_{IH}		CLK1, CLK2, TEST, M 1BS, SHL, DBO-DB7, DIOB1, DIOB2, DISPOFFB		0.8V_{DD}		V_{DD}	V
		V_{IL}				0		0.2V_{DD}	V
Output Voltage		V_{OH}		I_{OH}=-0.4mA	DIOB1	V_{DD}-0.4		V_{DD}	V
		V_{OL}		I_{OL}=-0.4mA	DIOB2	0		0.4	V
Y Output on Resistance		R_{ON}		ION=150uA V0, V2,V3,V5 Y~Y160				0.4	V
Input Leakage Current		I_{IL1}		V_{IN1}=VDD~VSS CLK1, CLK2, M, TEST, IBS, SHL DB0~DB7, DISPOFFB DIOB1, DIOB2		-5.0		5.0	uA
		I_{IL2}		V_{IN2}=VDD~VEE V0, V1, V2, V3, V5		-5.0		5.0	uA
Power Dissipation	VDD=5	I_{DD1}		fCLK2=8MHz fCLK1=28KHZ (OPERATION)				5.0	mA
		I_{EE1}						2.0	mA
		I_{ST}	I_{DD2}	LOGIC INPUT=DC LEVEL				0.5	mA
			I_{EE2}	fCLK2=8MHz fCLK1=28KHZ				0.1	mA
	VDD=3	I_{DD1}		fCLK2=6.5MHz fCLK1=36KHZ (OPERATION)				5.0	mA
		I_{EE1}						2.0	mA
		I_{ST}	I_{DD2}	LOGIC INPUT=DC LEVEL				0.5	mA
			I_{EE2}	fCLK2=6.5MHz fCLK1=36KHZ				0.1	mA

* Input and output current is excluded. When an input is at the intermediate level in CMOS, the excessive current flows from the power supply through the input circuit.
To avoid it, V_{IH} and V_{IL} must be fixed to VDD and VSS respectively.

AC CHARACTERISTICS

(Ta=+25 C, V_{DD}=5V(or 3V) ± 10%, V_{SS}=0V, V_{EE}=V_{DD}-37V,
V_1=V_{DD}, V_2=V_{DD}-3V, V_3=V_{DD}-34V, V_5=V_{EE}=V_{DD}-37V)

DESCRIPTION	SYMBOL	CONDITION	VDD=3V			VDD=5V			UNIT	PIN
			MIN	TYP	MAX	MIN	TYP	MAX		
OPERATION FREQUENCY	f_{CLK2}				6.5			8	MHz	CLK2
CLK2 HIGH LEVEL WIDTH	t_{CWH}		45			30			nS	CLK2, CLK1
CLK2 LOW LEVEL WIDTH	t_{CWL}		45			30			nS	CLK2, CLK1
CLOCK RISING TIME	t_R				30			30	nS	CLK1, CLK2
CLOCK FALLING TIME	t_F				30			30	nS	CLK1, CLK2
ENABLE INPUT SET UP TIME	t_{EDS}		50			38			nS	CLK2, DIOB1,2
ENABLE INPUT SET UP TIME	t_{ESU}		30			30			nS	CLK2, DIOB1,2
DATA SET UP TIME	t_{DSU}		30			30			nS	CLK2, DBO~7
DATA HOLD TIME	t_{DH}		30			30			nS	CLK2, DBO~7
CLK2 SET UP TIME	t_{SCL}		100			100			nS	CLK1, CLK2
CLK2 HOLD TIME	t_{HCL}		200			200			nS	CLK1, CLK2
ENABLE OUTPUT DELAY TIME	t_{DE01}	CL=30pF			110			70	nS	CLK, DIOB1,2
ENABLE OUTPUT DELAY TIME	t_{DE02}	CL=30pF			110			70	nS	CLK, DIOB1,2
M PHASE DIFFERENCE	t_{CM}	CL=100pF			300			300	nS	M,CLK1
Y OUTPUT DELAY TIME	t_{MYOUT}	CL=100pF			0.7			0.7	nS	M YOUT
Y OUTPUT DELAY TIME	t_{CYOUT}	CL=100pF			3			3	nS	CLK1, YOUT


CLK1
tR
0.8VDD
0.2VDD
tCWH
tF
CLK2
tR
tF
tCWH
tCWL
tDSU
tDH
DB0~DB7
CLK1
tSCL
tHCL
CLK2
1
19
20
1
tDEO2
DIOB1
DIOB2
(OUTPUT)
tDEO1
tEDIS
tESU
DIOB1
DIOB2
(NEXT OUTPUT)
M
tCM
tMOUT
YOUTPUT

OPERATING PRINCIPLES

IBS	SHL	MODE	INPUT DATA	OUTPUT DATA SHIFT DIRECTION			CHIP ENABLE IN/OUT
VSS	VSS	4BIT RIGHT	DB<0>~DB<3>	DB<3>	→	DB<0>	DIOB1=INPUT
				Y1	~	Y14	
							DIOB2=OUTPUT
				Y157	~	Y160	
	VDD	4BIT LEFT	DB<0>~DB<3>	DB<3>	←	DB<0>	DIOB1=OUTPUT
				Y160	~	Y157	
							DIOB2=INPUTT
				Y4	~	Y1	
	VSS	8BIT RIGHT	DB<0>~DB<7>	DB<7>	→	DB<0>	DIOB1=INPUT
				Y1	~	Y8	
							DIOB2=OUTPUT
				Y153	~	Y160	
VSS	VDD	8BIT LEFT	DB<0>~DB<7>	DB<7>	←	DB<0>	DIOB1=OUTPUT
				Y160	~	Y153	
							DIOB2=INPUTT
				Y8	~	Y1	

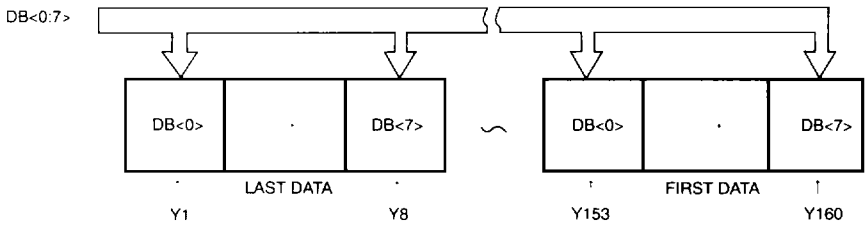
* SHL=VDD(DATA SHIFT DIRECTION=LEFT)
IBS=VSS(4BIT DATA INPUT MODE)

: The KS0787 starts data latch when DIOB2 is at low level. 4-bit parallel data is latched at the falling edge of CLK2. When 160-bit-data latch is completed. the KS0787 automatically stops and enters standby mode and DIOB1 is goes to low level. If DIOB1 is connected with DIOB2 of next-stage LSI, this next-stage LSI is activated when DIOB1 of the previous LSI goes low.

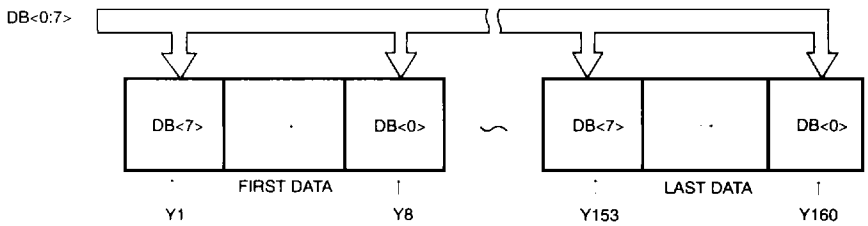
Data is output at the falling edge of CLK1.

DATA LATCH

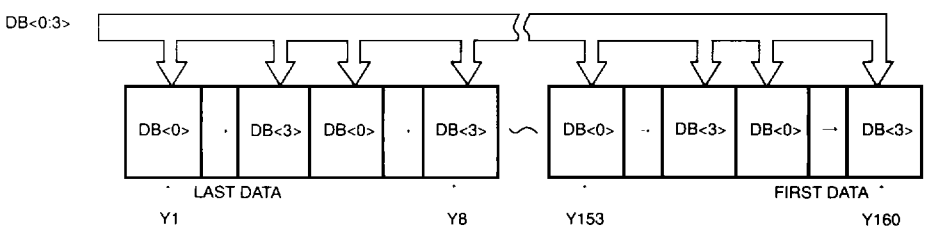
① SHL=VDD
IBS=VDD



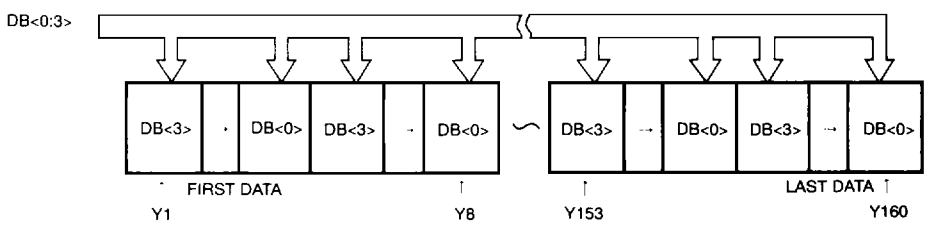
② SHL=VSS
IBS=VDD



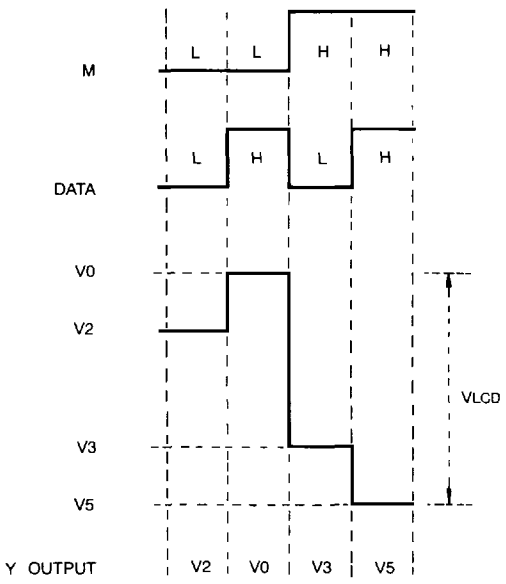
③ SHL=VDD
IBS=VSS



④ SHL=VSS
IBS=VSS



<M & DATA VOLTAGE LEVEL>



V0 : SELECT HIGH LEVEL VOLTAGE

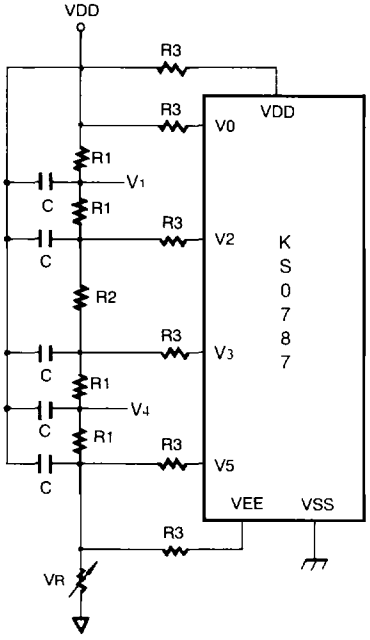
V2 : NONSELECT HIGH LEVEL VOLTAGE

V3 : NONSELECT LOW LEVEL VOLTAGE

V5 : SELECT LOW LEVEL VOLTAGE

* $V_{EE} \leq V_5 \leq V_3 \leq V_2 \leq V_0 \leq V_{DD}$

<LCD · DRIVING POWER CIRCUIT>



1/23 BIAS

1/480 DUTY

V0 : VEE+V_{LCD}

V2 : VEE+21/23*$_{LCD}$

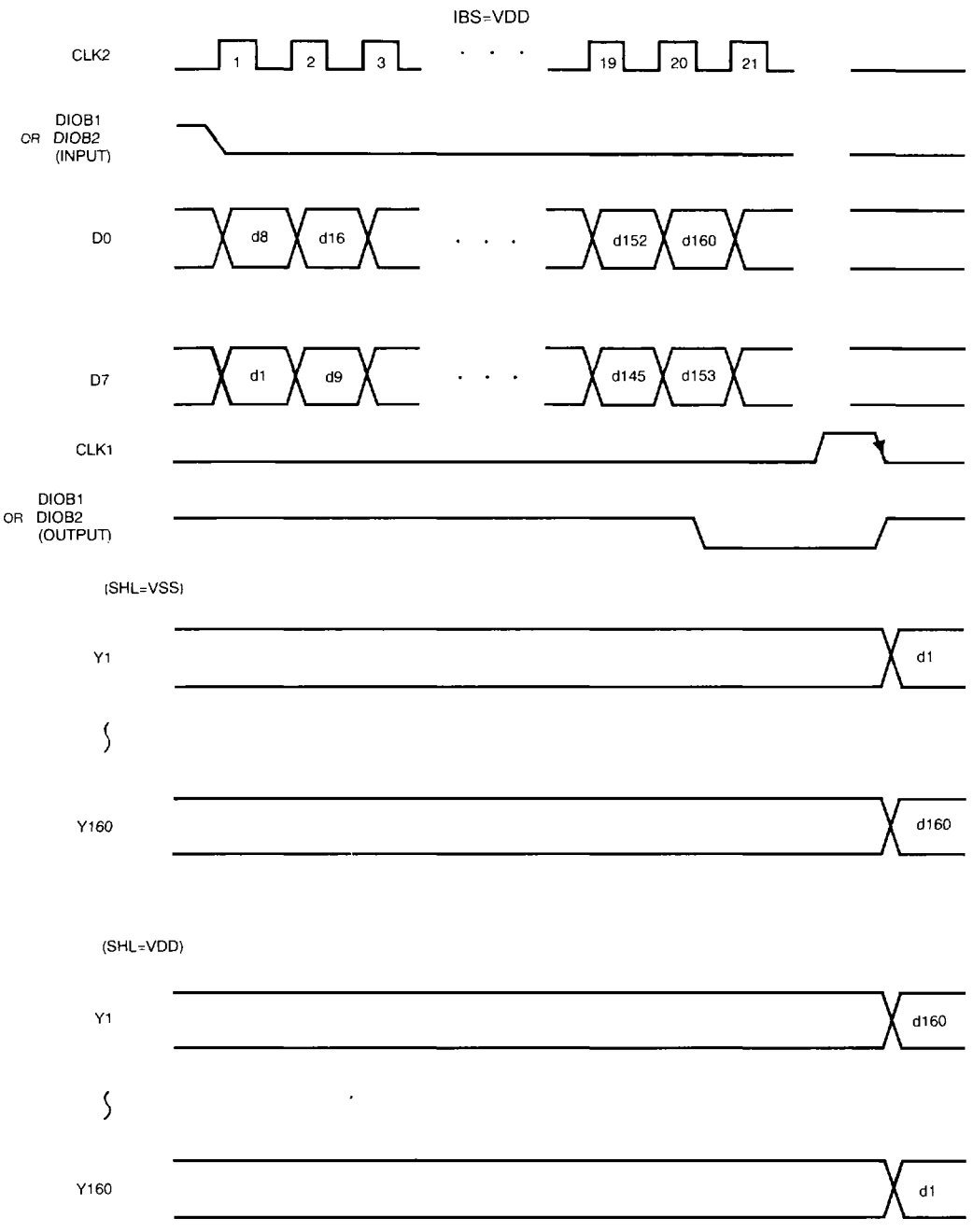
V3 : VEE+2/23*$_{LCD}$

V5 : VEE

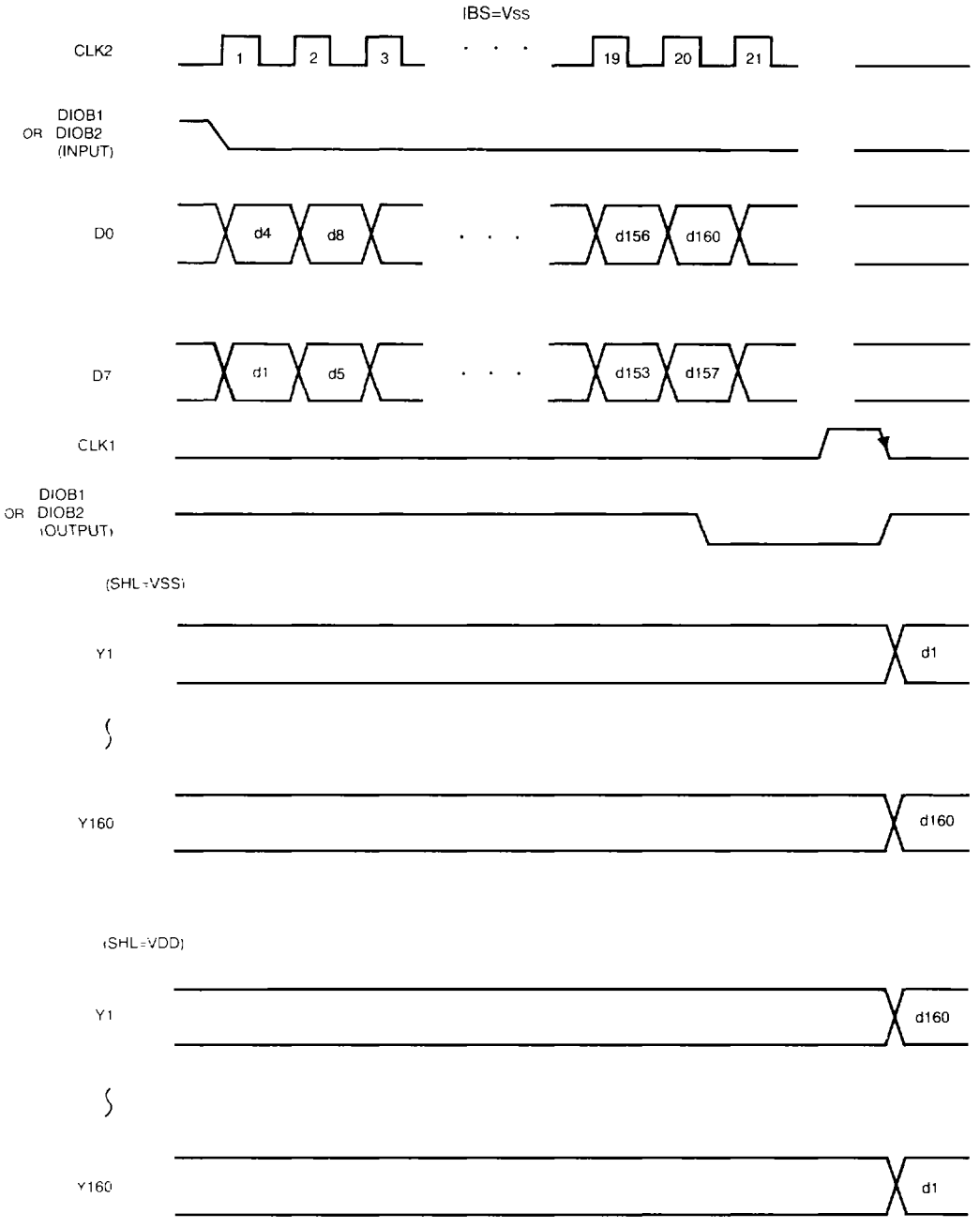
* . V1, V4 : COMMON DRIVER NONSELECT VOLTAGE R3 = 100[Ω]

SAMSUNG ELECTRONICS

TIMING CHART



TIMING CHART



SAMSUNG ELECTRONICS

Application Circuit