PRELIMINARY INFORMATION

4K	Commercial Industrial	X24LC04 X24LC04I	512 x 8 Bit

Electrically Erasable PROM

T-46-13-27

TYPICAL FEATURES

- 3V–6V V_{CC} Operation
- Low Power CMOS
  - —2 mA Active Current Typical
  - —60 μA Standby Current Typical
- Internally Organized as Two Pages
  - —Each 256 x 8
- 2 Wire Serial Interface
- Provides Bidirectional Data Transfer Protocol
- Sixteen Byte Page Write Mode
  - —Minimizes Total Write Time Per Byte
- Self Timed Write Cycle
  - —Typical Write Cycle Time of 5 ms
- Inherent 100+ Years Data Retention
- 8-Pin Mini-DIP Package
- 14-Pin SOIC Package

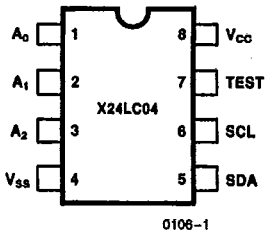
DESCRIPTION

The X24LC04 is a CMOS 4096 bit serial E^2PROM, internally organized as two 256 x 8 pages. The X24LC04 features a serial interface and software protocol allowing operation on a two wire bus.

Xicor E^2PROMs are designed and tested for applications requiring extended endurance.

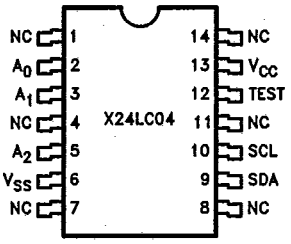
PIN CONFIGURATIONS

PLASTIC CERDIP



0106-1

SOIC



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PIN NAMES

A_0–A_2	Address Inputs
SDA	Serial Data
SCL	Serial Clock
TEST	Hold at V_{SS}
V_{SS}	Ground
V_{CC}	+3V to +6V
NC	No Connect

X24LC04, X24LC04I

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias
X24LC04 ..... −10°C to +85°C
X24LC04I ..... −65°C to +135°C
Storage Temperature ..... −65°C to +150°C
Voltage on any Pin with
Respect to V_{SS} ..... −1.0V to +7V
D.C. Output Current ..... 5 mA
Lead Temperature
(Soldering, 10 Seconds) ..... 300°C

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. OPERATING CHARACTERISTICS

X24LC04 T_A = 0°C to +70°C, V_{CC} = +3V to +6V, unless otherwise specified.
X24LC04I T_A = −40°C to +85°C, V_{CC} = +3V to +6V, unless otherwise specified.

Symbol	Parameter	Limits			Units	Test Conditions
		Min.	Typ.(1)	Max.		
I_{CC}	Power Supply Current		2.0	3.0	mA	f_{SCL} = 100 KHz
I_{SB}(2)	Standby Current V_{CC} = 6V			150	µA	V_{IN} = GND or V_{CC}
I_{SB}(2)	Standby Current V_{CC} = 3V			50	µA	V_{IN} = GND or V_{CC}
I_{LI}	Input Leakage Current		0.1	10	µA	V_{IN} = GND to V_{CC}
I_{LO}	Output Leakage Current		0.1	10	µA	V_{OUT} = GND to V_{CC}
V_{IL}(3)	Input Low Voltage	−1.0		V_{CC} ×0.3	V	
V_{IH}(3)	Input High Voltage	V_{CC} ×0.7		V_{CC} +0.5	V	
V_{OL}	Output Low Voltage			0.4	V	I_{OL} = 3 mA

CAPACITANCE T_A = 25°C, f = 1.0 MHz, V_{CC} = 5V

Symbol	Test	Max.	Units	Conditions
$C_{I/O}$(4)	Input/Output Capacitance (SDA)	8	pF	$V_{I/O}$ = 0V
C_{IN}(4)	Input Capacitance (A_0, A_1, A_2, SCL)	6	pF	V_{IN} = 0V

A.C. CONDITIONS OF TEST

Input Pulse Levels	V_{CC} ×0.1 to V_{CC} ×0.9
Input Rise and Fall Times	10 ns
Input and Output Timing Levels	V_{CC} ×0.5
Output Load	1 TTL Gate and C_L = 100 pF

Notes: (1) Typical values are for T_A = 25°C and nominal supply voltage.
(2) SDA and SCL require pull-up resistor.
(3) V_{IL} min. and V_{IH} max. are for reference only and are not tested.
(4) This parameter is periodically sampled and not 100% tested.

SYMBOL TABLE

WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from Low to High	Will change from Low to High
	May change from High to Low	Will change from High to Low
	Don't Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance

A.C. CHARACTERISTICS LIMITS

X24LC04 T_A = 0°C to +70°C, V_{CC} = +3V to +6V, unless otherwise specified.
X24LC04I T_A = −40°C to +85°C, V_{CC} = +3V to +6V, unless otherwise specified.

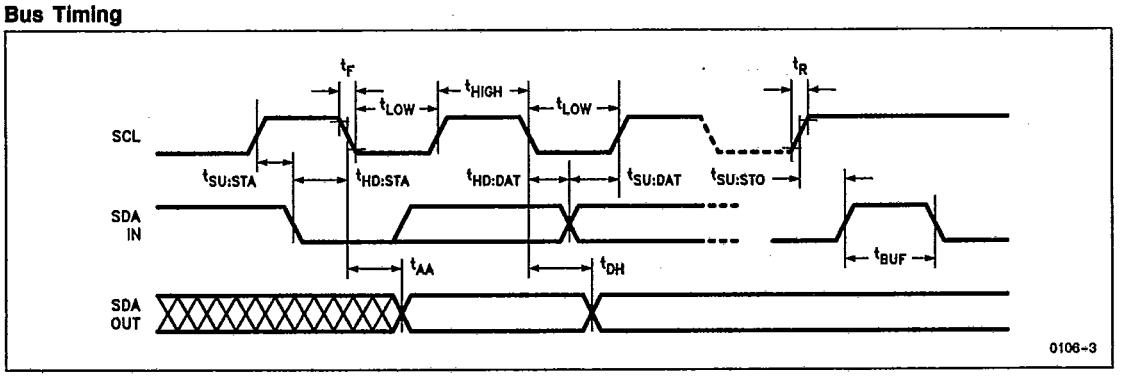
Read & Write Cycle Limits

Symbol	Parameter	Min.	Max.	Units
f_{SCL}	SCL Clock Frequency	0	100	KHz
T_I	Noise Suppression Time Constant at SCL, SDA Inputs		100	ns
t_{AA}	SCL Low to SDA Data Out Valid	0.3	3.5	μs
t_{BUF}	Time the Bus Must Be Free Before a New Transmission Can Start	4.7		μs
$t_{HD:STA}$	Start Condition Hold Time	4.0		μs
t_{LOW}	Clock Low Period	4.7		μs
t_{HIGH}	Clock High Period	4.0		μs
$t_{SU:STA}$	Start Condition Setup Time (for a Repeated Start Condition)	4.7		μs
$t_{HD:DAT}$	Data In Hold Time	0		μs
$t_{SU:DAT}$	Data In Setup Time	250		ns
t_R	SDA and SCL Rise Time		1	μs
t_F	SDA and SCL Fall Time		300	ns
$t_{SU:STO}$	Stop Condition Setup Time	4.7		μs
t_{DH}	Data Out Hold Time	300		ns

Typical Power-Up Timing

Symbol	Parameter	Typ.(5)	Units
t_{PUR}(6)	Power-Up to Read Operation	2.0	μs
t_{PUW}(6)	Power-Up to Write Operation	2.0	μs

Bus Timing



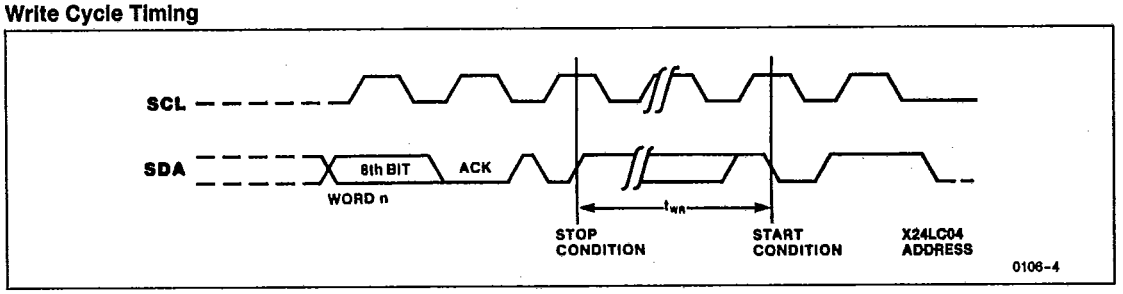
Notes: (5) Typical values are for T_A = 25°C and nominal supply voltage.
(6) This parameter is periodically sampled and not 100% tested.

Write Cycle Limits

Symbol	Parameter	Min.	Typ.(7)	Max.	Units
t_{WR}(8)	Write Cycle Time	10	5		ms

The write cycle time is the time from a valid stop condition of a write sequence to the end of the internal erase/program cycle. During the write cycle, the X24LC04 bus interface circuits are disabled, SDA is allowed to remain high, and the device does not respond to its slave address.

Write Cycle Timing



PIN DESCRIPTIONS

Serial Clock (SCL)

The SCL input is used to clock all data into and out of the device.

Serial Data (SDA)

SDA is a bidirectional pin used to transfer data into and out of the device. It is an open drain output and may be wire-ORed with any number of open drain or open collector outputs.

An open collector output implies the use of a pull-up resistor. For selecting typical values, refer to the Guidelines for Calculating Typical Values of Bus Pull-Up Resistors graph.

Address (A_0)

A_0 is unused by the X24LC04, however, it must be tied to V_{SS} to insure proper device operation.

Address (A_1, A_2)

The Address inputs are used to set the least significant two bits of the six bit slave address. These inputs can be used static or driven. If used statically they must be tied to V_{SS} or V_{CC} as appropriate. If driven they must be driven by open collector outputs with resistor pull-ups to V_{CC}.

DEVICE OPERATION

The X24LC04 supports a bidirectional bus oriented protocol. The protocol defines any device that sends data onto the bus as a transmitter, and the receiving device as the receiver. The device controlling the transfer is a master and the device being controlled is the slave. The master will always initiate data transfers, and provide the clock for both transmit and receive operations. Therefore, the X24LC04 will be considered a slave in all applications.

Clock and Data Conventions

Data states on the SDA line can change only during SCL LOW. SDA state changes during SCL HIGH are reserved for indicating start and stop conditions. Refer to Figures 1 and 2.

Start Condition

All commands are preceded by the start condition, which is a HIGH to LOW transition of SDA when SCL is HIGH. The X24LC04 continuously monitors the SDA and SCL lines for the start condition and will not respond to any command until this condition has been met.

Notes: (7) Typical values are for T_A = 25°C and nominal supply voltage (5V).

(8) t_{WR} is the minimum cycle time from the system perspective; it is the maximum time the device requires to perform the internal write operation.

Figure 1: Data Validity

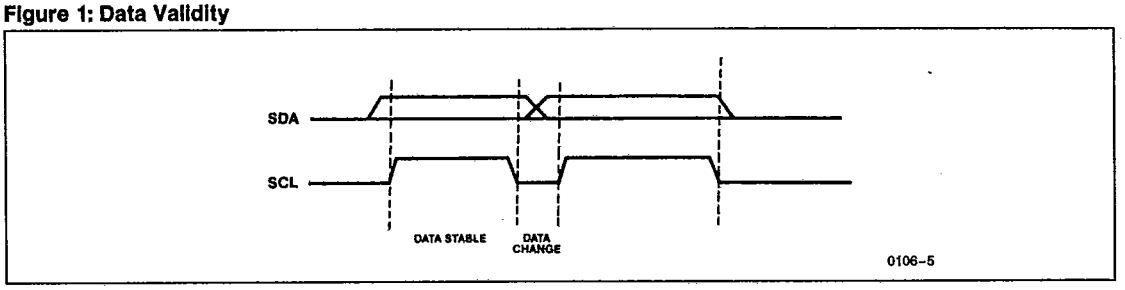
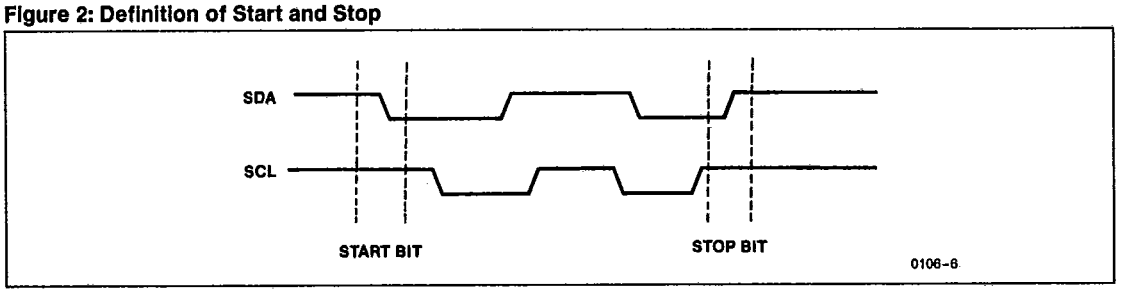


Figure 2: Definition of Start and Stop



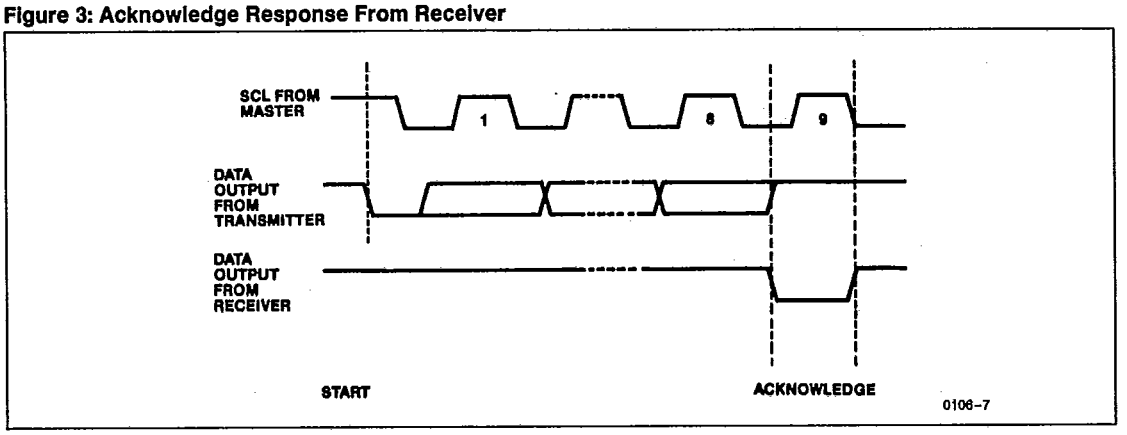
Stop Condition
All communications are terminated by a stop condition, which is a LOW to HIGH transition of SDA when SCL is HIGH. The stop condition is also used by the X24LC04 to place the device in the standby power mode.

Acknowledge
Acknowledge is a software convention used to indicate successful data transfers. The transmitting device, either master or slave, will release the bus after transmitting eight bits. During the ninth clock cycle the receiver will pull the SDA line LOW to acknowledge that it received the eight bits of data. Refer to Figure 3.

The X24LC04 will always respond with an acknowledge after recognition of a start condition and its slave address. If both the device and a write operation have been selected, the X24LC04 will respond with an acknowledge after the receipt of each subsequent eight bit word.

In the read mode the X24LC04 will transmit eight bits of data, release the SDA line and monitor the line for an acknowledge. If an acknowledge is detected and no stop condition is generated by the master, the X24LC04 will continue to transmit data. If an acknowledge is not detected, the X24LC04 will terminate further data transmissions and await the stop condition to return to the standby power mode.

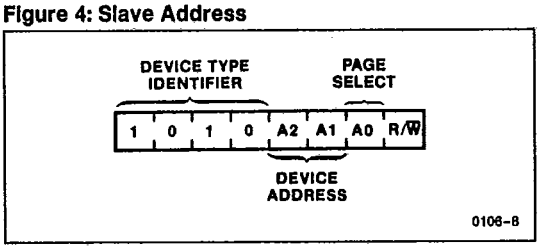
Figure 3: Acknowledge Response From Receiver



DEVICE ADDRESSING

Following a start condition the bus master must output the address of the slave it is accessing. The most significant four bits of the slave address are the device type identifier (see Figure 4). For the X24LC04 this is fixed as 1010[B].

Figure 4: Slave Address



The next two significant bits address a particular device. A system could have up to four X24LC04 devices on the bus (see Figure 10). The four addresses are defined by the state of the A_1 and A_2 inputs.

The next bit of the slave address field (bit 1) is the page select bit. It is used by the host to toggle between the two 256 word pages of memory. This is, in effect the most significant bit for the word address.

The last bit of the slave address defines the operation to be performed. When set to one a read operation is selected, when set to zero a write operation is selected.

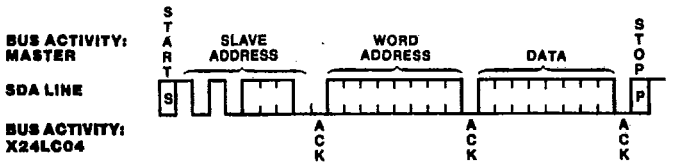
Following the start condition, the X24LC04 monitors the SDA bus comparing the slave address being transmitted with its address (device type and state of A_1 and A_2 inputs). Upon a compare the X24LC04 outputs an acknowledge on the SDA line. Depending on the state of the R/$\overline{W}$ bit, the X24LC04 will execute a read or write operation.

WRITE OPERATIONS

Byte Write

For a write operation, the X24LC04 requires a second address field. This address field is the word address, comprised of eight bits, providing access to any one of the 256 words of memory. Upon receipt of the word address the X24LC04 responds with an acknowledge, and awaits the next eight bits of data, again responding with an acknowledge. The master then terminates the transfer by generating a stop condition, at which time the X24LC04 begins the internal write cycle to the nonvolatile memory. While the internal write cycle is in progress the X24LC04 inputs are disabled, and the device will not respond to any requests from the master. Refer to Figure 5 for the address, acknowledge and data transfer sequence.

Figure 5: Byte Write



Page Write

The X24LC04 is capable of a sixteen byte page write operation. It is initiated in the same manner as the byte write operation, but instead of terminating the write cycle after the first data word is transferred, the master can transmit up to fifteen more words. After the receipt of each word, the X24LC04 will respond with an acknowledge.

After the receipt of each word, the four low order address bits are internally incremented by one. The high order five bits of the address remain constant. If the master should transmit more than sixteen words prior to generating the stop condition, the address counter will "roll over" and the previously written data will be overwritten. As with the byte write operation, all inputs are disabled until completion of the internal write cycle. Refer to Figure 6 for the address, acknowledge and data transfer sequence.

Acknowledge Polling

The disabling of the inputs can be used to take advantage of the typical 5 ms write cycle time. Once the stop condition is issued to indicate the end of the host's write operation the X24LC04 initiates the internal write cycle. ACK polling can be initiated immediately. This involves issuing the start condition followed by the slave address for a write operation. If the X24LC04 is still busy with the write operation no ACK will be returned. If the X24LC04 has completed the write operation an ACK will be returned and the host can then proceed with the next read or write operation.

READ OPERATIONS

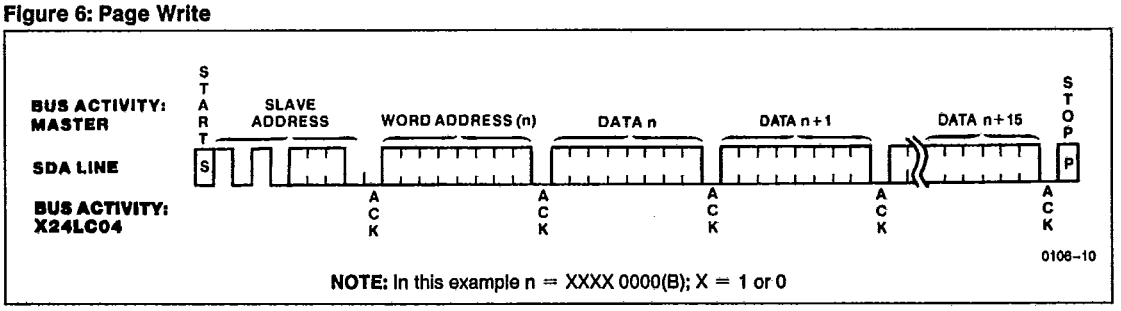
Read operations are initiated in the same manner as write operations with the exception that the bit of the slave address is set to a one. There are three basic read operations: current address read, random read and sequential read.

Note: For each read operation, SDA must be brought back to a high level prior to the stop bit.

Current Address Read

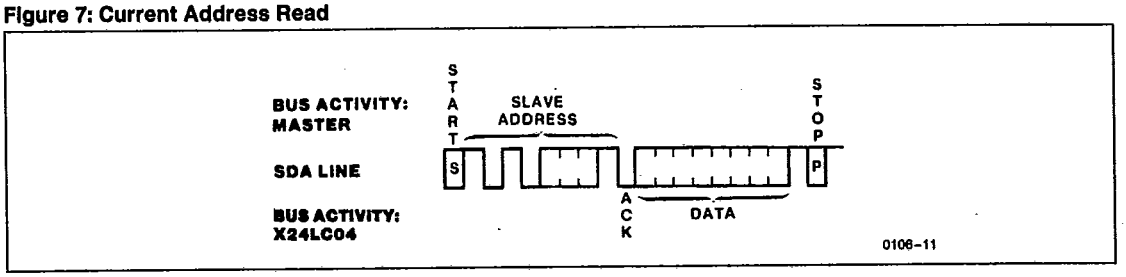
Internally the X24LC04 contains an address counter that maintains the address of the last word accessed, incremented by one. Therefore, if the last access (either a read or write) was to address n, the next read operation would access data from address n+1. Upon receipt of the slave address with R/$\overline{W}$ set to one, the X24LC04 issues an acknowledge and transmits the eight bit word. The master does not acknowledge the transfer but does generate a stop condition and the X24LC04 discontinues transmission. Refer to Figure 7 for the sequence of address, acknowledge and data transfer.

Figure 6: Page Write



NOTE: In this example n = XXXX 0000(B); X = 1 or 0

Figure 7: Current Address Read



Random Read

Random read operations allow the master to access any memory location in a random manner. Prior to issuing the slave address with the R/$\overline{W}$ bit set to one, the master must first perform a "dummy" write operation. The master issues the start condition, and the slave address followed by the word address it is to read. After the word address acknowledge, the master immediately reissues the start condition and the slave address with the R/$\overline{W}$ bit set to one. This will be followed by an acknowledge from the X24LC04 and then by the eight bit word. The master does not acknowledge the transfer but does generate the stop condition and the X24LC04 discontinues transmission. Refer to Figure 8 for the address, acknowledge and data transfer sequence.

Sequential Read

Sequential reads can be initiated as either a current address read or random access read. The first word is transmitted as with the other read modes, however, the master now responds with an acknowledge, indicating it requires additional data. The X24LC04 continues to output data for each acknowledge received. The read operation is terminated by the master not responding with an acknowledge and generating a stop condition.

The data output is sequential, with the data from address n followed by the data from n+1. The address counter for read operations increments all address bits, allowing the entire memory contents to be serially read during one operation. If more than 512 words are read, the counter "rolls over" and the X24LC04 continues to output data for each acknowledge received. Refer to Figure 9 for the address, acknowledge and data transfer sequence.

Figure 8: Random Read

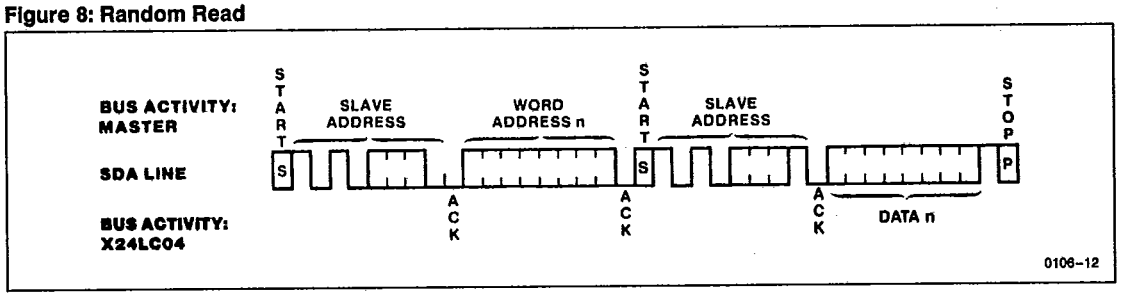


Figure 9: Sequential Read

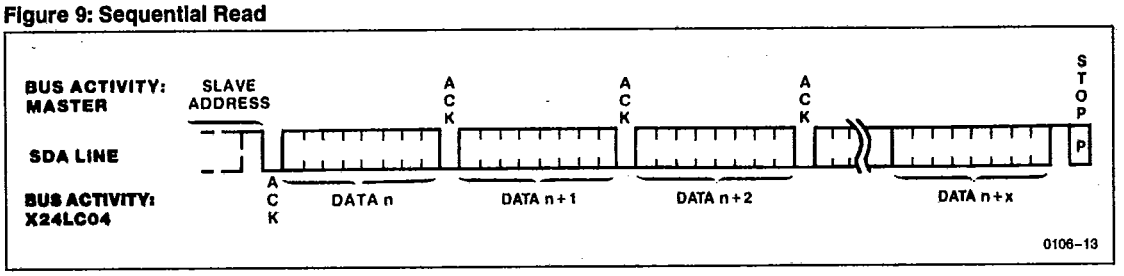
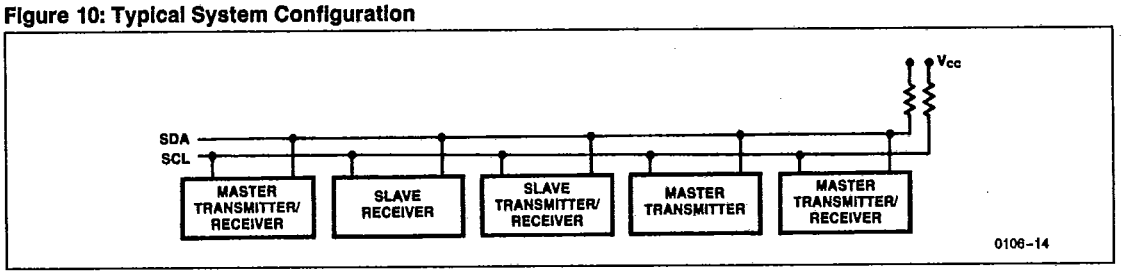
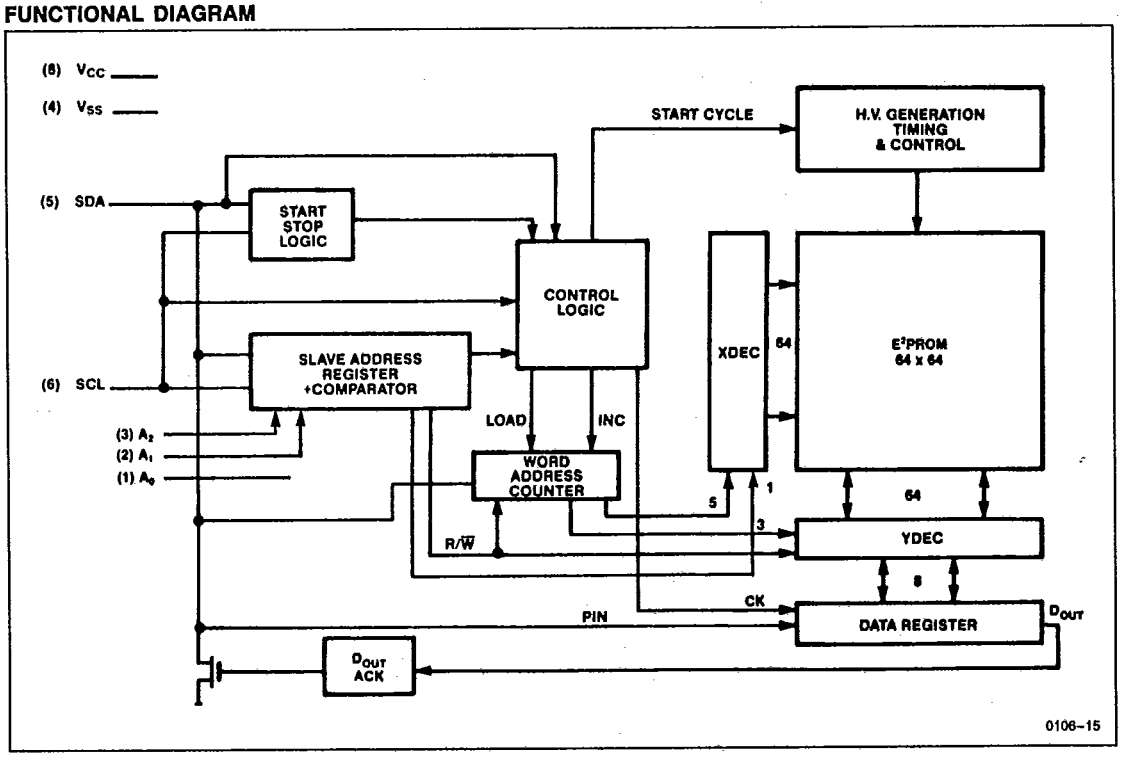


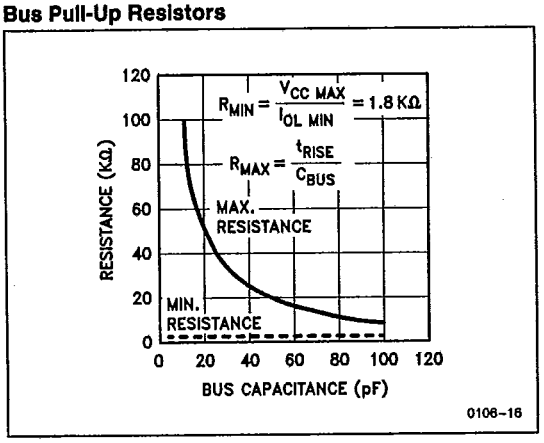
Figure 10: Typical System Configuration



FUNCTIONAL DIAGRAM



Guidelines for Calculating Typical Values of Bus Pull-Up Resistors



X24LC04, X24LC04I

ORDERING INFORMATION

SERIAL E²PROMs

Device Order Number	Organization	Package										Temp. Range	Process Technology	Processing Level
		S	P	D	C	F1	F2	K	J	E	G			
X24LC04S	512 x 8	•										†	CMOS	Standard
X24LC04SI	512 x 8	•										I	CMOS	Standard
X24LC04P	512 x 8		•									†	CMOS	Standard
X24LC04PI	512 x 8		•									I	CMOS	Standard
X24LC04D	512 x 8			•								†	CMOS	Standard
X24LC04DI	512 x 8			•								I	CMOS	Standard

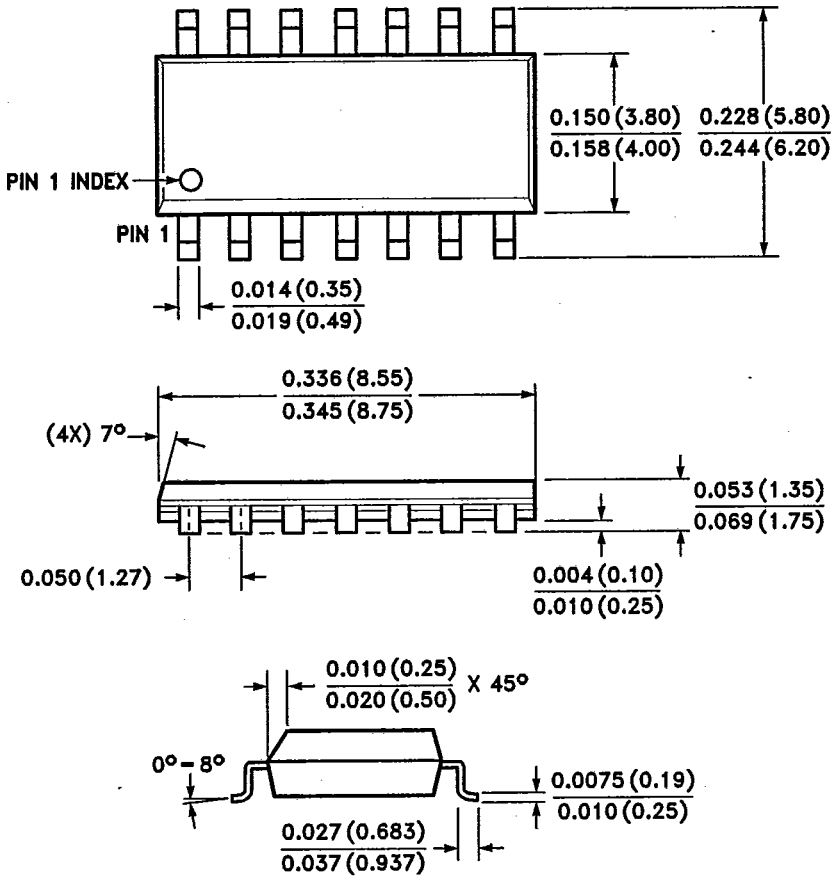
Key:

† = Blank = Commercial = 0°C to +70°C
I = Industrial = −40°C to +85°C
M = Military = −55°C to +125°C

S = 14-Lead Plastic Small Outline Gull Wing
P = 8-Lead Plastic DIP
D = 8-Lead Cerdip
C = Side Braze
F1 = Ceramic Flat Pack for X2864A, X2864B, X2864H and X28C64
F2 = Ceramic Flat Pack for X28C256 and X28C256B
K = Ceramic Pin Grid Array
J = J-Hook Plastic Leaded Chip Carrier
E = Ceramic Leadless Chip Carrier (Solder Seal)
G = Ceramic Leadless Chip Carrier (Glass Frit Seal)

PACKAGING INFORMATION

14-LEAD PLASTIC SMALL OUTLINE GULL WING PACKAGE TYPE S



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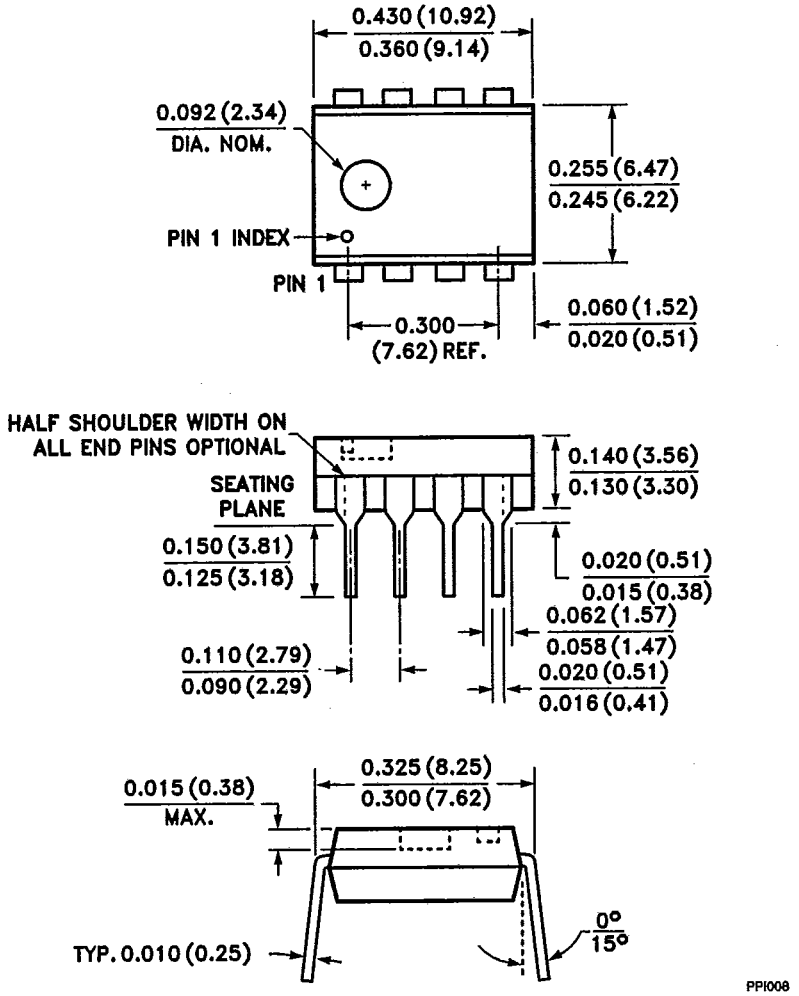
NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)

PACKAGING INFORMATION

8-LEAD PLASTIC DUAL IN-LINE PACKAGE TYPE P



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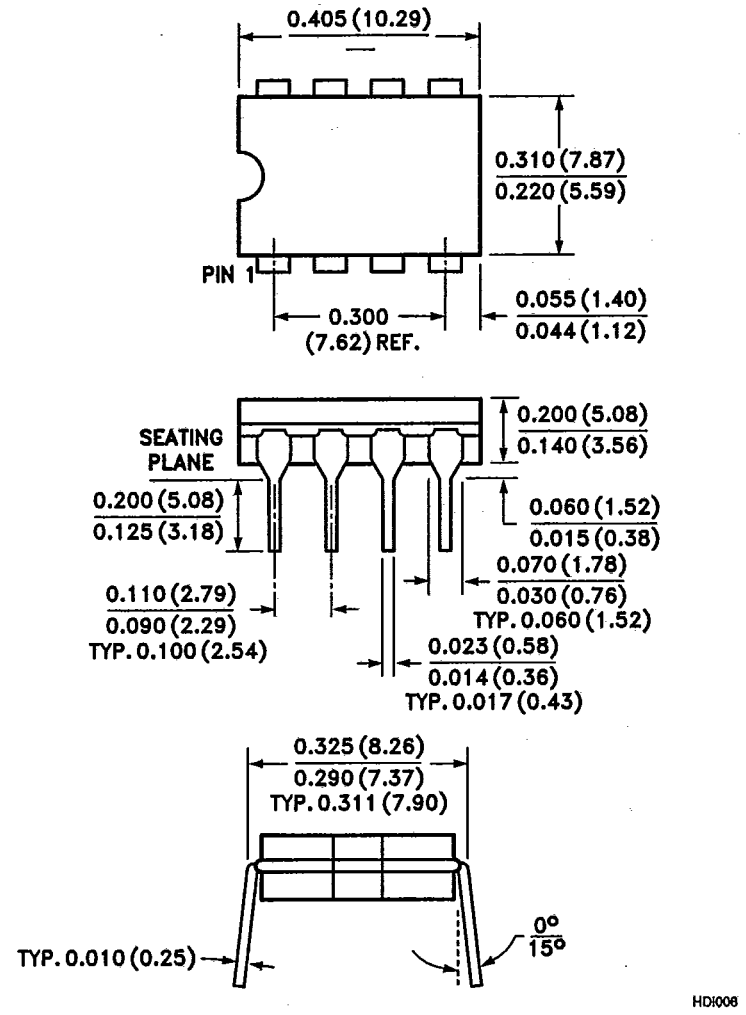
NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)

PACKAGING INFORMATION

8-LEAD HERMETIC DUAL IN-LINE PACKAGE TYPE D



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