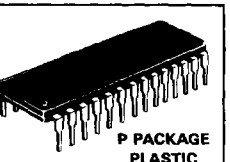
MCM6206

Advance Information

32K x 8 Bit Fast Static Random Access Memory



P PACKAGE
PLASTIC
CASE 710

J PACKAGE
PLASTIC
CASE 810

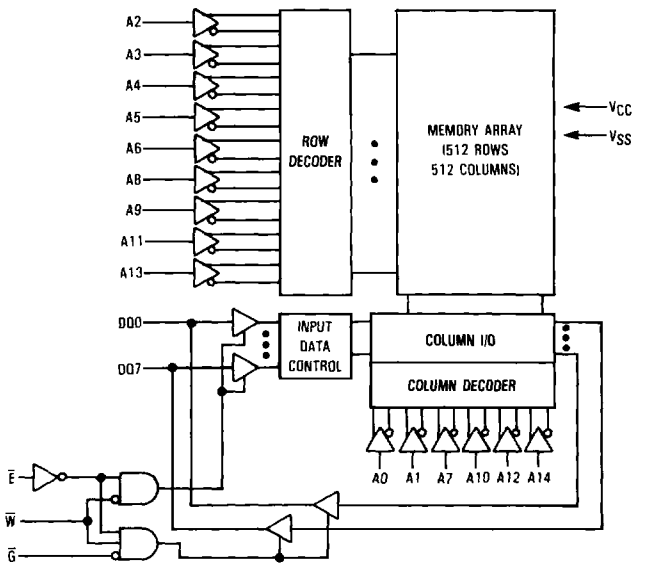
The MCM6206 is a 262,144 bit static random access memory organized as 32,768 words of 8 bits, fabricated using Motorola's high-performance silicon-gate CMOS technology. Static design eliminates the need for external clocks or timing strobes, while CMOS circuitry reduces power consumption and provides for greater reliability.

Chip enable ($\overline{E}$) controls the power-down feature. It is not a clock but rather a chip control that affects power consumption. In less than a cycle time after $\overline{E}$ goes high, the part automatically reduces its power requirements and remains in this low-power standby mode as long as $\overline{E}$ remains high. This feature provides significant system-level power savings. Another control feature, output enable ($\overline{G}$) allows access to the memory contents as fast as 15 ns (MCM6206-35).

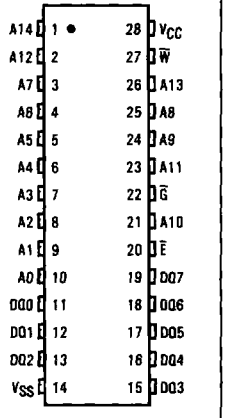
The MCM6206 is packaged in a 600 mil, 28 pin plastic dual-in-line package or a 28 lead 400 mil plastic SOJ package with the JEDEC standard pinout.

- Single 5 V Supply, ±10%
- Fully Static—No Clock or Timing Strobes Necessary
- Fast Access Time—35 or 45 ns (Maximum)
- Low Power Dissipation
- Two Chip Controls; $\overline{E}$ for Automatic Power Down
  $\overline{G}$ for Fast Access to Data
- Three State Outputs
- Fully TTL Compatible

BLOCK DIAGRAM



PIN ASSIGNMENT



PIN NAMES	
A0-A14	Address
$\overline{W}$	Write Enable
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
DQ0-DQ7	Data Input/Output
V_{CC}	+5 V Power Supply
V_{SS}	Ground

This document contains information on a new product. Specifications and information herein are subject to change without notice.

TRUTH TABLE

$\overline{E}$	$\overline{G}$	$\overline{W}$	Mode	Supply Current	I/O Pin
H	X	X	Not Selected	I_{SB}	High Z
L	H	H	Output Disabled	I_{CC}	High Z
L	L	H	Read	I_{CC}	D_{out}
L	X	L	Write	I_{CC}	D_{in}

X—Don't Care

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	−0.5 to +7.0	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	−0.5 to V_{CC} +0.5	V
Output Current (per I/O)	I_{out}	±20	mA
Power Dissipation (T_A = 25°C)	P_D	1.0	W
Temperature Under Bias	T_{bias}	−10 to +85	°C
Operating Temperature	T_A	0 to +70	°C
Storage Temperature—Plastic	T_{stg}	−55 to +125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 ±10%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.2	–	V_{CC} + 0.3	V
Input Low Voltage	V_{IL}	−0.3*	–	0.8	V

*V_{IL} (min) = −0.3 V dc; V_{IL} (min) = −3.0 V ac (pulse width ≤ 20 ns)

DC CHARACTERISTICS

Parameter		Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})		$I_{lkg(I)}$	–	±1.0	μA
Output Leakage Current ($\overline{E}$ = V_{IH}, or $\overline{G}$ = V_{IH}, V_{out} = 0 to 5.5 V)		$I_{lkg(O)}$	–	±1.0	μA
Power Supply Current	(t_{AVAV} = 35 ns)	I_{CC}	–	120	mA
($\overline{E}$ = V_{IL}, I_{out} = 0)	(t_{AVAV} = 45 ns)	I_{CC}	–	110	mA
Standby Current ($\overline{E}$ = V_{IH}) (TTL Levels)		I_{SB1}	–	20	mA
Standby Current ($\overline{E}$ ≥ V_{CC} − 0.2 V) (CMOS Levels)		I_{SB2}	–	15	mA
Output Low Voltage (I_{OL} = 8.0 mA)		V_{OL}	–	0.4	V
Output High Voltage (I_{OH} = −4.0 mA)		V_{OH}	2.4	–	V

CAPACITANCE (f = 1.0 MHz, T_A = 25°C, periodically sampled and not 100% tested.)

Characteristic	Symbol	Max	Unit
Input Capacitance	C_{in}	6	pF
I/O Capacitance	$C_{I/O}$	8	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5 V ±10%, T_A = 0 to 70°C, Unless Otherwise Noted)

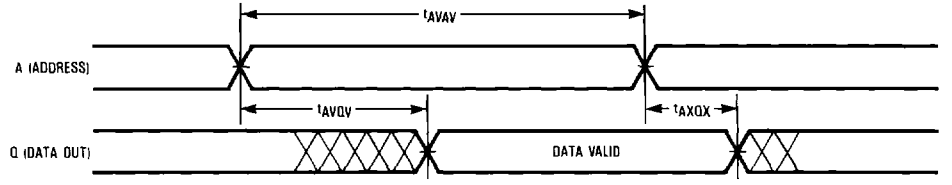
Input Pulse Levels . . . . . 0 to 3.0 V
Input Rise/Fall Time . . . . . 5 ns
Input Timing Measurement Reference Levels . . . . . 1.5 V
Output Timing Measurement Reference Levels . . . . . 1.5 V
Output Load . . . . . See Figure 1

READ CYCLE 1 & 2 (See Note 1)

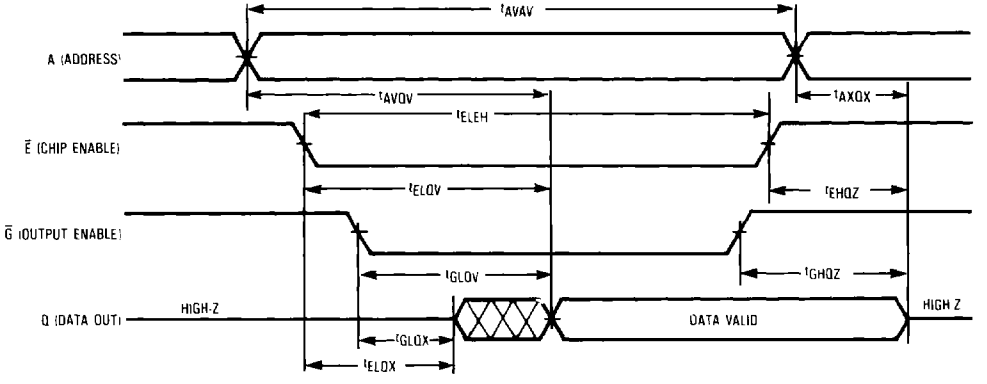
Parameter	Symbol	Alt Symbol	MCM6206-35		MCM6206-45		Unit	Notes
			Min	Max	Min	Max		
Read Cycle Time	t_{AVAV}	t_{RC}	35	–	45	–	ns	–
Address Access Time	t_{AVQV}	t_{AA}	–	35	–	45	ns	–
$\overline{E}$ Access Time	t_{ELQV}	t_{AC}	–	35	–	45	ns	–
$\overline{G}$ Access Time	t_{GLQV}	t_{OE}	–	15	–	20	ns	–
Enable Low to Enable High	t_{ELEH}	t_{CW}	35	–	45	–	ns	–
Output Hold from Address Change	t_{AXQX}	t_{OH}	5	–	5	–	ns	2
Chip Enable to Output Low-Z	t_{ELQX}	t_{CLZ}	10	–	10	–	ns	2, 3
Output Enable to Output Low-Z	t_{GLQX}	t_{OLZ}	0	–	0	–	ns	2, 3
Chip Enable to Output High-Z	t_{EHQZ}	t_{CHZ}	0	20	0	20	ns	2, 3
Output Enable to Output High-Z	t_{GHQZ}	t_{OHZ}	0	20	0	20	ns	2, 3

NOTES:
1. $\overline{W}$ is high at all times for read cycles.
2. All high-Z and low-Z parameters are considered in a high or low impedance state when the output has made a 500 mV transition from the previous steady state voltage.
3. These parameters are periodically sampled and not 100% tested.

READ CYCLE 1 ($\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$)



READ CYCLE 2



WRITE CYCLE 1 & 2 (See Note 1)

Parameter	Symbol	Alt Symbol	MCM6206-35		MCM6206-45		Unit	Notes
			Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	35	–	45	–	ns	–
Address Setup to Write Low Address Setup to Enable Low	t_{AVWL} t_{AVEL}	t_{AS}	0	–	0	–	ns	2
Address Valid to Write High Address Valid to Enable High	t_{AVWH} t_{AVEH}	t_{AW}	25	–	35	–	ns	–
Data Valid to Write High Data Valid to Enable High	t_{DVWH} t_{DVEH}	t_{DW}	15	–	20	–	ns	–
Data Hold From Write High Data Hold From Enable High	t_{WHDX} t_{EHDX}	t_{DH}	0	–	0	–	ns	–
Write Recovery Time Enable Recovery Time	t_{WHAX} t_{EHAX}	t_{WR}	0	–	0	–	ns	2
Chip Enable to End of Write Enable Low to Enable High	t_{ELWH} t_{ELEH}	t_{CW}	25	–	35	–	ns	1
Write Pulse Width	t_{WLWH}	t_{WP}	25	–	30	–	ns	3
Write Low to Output High-Z	t_{WLQZ}	t_{WHZ}	0	20	0	20	ns	4, 5
Write High to Output Low-Z	t_{WHQX}	t_{WLZ}	5	–	5	–	ns	4, 5

NOTES:
1. A write cycle starts at the latest transition of a low $\overline{E}$ or low $\overline{W}$. A write cycle ends at the earliest transition of a high $\overline{E}$ or high $\overline{W}$.
2. $\overline{W}$ must be high during all address transitions.
3. If $\overline{G}$ is enabled, allow an additional 15 ns t_{WLWH} to avoid bus contention.
4. *All high-Z and low-Z parameters are considered in a high or low impedance state when* the output has made a 500 mV transition from the previous steady state voltage.
5. These parameters are periodically sampled and not 100% tested.

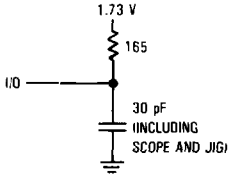
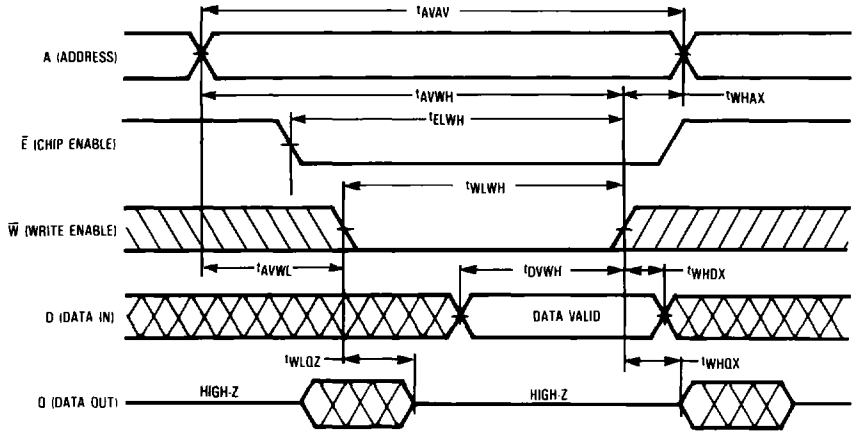
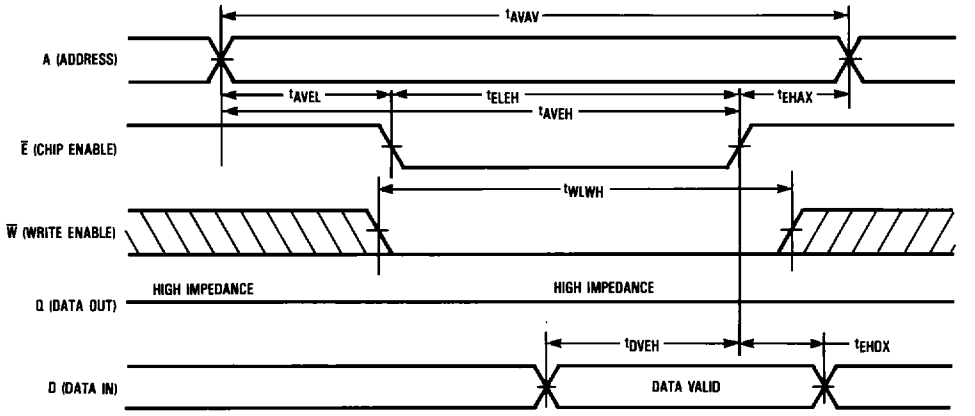


Figure 1. Test Load

WRITE CYCLE 1 ($\overline{W}$ Controlled)



WRITE CYCLE 2 ($\overline{E}$ Controlled)



ORDERING INFORMATION
(Order by Full Part Number)

MCM 6206 X XX XX

- MCM — Motorola Memory Prefix
- 6206 — Part Number
- X — Package (P = Plastic DIP, J = Plastic SOJ)
- XX — Speed (35 = 35 ns, 45 = 45 ns)
- XX — Shipping Method (R2 = Tape & Reel, Blank = Rails)

Full Part Numbers — MCM6206P35, MCM6206P45, MCM6206J35, MCM6206J45, MCM6206J35R2, MCM6206J45R2