DR-11525

16-BIT HIGH FREQUENCY HYBRID DIGITAL-TO-RESOLVER CONVERTER

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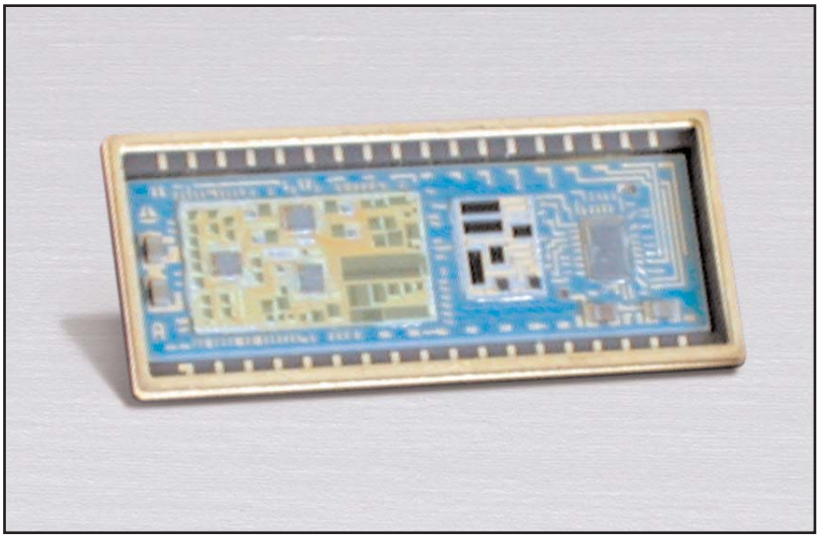

FEATURES

- Accuracy Up to 1 Minute
- Operational Up to 10 kHz
- 2 Vrms, 6.81 Vrms, 11.8 V_{L-L}, or Scalable Resolver Outputs
- 2 mA rms Output
- 16-Bit Resolution
- 8-Bit/2-Byte Double Buffered Transparent Latches
- DC-Coupled Reference Accepts Any Waveform
- High-Rel CMOS D/R Chip
- No +5 V Supply Required

DESCRIPTION

The DR-11525 is a versatile multiplying Digital-to-Resolver converter. The digital input represents an angle, and the output is resolver type, SIN/COS. The reference input will accept any waveform, even a sawtooth for CRT drive. Because the reference is DC-coupled to the output, the DR-11525 can be used as: a Digital-to-Resolver converter using a sinusoidal reference as an input; a Digital-to-SIN/COS DC converter using a DC reference; a polar-to-rectangular converter using a reference input proportional to the radius vector; or a rotating cartwheel sweep generator for PPI displays using a sawtooth reference.

The DR-11525 is a complete Digital-to-Resolver (D/R) converter in one hybrid module. The DR-11525 circuit design allows for higher accuracy and reduces the output scale factor variation so that the output can drive displays directly. The output line-to-ground voltage can be scaled by external resistors. The DR-11525 also includes high AC and DC common-mode rejection at the reference input.

APPLICATIONS

Because of its high reliability, small size and low power consumption, the hybrid DR-11525 is ideal for the most stringent and severe industrial and military ground or avionics applications. All units are available with MIL-PRF-38534 processing as a standard option.

Among the many possible applications are computer-based systems in which digital angle information is processed, such as synchro/resolver simulators, flight trainers, flight instrumentation, fire control systems, IR, and radar and navigation systems. In addition, the DR-11525 is ideal for motor and robotic control test systems.

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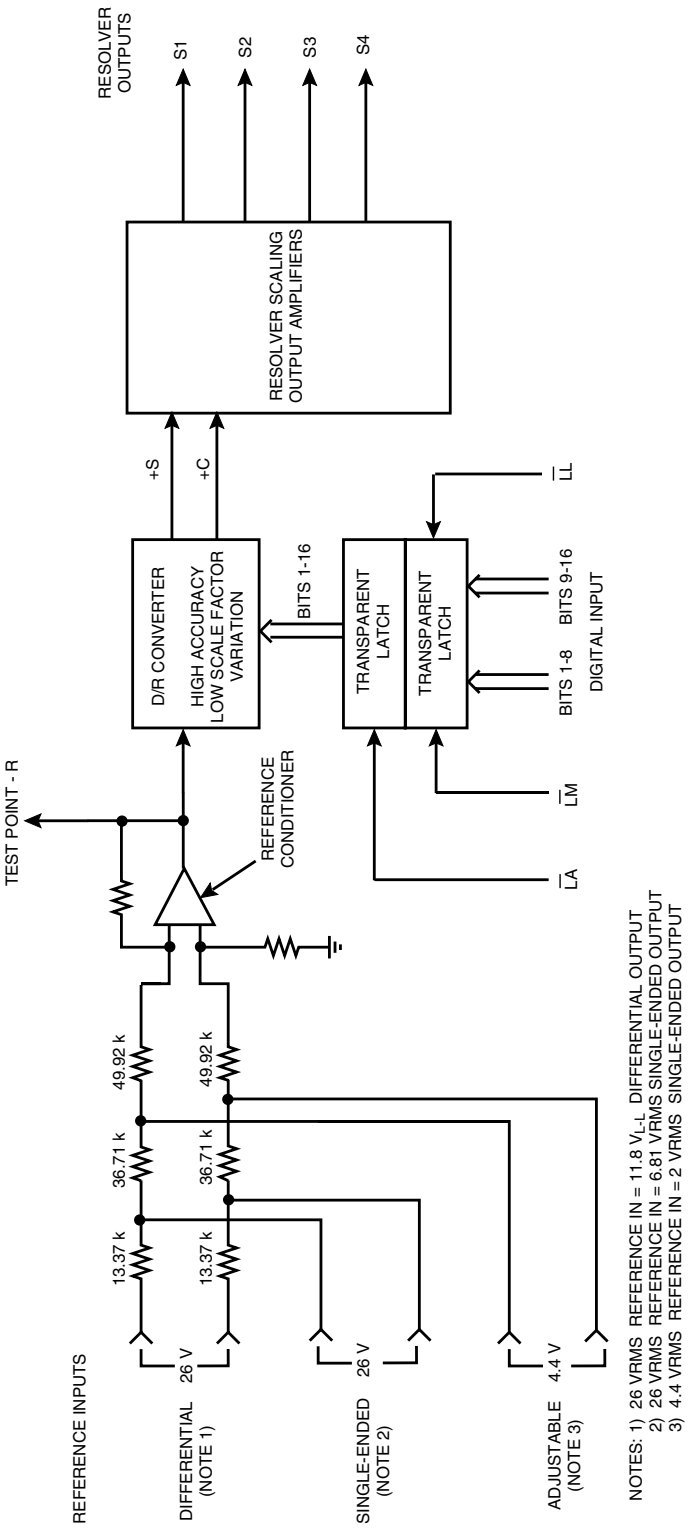


FIGURE 1. DR-11525 BLOCK DIAGRAM

TABLE 1. DR-11525 SPECIFICATIONS

Apply over temperature range, power supply range, reference voltage and frequency range, and 10% harmonic distortion in the reference.

PARAMETER	UNIT	VALUE	
RESOLUTION	Bits	16	
ACCURACY AND DYNAMICS			
Output Accuracy	Minutes	4 to 1 min. (See Ordering information) 1 minute part: 1 min up to 1 kHz, 1.5 min for 1 to 5 kHz, and 3 min for 5 to 10 kHz (guaranteed by design - tested at 5 kHz)	
Differential Linearity	LSB	±1 max	
Output Settling Time	µsec	Less than 20 for any digital step change	
DIGITAL INPUT			
Logic Type		Natural binary angle, parallel positive logic CMOS and TTL compatible. Inputs are CMOS transient protected. Logic 0 = 0 to +1 V Logic 1 = +2.2V to +5V	
Load Current	µA	20 max to GND (bits 1-16) 20 max to +5V ($\overline{LL}$, $\overline{LM}$, $\overline{LA}$) See Timing Diagram (FIGURE 2.).	
REFERENCE INPUT			
Type		Three differential solid-state inputs: two for standard 26V, one programmable.	
Frequency Range	Hz	DC to 10k	
Standard Input Voltage (Note 1)			
RH3-RL3	V	4.4	
RH2-RL2	V	26	
RH-RL	V	26	
INPUT IMPEDANCE			
Single-Ended: RH-gnd	k ohm	100 ±0.5%	
Differential: RH to RL	k ohm	200 ±0.5%	
ANALOG OUTPUT			
Type		Resolver	
Output Current	mA rms	2 max	
Standard Output Voltage (Note 2)		(Tracks Reference Input Voltage)	
RH-RL	$Vrms_{L-L}$	11.8 nominal	
RH2-RL2	Vrms	6.81 (single ended)	
RH3-RL3	Vrms	2.0 nominal (single ended)	
Transform. Ratio Tol.	%	±0.5 max	
Scale Factor Variation	%	±0.1 max	
DC Offset (Single ended)	mV	±15 max Varies with input angle.	
POWER SUPPLIES			
Voltage	V	+15 ±5%	-15 ±5%
Max volt. w/o damage		**+18V**	**-18V**
Current or Impedance	mAmax	35+ load current	35+ load current
TEMPERATURE RANGES (CASE)			
Operation			
-1 Option	°C	-55 to +125	
-2 Option	°C	-40 to +85	
-3 Option	°C	0 to +70	
Storage	°C	-55 to +135	
PHYSICAL CHARACTERISTICS			
Package Type		36-pin DDIP	
Size	in.(mm)	0.78 x 1.9 x 0.21 (19.7 x 48.1 x 5.3)	
Weight	oz (g)	0.85 (24)	

Notes: 1) Maximum reference input RH-RL = 26V +10%; RH2-RL2 = 26V +10%; RH3-RL3 = 16.4V. (2) Minimum voltage output (when using scalable reference input) is 1V differential or 0.5V single ended. (3) Differential is line-to-line (L-L); single ended is line-to-ground (L-gnd).

INTRODUCTION

As shown in FIGURE 1, the signal conversion in the DR-11525 is performed by a high-accuracy digital-to-resolver converter whose sin and cos outputs have a low scale factor variation as a function of the digital input angle. This resolver output is amplified by scaling amplifiers for resolver output. The output line currents can be 2 mA rms max, which is sufficient for driving R/D converters, solid-state control transformers, and displays. Output power amplifiers will be required, however, for driving electromechanical devices such as synchros and resolvers.

The reference conditioner has a differential input with high AC and DC common mode rejection, so that a reference isolation transformer will seldom be required. There are three sets of reference inputs which provide three different input/output ratios. The RH- RL input provides a 0.45 ratio between the reference input and the signal output and is designed to provide 11.8 VL-L differential output for a 26 Vrms reference input. The RH2-RL2 input provides a 0.52 ratio between the reference input and the signal output and is designed to provide a 6.81 Vrms single-ended output for a 26 Vrms reference input. The RH3-RL3 input provides a 0.91 ratio between the reference input and the signal output and is designed to provide a 2 Vrms single-ended output for a 4.4 Vrms reference input. Series resistors can be added to accommodate higher reference levels or to reduce the output level.

TABLE 2. ANGLES IN DEGREES CROSS REFERENCED TO A 16-BIT DIGITAL WORD

DEGREES (HEX)	16 BIT DIGITAL WORD (Φ) (1 = MSB, 16 = LSB)															
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
0° (0000)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
15° (0AAB)	0	0	0	0	1	0	1	0	1	0	1	0	1	0	1	1
30° (1555)	0	0	0	1	0	1	0	1	0	1	0	1	0	1	0	1
45° (2000)	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
60° (2AAB)	0	0	1	0	1	0	1	0	1	0	1	0	1	0	1	1
75° (3666)	0	0	1	1	0	1	0	1	0	1	0	1	0	1	0	1
90° (4000)	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
120° (5555)	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
135° (6000)	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0
180° (8000)	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
240° (AAAB)	1	0	1	0	1	0	1	0	0	0	1	0	1	0	1	1
270° (C000)	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
285° (CAAB)	1	1	0	0	1	0	1	0	1	0	0	0	1	0	1	1
300° (D555)	1	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
315° (E000)	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0
330° (EAAB)	1	1	1	0	1	0	1	0	1	0	1	0	1	0	1	1
345° (F555)	1	1	1	1	0	1	0	1	0	1	0	1	0	1	0	1
359° (FFFF)	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

POWER SUPPLY CYCLING

Power supply cycling of the DDC converter should follow the guidelines below to avoid any potential problems. Strictly maintain proper sequencing of supplies and signals per typical CMOS circuit guidelines:

- Apply power supplies first (+15, -15V and ground).
- Apply digital control signals next.
- Apply analog signals last.

The reverse sequence should be followed during power down of the circuit.

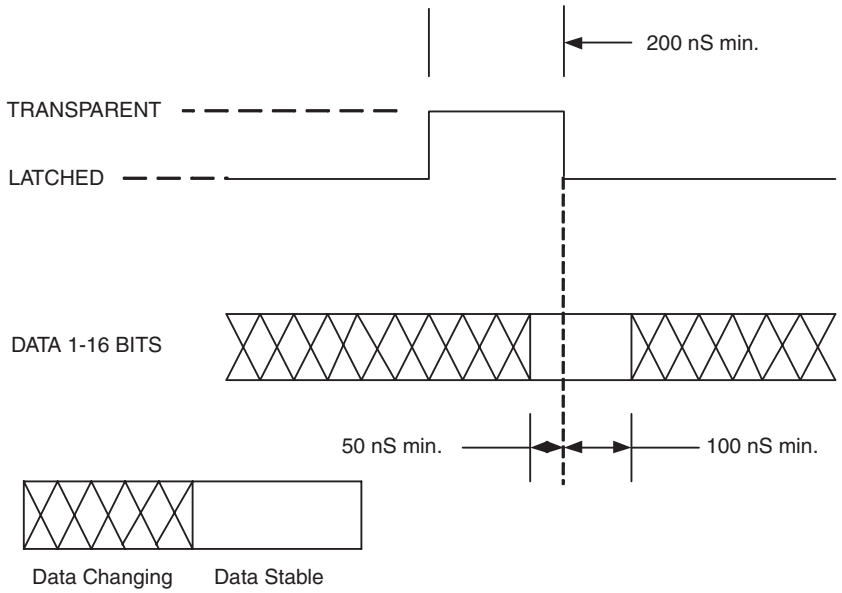


FIGURE 2A. $\overline{LL}$, $\overline{LM}$, $\overline{LA}$ TIMING DIAGRAMS (16 BIT)

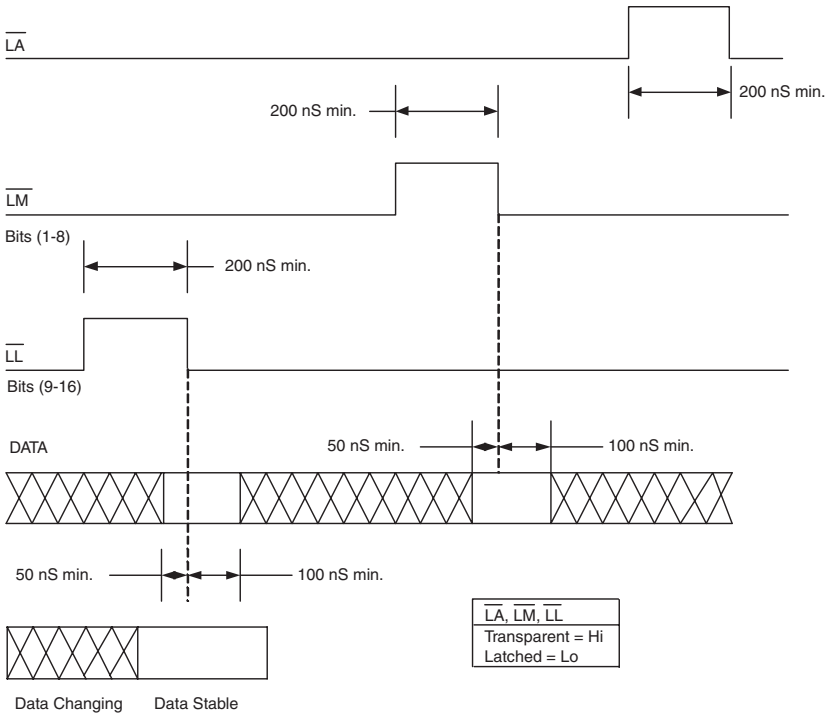


FIGURE 2B. $\overline{LL}$, $\overline{LM}$, $\overline{LA}$ TIMING DIAGRAMS (8 BIT)

The reference conditioner output -R is intended for test purposes. For a 26 Vrms nominal input to RH, RL, -R should be 5.9 Vrms.

The timing relationship of $\overline{LL}$, $\overline{LM}$, and $\overline{LA}$ is shown in FIGURE 2 as a design reference.

OUTPUT SCALING AND REF. LEVEL ADJUSTMENT

The DR-11525 operates like a multiplying D/A converter in that the voltage of each output line is directly proportional to the reference voltage. See FIGURE 3.

The magnitude of the resistors, R', in ohms is calculated as follows:

*Note: For RH2, RL2 and RH3, RL3: Vout(single-ended) = 1/2 $Vout_{L-L}$.

For RH-RL: $\frac{Vout_{L-L}}{Vin} = \frac{45.38k}{100k + R'}$

*For RH2-RL2: $\frac{Vout_{L-L}}{Vin} = \frac{45.38k}{86.63k + R'}$

*For RH3-RL3: $\frac{Vout_{L-L}}{Vin} = \frac{45.38k}{49.92k + R'}$

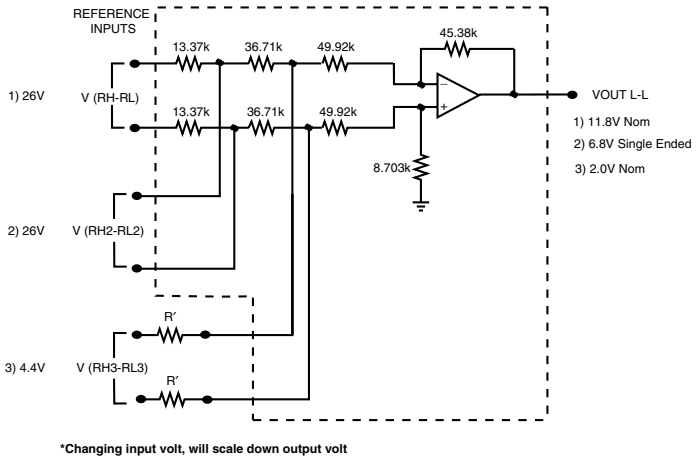


FIGURE 3. REFERENCE LEVEL ADJUSTMENT

OUTPUT PHASING AND OUTPUT SCALE FACTOR

The analog output signals have the following phasing:

Resolver output:

S3—S1 = (RH - RL)Ao(1 + A(θ)) sin θ

S2—S4 = (RH - RL)Ao(1 + A(θ)) cos θ

The output amplifiers simultaneously track reference voltage fluctuations because they are proportional to (RH - RL). The transformation ratio Ao is 11.8/26 for 11.8 $Vrms_{L-L}$ output. The maximum variation in Ao from all causes is ± 0.2%. The term A(θ) represents the variation of the amplitude with the digital signal input angle. A(θ), which is called the scale factor variation, is a smooth function of (θ) without discontinuities and is less than ±0.1% for all values of (θ). Therefore, the analog output can vary as much as ±0.3% due to the transformation ratio and scale factor variations.

Because the amplitude factor (RH - RL)Ao(1 + A(θ)) varies simultaneously on all output lines, it will not be a source of error when the DR-11525 is to drive a ratiometric system such as a synchro or resolver. However, if the outputs are used independently, as in x-y plotters, the amplitude variations must be taken into account.

TABLE 3. PIN CONNECTION TABLE

PIN	NAME	PIN	NAME	PIN	NAME
1	NC	13	Bit 13	25	Bit 1 (MSB)
2	+15V	14	Bit 12	26	Bit 15
3	GND	15	Bit 11	27	Bit 16 (LSB)
4	-15V	16	Bit 10	28	$\overline{LM}$
5	RH2 (6.81V)	17	Bit 9	29	$\overline{LL}$
6	RL2 (6.81V)	18	Bit 8	30	$\overline{LA}$
7	-R	19	Bit 7	31	S4 (-COS)
8	RL (11.8V)	20	Bit 6	32	S1 (-SIN)
9	RL3 (2V)	21	Bit 5	33	NC
10	RH (11.8V)	22	Bit 4	34	NC
11	RH3 (2V)	23	Bit 3	35	S3 (+SIN)
12	Bit 14	24	Bit 2	36	S2 (+COS)

Notes:
1. -R (Pin 7) can be used for test purposes to detect whether a reference signal is present. See block diagram.
2. Functions LL, LA, and LM may be left unconnected when not used.
3. External scaling resistor pin 11 RH3 output pins (31, 32, 35, 36).
4. RH and RL (pins 10, 8) 26 V reference with differential outputs on pins 35, 36, 32, 31.
5. RH2 and RL2 (pins 5, 6) 26 V reference with single-ended output on pins 35, 36.
6. RH3 and RL3 (pins 11, 9) 4.4 V reference with single-ended outputs on pins 35, 36.

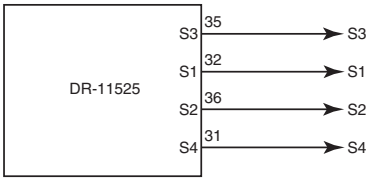


FIGURE 4. DIFFERENTIAL RESOLVER OUTPUT

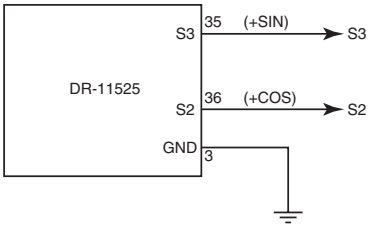
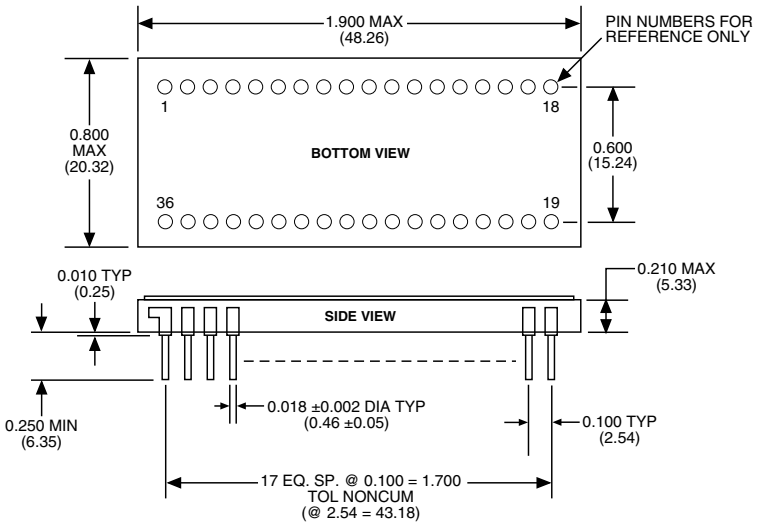
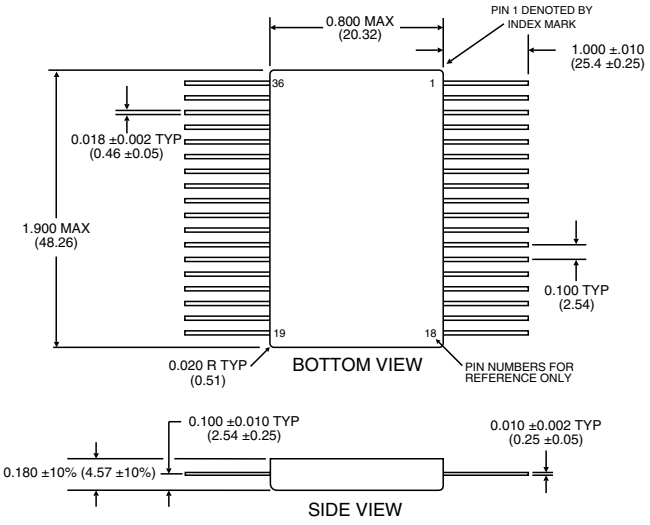


FIGURE 5. SINGLE-ENDED RESOLVER OUTPUT



Notes:
1. Dimensions shown are in inches (millimeters).
2. Lead identification numbers are for reference only.
3. Lead cluster shall be centered within ±0.005 of outline dimensions.
Lead spacing dimensions apply only at seating plane.
4. Pin material meets solderability requirements of MIL-STD-202E,
Method 208C.

FIGURE 6. DR-11525 MECHANICAL OUTLINE
36-PIN DDIP (CERAMIC)



Notes:
1. Dimensions shown are in inches (millimeters).
2. Lead identification numbers are for reference only.
3. Lead cluster shall be centered within ±0.005 of outline dimensions.
Lead spacing dimensions apply only at seating plane.
4. Pin material meets solderability requirements of MIL-STD-202E,
Method 208C.

FIGURE 7. DR-11525 MECHANICAL OUTLINE
36-PIN FLAT PACK (CERAMIC)

ORDERING INFORMATION

DR-11525D X-XXXX

Supplemental Process Requirements:
- S = Pre-Cap Source Inspection
- L = Pull Test
- Q = Pull Test and Pre-Cap Inspection
- K = One Lot Date Code
- W = One Lot Date Code and PreCap Source
- Y = One Lot Date Code and 100% Pull Test
- Z = One Lot Date Code, PreCap Source and 100% Pull Test
- Blank = None of the Above

Accuracy:
- 3 = 4 minutes + 1 LSB
- 4 = 2 minutes + 1 LSB
- 5 = 1 minute + 1 LSB*

Reliability:
- 0 = Standard DDC Processing, no Burn-In (See table below.)
- 1 = MIL-PRF-38534 Compliant
- 2 = B**
- 3 = MIL-PRF-38534 Compliant with PIND Testing
- 4 = MIL-PRF-38534 Compliant with Solder Dip
- 5 = MIL-PRF-38534 Compliant with PIND Testing and Solder Dip
- 6 = B** with PIND Testing
- 7 = B** with Solder Dip
- 8 = B** with PIND Testing and Solder Dip
- 9 = Standard DDC Processing with Solder Dip, no Burn-In (See table below.)

Temperature Grade/Data Requirements:
- 1 = -55 to +125°C (Case)
- 2 = -40 to +85°C (Case)
- 3 = 0 to +70°C (Case)
- 4 = -55 to +125°C (Case) + Variables Data
- 5 = -40 to +85°C (Case) + Variables Data
- 8 = 0 to +70°C (Case) + Variables Data

Options:
- X = NONE

Package:
- D = DIP Package
- F = Flat Package

* Consult factory for availability of ±1 minute parts.

** Standard DDC Processing with burn-in and full temperature test (See table below).

STANDARD DDC PROCESSING FOR HYBRID AND MONOLITHIC HERMETIC PRODUCTS

TEST	MIL-STD-883	
	METHOD(S)	CONDITION(S)
INSPECTION	2009, 2010, 2017, and 2032	—
SEAL	1014	A and C
TEMPERATURE CYCLE	1010	C
CONSTANT ACCELERATION	2001	3000g
BURN-IN	1015 (note 1), 1030 (note 2)	TABLE 1

Notes:
1. For Process Requirement "B*" (refer to ordering information), devices may be non-compliant with MIL-STD-883, Test Method 1015, Paragraph 3.2. Contact factory for details.
2. When applicable.

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