1.1 Scope.

This specification covers the detail requirements for a monolithic 12-bit, 2 MHz A/D converter.

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number
−1	AD671SD-500/883B
−2	AD671SD-750/883B

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline:

Package	Description
D-24A	24-Lead Side Brazed Ceramic DIP (Single Width)

1.3 Absolute Maximum Ratings. (T_A = +25°C unless otherwise noted)

V_{CC} to ACOM ..... −0.5 V to +6.5 V
V_{EE} to ACOM ..... −6.5 V to +0.5 V
V_{LOGIC} to DCOM ..... −0.5 V to +6.5 V
ACOM to DCOM ..... −1 V to +1 V
V_{CC} to V_{LOGIC} ..... −6.5 V to +6.5 V
ENCODE to DCOM ..... −0.5 V to V_{LOGIC} + 0.5 V
REF IN to ACOM ..... −0.5 V to V_{CC} + 0.5 V
AIN, BPO/UPO to ACOM ..... −6.5 V to +11 V
Power Dissipation ..... 1000 mW
Storage Temperature Range ..... −65°C to +150°C
Lead Temperature (Soldering 10 sec) ..... +300°C

1.5 Thermal Characteristics.

Thermal Resistance θ_{JC} = 25°C/W
θ_{JA} = 80°C/W

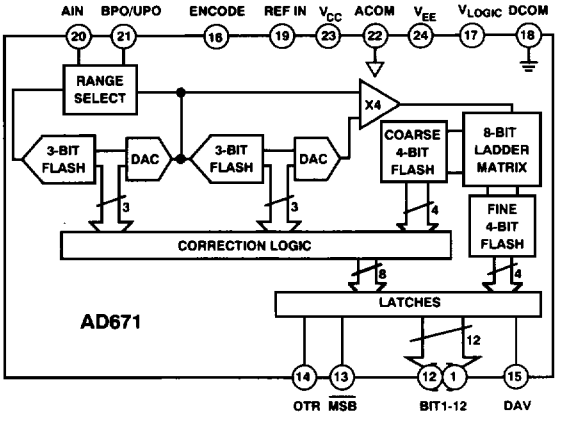
AD671—SPECIFICATIONS

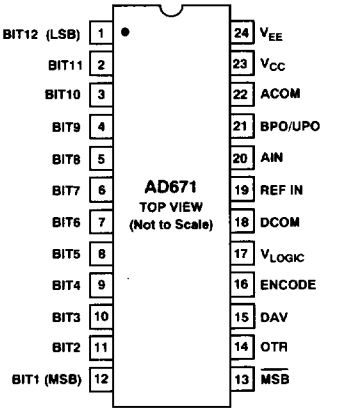
Table 1.

Test	Symbol	Device	Design Limit @ +25°C	Sub Group 1	Sub Group 2, 3	Test Condition	Units
Resolution	RES	−1, 2	12	12	12		Bits
Integral Nonlinearity	INL	−1	4	4	4	All Codes Histogram Test	±LSB
		−2	2.5	2.5	2.5		
Differential Nonlinearity	DNL	−1	10	10	10	All Codes Histogram Test	Bits
		−2	11	11	11		
Unipolar Offset Error	V_{OSE}	−1, 2	4	4		5 V, 10 V Span	±LSB
Unipolar Offset Drift	TC_{VOS}	−1, 2	10		10	5 V, 10 V Span	±ppm/°C
Gain Error	A_E	−1, 2	0.25	0.25		Unipolar & Bipolar	% FSR
Gain Drift	TC_A	−1, 2	20		20	Unipolar & Bipolar	±ppm/°C
Bipolar Zero	B_{POE}	−1, 2	10	10		±5 V Mode	±LSB
Bipolar Zero Drift	TC_{BPO}	−1, 2	15		15	±5 V Mode	±ppm/°C
Analog Input Ranges	V_{IN}	−1, 2	5	5	5		V Unipolar
			10	10	10		
			5	5	5		±V Bipolar
Input Resistance (5 V Range)	R_{IN5}	−1, 2	0.5				kΩ min
			1				kΩ max
Input Resistance (10 V Range)	R_{IN10}	−1, 2	1				kΩ min
			2				kΩ max
Reference Input Resistance	R_{REF}	−1, 2	2.4				kΩ min
			4.7				kΩ max
Input Capacitance	C_{IN}	−1, 2	10				pF
Power Dissipation	P_D	−1, 2	621	621	621		mW
Power Supply Current	I_{CC}	−1, 2	56	56	56	Tested Under Static Conditions	mA max
	I_{EE}		56	56	56		−mA min
	I_{DD}		6	6	6		mA max
Operating Voltage Range	V_{CC}	−1, 2	4.75 5.25				V min V max
	V_{EE}		4.75 5.25				−V max −V min
	V_{DD}		4.5 5.5				V min V max
PSRR	V_{CC}	−1, 2	1	1	1	Full-Scale Change Measured	±LSB
	V_{EE}		1	1	1		
	V_{DD}		1	1	1		
Input Logic Levels	V_{IH}	−1, 2	2	2	2	Encode Input	V min
	V_{IL}		0.8	0.8	0.8		V max
Input Logic Currents	I_{IH}	−1, 2	10	10	10	Encode Input	±μA
	I_{IL}		10	10	10		
Logic Outputs	V_{OH}	−1, 2	2.4	2.4	2.4	I_{OH} = 500 μA	V min
	V_{OL}		0.4	0.4	0.4	I_{OL} = −1.6 mA	V max
	I_{OH}		500	500	500		μA
	I_{OL}		1.6	1.6	1.6		−mA

Test	Symbol	Device	Design Limit @ +25°C	Sub Group 9	Sub Group 10, 11	Test Condition	Units
Conversion Time	T_{CONV}	−1	500	500	500		ns max
		−2	750	750	750		
Encode Width High (Short Encode)	t_{ENC}	−1, 2	20			See Figure 1a	ns min
		−1	30	30	30		ns max
		−2	50	50	50		
Encode Width Low (Long Encode)	t_{ENCL}	−1, 2	20			See Figure 1b	ns min
DAV Width	t_{DAV}	−1, 2	75	75	75		ns min
		−1	200	200	200		ns max
		−2	300	300	300		
Encode Falling Edge Delay	t_F	−1, 2	0				ns min
Start New Conversion Delay	t_R	−1, 2	0				ns min
Data Update Delay from DAV ↓	t_{DD}	−1, 2	20	20	20		ns min
Data Update Delay from DAV ↑	t_{SS}	−1, 2	20	20	20		ns min

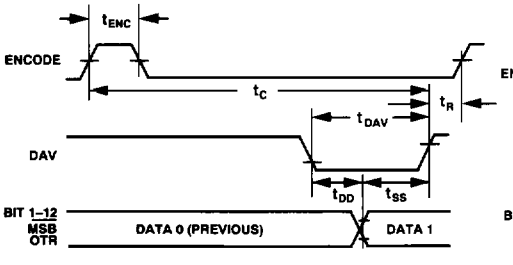
3.2.1 Functional Block Diagram and Terminal Assignments



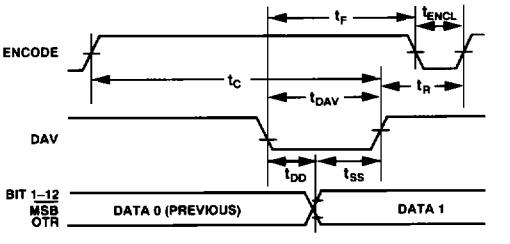


3.2.4 Microcircuit Technology Group

This circuit is covered by technology group (93).



a. Encode Pulse HIGH



b. Encode Pulse LOW

Figure 1. AD671 Timing Diagram

4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).