REVISIONS			
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	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

STANDARDIZED MILITARY DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

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DRAWING APPROVAL DATE
91-10-02

REVISION LEVEL

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUITS, LINEAR, CMOS, 8-BIT, A/D CONVERTER WITH TRACK/HOLD, MONOLITHIC SILICON

SIZE	CAGE CODE	5962-89518
A	67268	

SHEET 1 OF 15

1

DESC FORM 193
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Use previous edition until exhausted.

5962-E049

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

1. SCOPE

1.1 Scope. This drawing describes device requirements for class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices".

1.2 Part or Identifying Number (PIN). The complete PIN shall be as shown in the following example:

1.2.1 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Generic number	Circuit function	Total unadjusted error
01	AD7821	CMOS 8-bit ADC with track/hold	±1.0 LSB

1.2.2 Case outline(s). The case outline(s) shall be as designated in appendix C of MIL-M-38510, and as follows:

Outline letter	Case outline
R	D-8 (20-lead, 1.060" x .310" x .200"), dual-in-line package
2	C-2 (20-lead, .358" x .358" x .100"), square chip carrier package

1.3 Absolute maximum ratings. 1/

Supply voltage to ground (V_{SS})	0 V dc to -7.0 V dc
Supply voltage to ground (V_{DD})	0 V dc to +7.0 V dc
Digital input voltage	-0.3 V dc to V_{DD}
Digital output voltage	-0.3 V dc to V_{DD}
Positive reference voltage (V_{REF+})	V_{SS} - 0.3 V dc, V_{DD} + 0.3 V dc
Negative reference voltage (V_{REF-})	V_{SS} - 0.3 V dc, V_{DD} + 0.3 V dc
Input voltage (V_{IN})	V_{SS} - 0.3 V dc, V_{DD} + 0.3 V dc
Storage temperature range	-65°C to +150°C
Lead temperature (soldering, 10 seconds)	+300°C
Power dissipation (P_D)	450 mW 2/
Thermal resistance, junction-to-case (θ_{JC})	See MIL-M-38510, appendix C
Junction temperature (T_J)	+150°C

1.4 Recommended operating conditions.

Supply voltage to ground (V_{SS})	-4.75 V dc to -5.25 V dc
Supply voltage to ground (V_{DD})	+4.75 V dc to +5.25 V dc
Ambient operating temperature range (T_A)	-55°C to +125°C
Positive reference voltage (V_{REF+})	V_{REF-} to V_{DD}
Negative reference voltage (V_{REF-})	V_{SS} to V_{REF+}

1/ All voltages are with respect to ground.
2/ Derate above T_A = +75°C at 6.0 mW/°C.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standard, and bulletin. Unless otherwise specified, the following specification, standard, and bulletin of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

BULLETIN

MILITARY

MIL-BUL-103 - List of Standardized Military Drawings (SMD's).

(Copies of the specification, standard, and bulletin required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.2 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full ambient operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ 2/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Limits		Unit
				Min	Max	
Resolution	Res	This is the minimum resolution for which no missing codes are guaranteed.	1, 2, 3	8.0		Bits
Total unadjusted error	TUE	3/	1, 2, 3		±1.0	LSB
Analog input leakage current	I_{IN}		1, 2, 3		±3.0	µA
Reference input resistance	R_{IN}		1, 2, 3	1.0	4.0	kΩ
Digital input high current	I_{IH}	$\overline{CS}$ and $\overline{RD}$ inputs, V_{IH} = 5.25 V, V_{IL} = 0 V	1, 2, 3		±1.0	µA
		$\overline{WR}$ input, V_{IH} = 5.25 V, V_{IL} = 0 V			±3.0	
		Mode input, V_{IH} = 5.25 V, V_{IL} = 0 V			±200	
Digital input low current	I_{IL}	$\overline{CS}$, $\overline{WR}$, $\overline{RD}$ and mode inputs	1, 2, 3		-1.0	µA
Digital output high level voltage	V_{OH}	DB_0-DB_7, $\overline{OFL}$, and $\overline{INT}$ outputs, I_{SOURCE} = -360 µA	1, 2, 3	4.0		V
Digital output low level voltage	V_{OL}	DB_0-DB_7, $\overline{OFL}$, and $\overline{INT}$ outputs, I_{SINK} = 1.6 mA	1, 2, 3		0.4	V
Floating state leakage current	I_{OUT}	DB_0-DB_7, V_{OUT} = 5.25 V, then V_{OUT} = 0 V	1, 2, 3		±3.0	µA
Supply current from V_{DD}	I_{DD}	$\overline{CS}$ = $\overline{RD}$ = 0 V	1, 2, 3		20.0	mA
Digital input low level voltage	V_{IL}	$\overline{CS}$, $\overline{WR}$ and $\overline{RD}$ inputs	1, 2, 3		0.8	V
		Mode input			1.5	
Digital input high level voltage	V_{IH}	$\overline{CS}$, $\overline{WR}$ and $\overline{RD}$ inputs	1, 2, 3	2.4		V
		Mode input		3.5		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ 2/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Limits		Unit
				Min	Max	
Power supply sensitivity	PSS	V_{DD} = 5.0 V ±5% V_{REF} = 4.75 V maximum	1, 2, 3		±0.25	LSB
Signal to noise ratio	SNR	4/ 5/	1, 2, 3	45		dB
Total harmonic distortion	THD	4/ 5/	1, 2, 3		-50	dB
Peak harmonic or spurious noise		4/ 5/	1, 2, 3		-50	dB
Intermodulation distortion	IMD	Second order terms 5/ 6/	1, 2, 3		-50	dB
		Third order terms 5/ 6/			-50	
Supply current from V_{SS}	I_{SS}	$\overline{CS}$ = $\overline{RD}$ = 0 V	1, 2, 3		100	µA
Digital input capacitance	C_{ID}	$\overline{CS}$, $\overline{WR}$, $\overline{RD}$ and mode inputs See 4.3.1c, T_A = +25°C	4		8.0	pF
Analog input capacitance	C_{IA}	See 4.3.1c	4		55	pF
Digital output capacitance	C_{OUT}	See 4.3.1c, T_A = +25°C	4		8.0	pF
Slew rate, tracking	SR	4/ 5/	7, 8		1.6	V/µs
$\overline{RD}$ pulse width	t_{READ1}	Determined by t_{ACC1} 7/ 8/	9	160		ns
			10, 11	240		
$\overline{RD}$ pulse width	t_{READ2}	Determined by t_{ACC2} 7/ 8/	9	65		ns
			10, 11	85		
$\overline{CS}$ to $\overline{RD}$/$\overline{WR}$ setup time	t_{CSS}	7/ 8/	9, 10, 11	0		ns
$\overline{CS}$ to $\overline{RD}$/$\overline{WR}$ hold time	t_{CSH}	7/ 8/	9, 10, 11	0		ns
$\overline{CS}$ to RDY delay	t_{RDY}	C_L = 50 pF, pull-up resistor = 4.7 kΩ 8/	9		70	ns
			10, 11		100	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ 2/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Limits		Unit
				Min	Max	
Conversion time ($\overline{RD}$ mode)	t_{CRD}	8/	9		700	ns
			10, 11		975	
Data access time ($\overline{RD}$ mode)	t_{ACCO}	8/ 9/	9		750	ns
			10, 11		1050	
$\overline{RD}$ to $\overline{INT}$ delay ($\overline{RD}$ mode)	t_{INTH}	C_L = 50 pF 8/	9		80	ns
			10, 11		90	
Data hold time	t_{DH}	8/ 10/	9		60	ns
			10, 11		80	
Delay time between conversion	t_P	7/ 8/	9	350		ns
			10, 11	500		
Write pulse width	t_{WR}	7/ 8/	9	0.25	10	µs
			10, 11	0.4	10	
Delay time between $\overline{WR}$ and $\overline{RD}$ pulses	t_{RD}	7/ 8/	9	250		ns
			10, 11	450		
Data access time ($\overline{WR}$/$\overline{RD}$ mode)	t_{ACC1}	8/ 9/	9		185	ns
			10, 11		275	
$\overline{RD}$ to $\overline{INT}$ delay	t_{R1}	8/	9		150	ns
			10, 11		220	
$\overline{WR}$ to $\overline{INT}$ delay	t_{INTL}	C_L = 50 pF, see figure 3 11/	9		500	ns
			10, 11		700	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ 2/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Limits		Unit
				Min	Max	
Data access time ($\overline{WR}/\overline{RD}$ mode)	t_{ACC2}	8/ 9/	9		90	ns
			10, 11		130	
$\overline{WR}$ to $\overline{INT}$ delay (stand alone operation)	t_{IHWR}	C_L = 50 pF 8/	9		80	ns
			10, 11		120	
Data access time after $\overline{INT}$ (stand alone operation)	t_{ID}	8/ 9/	9		45	ns
			10, 11		70	

1/ Unless otherwise specified, V_{DD} = +5.0 V; V_{REF+} = +5.0 V; V_{REF-} = GND = 0 V and V_{SS} = 0 V.

2/ All input control signals are specified with $t_R = t_F$ = 20 ns (10% to 90% of +5.0 V) and timed from a voltage level of 1.6 V.

3/ Includes gain error, offset error and linearity error.

4/ V_{IN} = 99.85 kHz full scale sine wave at 5.0 V peak to peak with f sampling = 500 kHz.

5/ V_{SS} = -5.0 V; V_{DD} = +5.0 V; V_{REF+} = +2.5 V; V_{REF-} = -2.5 V.

6/ fa (84.72 kHz) and fb (94.97 kHz) combine to produce a full scale sine wave at the analog input with f sampling = 500 kHz.

7/ Pass/fail tested only with tested parameter used as a test condition.

8/ Refer to timing diagram of figure 3. These parameters are tested to subgroup 9 under group A test requirements.

9/ Measured with load circuits of figure 2 and defined as the time required for an output to cross 0.8 V to 2.4 V.

10/ Defined as the time required for the data lines to change 0.5 V when loaded with the circuits of figure 2 and is measured only for initial test and after process or design changes which may affect t_{DH}.

11/ If not tested, shall be guaranteed to the limits specified in table I herein.

Device type	01
Case outlines	R and 2
Terminal number	Terminal symbol
1	V_{IN}
2	DB_0(LSB)
3	DB_1
4	DB_2
5	DB_3
6	$\overline{WR}$/RDY
7	Mode
8	$\overline{RD}$
9	$\overline{INT}$
10	GND
11	V_{REF-}
12	V_{REF+}
13	$\overline{CS}$
14	DB_4
15	DB_5
16	DB_6
17	DB_7(MSB)
18	$\overline{OFL}$
19	V_{SS}
20	V_{DD}

FIGURE 1. Terminal connections.

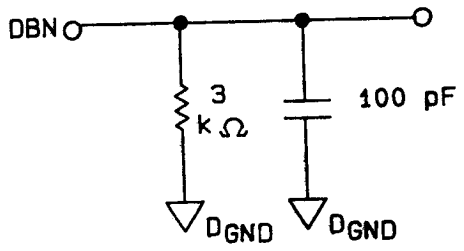
Pin function description

Pin	Symbol	Description
1	V_{IN}	Analog input: Range $V_{REF}(-) \leq V_{IN} \leq V_{REF}(+)$
2	DB_0	Three-State Data Output (LSB)
3-5	DB_1-DB_3	Three-State Data Outputs.
6	$\overline{WR}$/RDY	WRITE control input/READY status output.
7	MODE	Mode Selection Input. It determines whether the device operates in the WR-RD or RD mode. This input is internally pulled low through a 50 μA current source.
8	$\overline{RD}$	READ input. $\overline{RD}$ must be low to access data from the part.
9	$\overline{INT}$	INTERRUPT Output. $\overline{INT}$ going low indicates that the conversion is complete. $\overline{INT}$ returns high on the rising edge of $\overline{CS}$ or $\overline{RD}$.
10	GND	Ground.
11	$V_{REF}(-)$	Lower limit of reference span. Range: $V_{SS} \leq V_{REF}(-) < V_{REF}(+)$
12	$V_{REF}(+)$	Upper limit of reference span. Range: $V_{REF}(-) < V_{REF}(+) \leq V_{DD}$.
13	$\overline{CS}$	Chip Select Input. The device is selected when this input is low.
14-16	DB_4-DB_6	Three-State Data Outputs.
17	DB_7	Three-State Data Output (MSB).
18	$\overline{OFL}$	Overflow Output. If the analog input is higher than ($V_{REF}(+)$ - 1/2 LSB, $\overline{OFL}$ will be low at the end of conversion. It is a non-three-state output which can be used to cascade 2 or more device to increase resolution.
19	V_{SS}	Negative supply voltage. V_{SS} = 0 V; Unipolar Operation. V_{SS} = -5 V; Bipolar Operation.
20	V_{DD}	Positive supply voltage, +5 V.

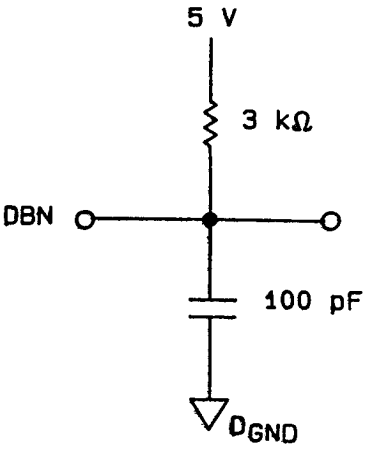
FIGURE 1. Terminal connections - Continued.

Load circuits for data access time

High-Z to V_{OH}

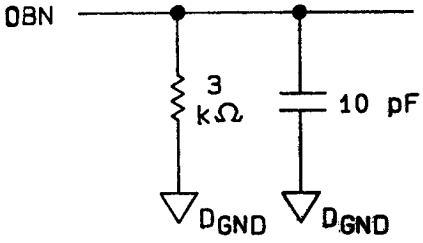


High-Z to V_{OL}



Load circuits for data hold time

V_{OH} to High-Z



V_{OL} to High-Z

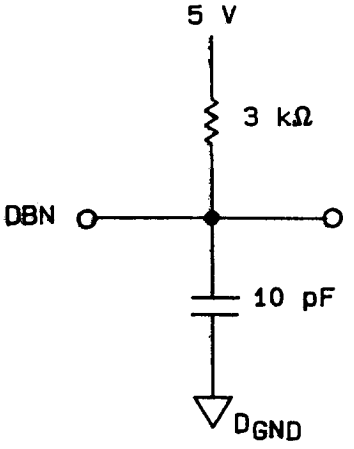
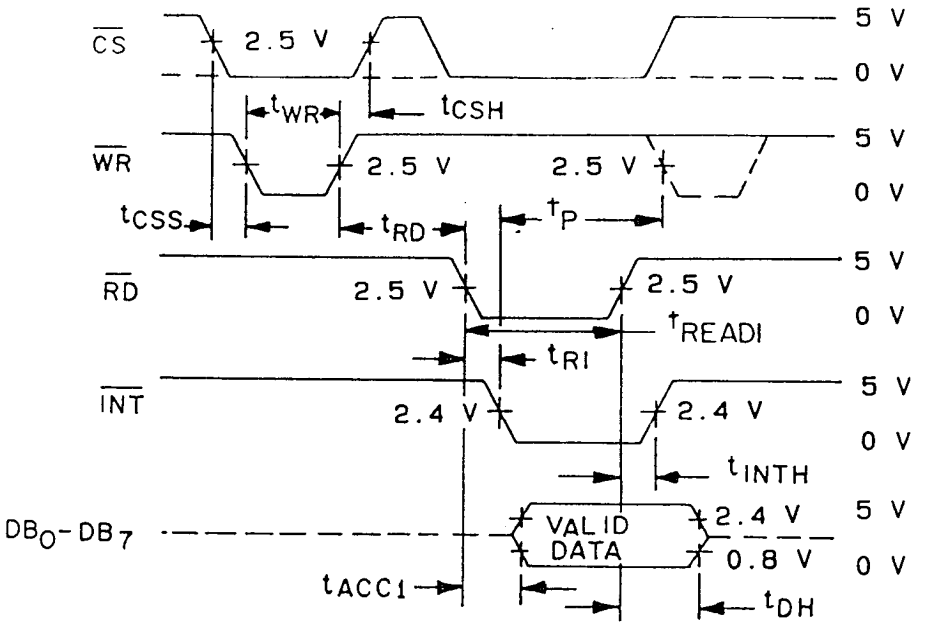


FIGURE 2. Output load circuits.

WR-RD mode ($t_{RD} < t_{INTL}$)



WR-RD mode ($t_{RD} > t_{INTL}$)

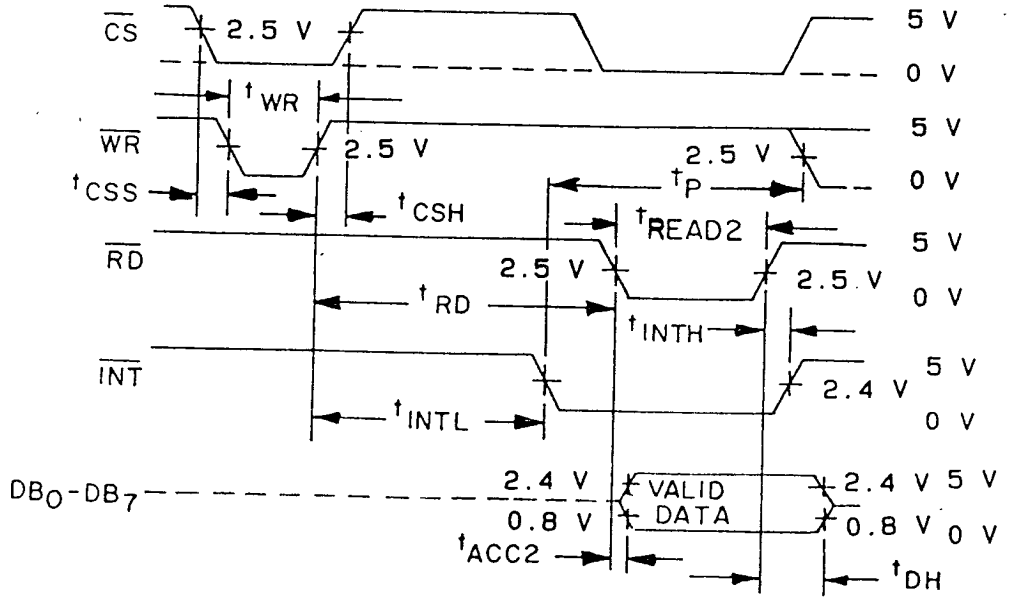


FIGURE 3. Mode timing waveforms.

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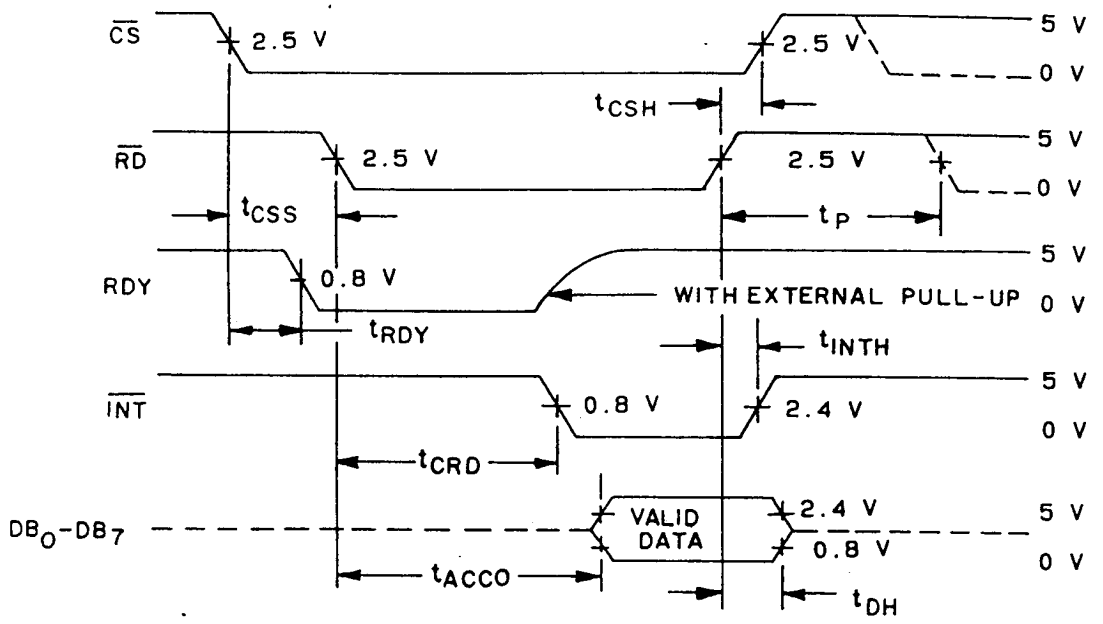
RD mode



WR-RD mode stand-alone operation, $\overline{CS} = \overline{RD} = 0$

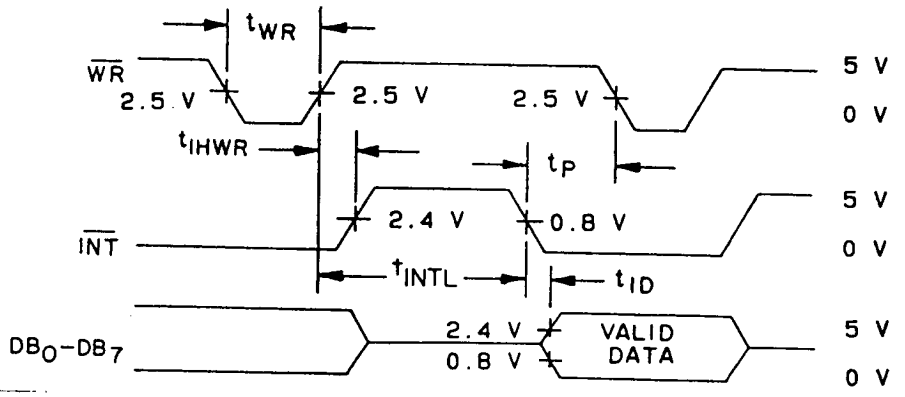


FIGURE 3. Mode timing waveforms - Continued.

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3.5 Marking. Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-BUL-103 (see 6.6 herein).

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-BUL-103 (see 6.6 herein). The certificate of compliance submitted to DESC-ECS prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-STD-883 (see 3.1 herein) and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DESC-ECS shall be required in accordance with MIL-STD-883 (see 3.1 herein).

3.9 Verification and review. DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein).

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D using the circuit submitted with the certificate of compliance (see 3.6 herein).

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_{IA}, C_{ID}, and C_{OUT} measurements) shall be measured only for the initial test and after process or design changes which may affect capacitance. For C_{IA} and C_{ID}, each input is checked separately. For C_{OUT}, each output is checked separately.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (per method 5005, table I)
Interim electrical parameters (method 5004)	1
Final electrical test parameters (method 5004)	1*,2,3,7,8
Group A test requirements (method 5005)	1,2,3,4,7,8, 9, 10**,11**
Groups C and D end-point electrical parameters (method 5005)	1

* PDA applies to subgroup 1.
** Subgroups 10 and 11, if not tested, shall be guaranteed to the specified limits in table I.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition A, B, C, or D using the circuit submitted with the certificate of compliance (see 3.6 herein).

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use when military specifications do not exist and qualified military devices that will perform the required function are not available for OEM application. When a military specification exists and the product covered by this drawing has been qualified for listing on QPL-38510, the device specified herein will be inactivated and will not be used for new design. The QPL-38510 product shall be the preferred item for all applications.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-481 using DD Form 1693, Engineering Change Proposal (Short Form).

6.4 Record of users. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and the applicable SMD. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DESC-ECS, telephone (513) 296-6022.

6.5 Comments. Comments on this drawing should be directed to DESC-ECS, Dayton, Ohio 45444, or telephone (513) 296-5375.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-BUL-103. The vendors listed in MIL-BUL-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-ECS.