



Quad 2-Input Multiplexer (Non-Inverting)

**ELECTRICALLY TESTED PER:
5962-8756601**

The 10H558 is a quad two channel multiplexer with common input select. A "high" level select enables input D00, D10, D20 and D30 and a "low" level select enables input D01, D11, D21 and D31.

This MECL 10H part is a functional/pinout duplication of the standard MECL 10K family part, with 100% improvement in propagation delay and no increase in power-supply current.

- Propagation Delay, 1.5 ns Typical
- 290 mW Max/Pkg (No Load)
- Improved Noise Margin 150 mV (Over Operating Voltage and Temperature Range)
- Voltage Compensated
- MECL 10K-Compatible

PIN ASSIGNMENTS

FUNCTION	DIL	FLATS	LCC	BURN-IN (CONDITION C)
Q0	1	5	2	51 Ω to V _{TT}
Q1	2	6	3	51 Ω to V _{TT}
D11	3	7	4	51 Ω to V _{TT}
D10	4	8	5	OPEN
D01	5	9	7	GND
D00	6	10	8	OPEN
NC	7	11	9	OPEN
VEE	8	12	10	VEE
Select	9	13	12	OPEN
D31	10	14	13	GND
D30	11	15	14	OPEN
D21	12	16	15	GND
D20	13	1	17	OPEN
Q3	14	2	18	51 Ω to V _{TT}
Q2	15	3	19	51 Ω to V _{TT}
VCC	16	4	20	GND

BURN - IN CONDITIONS:

V_{TT} = - 2.0 V MAX/ - 2.2 V MIN

VEE = - 5.7 V MAX/ - 5.2 V MIN

Select	D0	D1	Q
L	∅	L	L
L	∅	H	H
H	L	∅	L
H	H	∅	H

∅ = Don't Care

Military 10H558

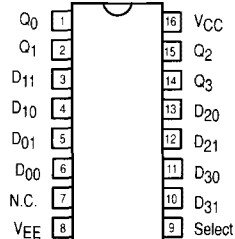


AVAILABLE AS

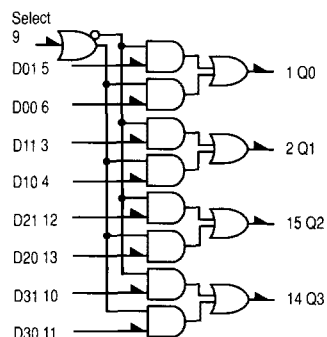
- 1) JAN: N/A
 - 2) SMD: 5962-8756601
 - 3) 883: 10H558/BXAJC
- X = CASE OUTLINE AS FOLLOWS:

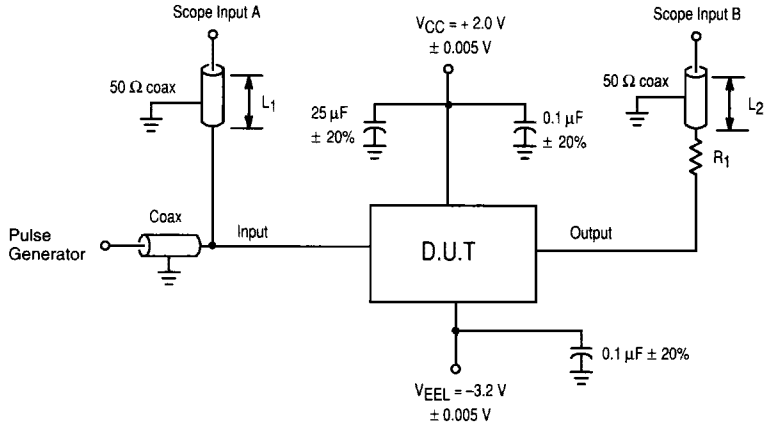
PACKAGE: CERDIP: E
CERFLAT: F
LCC: 2

The letter "M" appears before the slash on LCC.



POSITIVE LOGIC DIAGRAM





NOTES

1. Pulse generator must be capable of rise and fall times of $2.0 \text{ ns} \pm 0.2 \text{ ns}$.
2. Unused outputs connected to $100 \text{ } \Omega$ resistor to ground.
3. 2:1 divider may be used.
4. $L1 = L2$: Matched for equal time delay.
5. $R1 = 50 \text{ } \Omega$ resistor in series with $50 \text{ } \Omega$ coax constituting the $100 \text{ } \Omega$ load.
6. $t_r = t_f = 1.0 \text{ ns} \pm 0.1 \text{ ns}$ (20% - 80%).
7. $P_W \geq 20 \text{ ns}$.
7. $P_{RF} = 1.0 \text{ MHz}$.

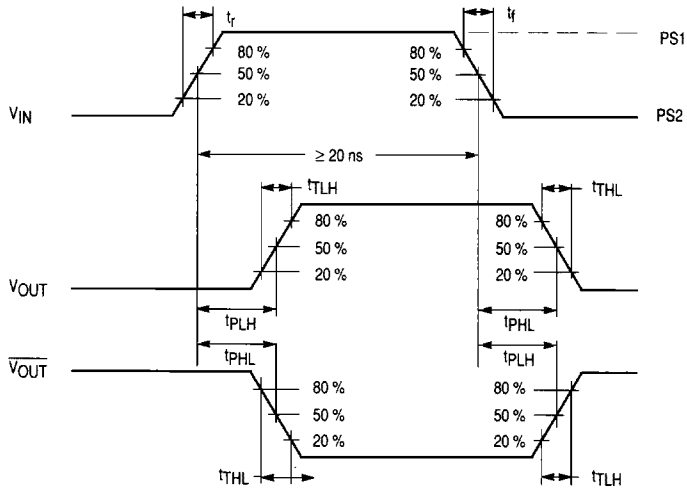


Figure 1. Switching Test Circuit and Waveforms

10H558 QUIESCENT LIMIT TABLE *

* ELECTRICAL CHARACTERISTICS

Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to - 2.0 volts.

Test Temperature	Test Voltage Values (Volts)									
	V _{IH}	V _{IL}	V _{IH1}	V _{IL1}	PS1	PS2	VEE1	VEE2	VEEL	VEEL
T _A = 25 °C	-0.78	-1.95	-1.10	-1.480	+1.11	+0.31	-5.46	-4.94	-2.94	-2.94
T _A = 125 °C	-0.65	-1.95	-0.96	-1.465	+1.24	+0.36	-5.46	-4.94	-2.94	-2.94
T _A = -55 °C	-0.84	-1.95	-1.16	-1.510	+1.01	+0.28	-5.46	-4.94	-2.94	-2.94

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW									
		+ 25° C		+ 125° C		- 55° C			Pinouts referenced are for DIL package, check Pin Assignments VCC = 0 V, Output Load = 100 Ω to GND									
		Subgroup 1 Min	Subgroup 1 Max	Subgroup 2 Min	Subgroup 2 Max	Subgroup 3 Min	Subgroup 3 Max		V _{IH1}	V _{IL1}	V _{IH2}	V _{IL2}	VEE1	VEE2	V _{CC}	P.U.T.		
V _{OH}	High Output Voltage	-1.01	-0.78	-0.86	-0.65	-1.06	-0.84	V	3-5, 10, 12				8		16	1, 2, 14, 15		
V _{OL}	Low Output Voltage	-1.95	-1.58	-1.95	-1.565	-1.95	-1.61	V					8		16	1, 2, 14, 15		
V _{OH1}	High Output Voltage	-1.01	-1.78	-0.86	-0.65	-1.06	-0.84	V	3-6, 9-13				8	8	16	1, 2, 13, 15		
V _{OL1}	Low Output Voltage	-1.95	-0.58	-1.95	-1.565	-1.95	-1.61	V	3-6, 9-13		3-6, 9-13		8	8	16	1, 2, 14, 15		
IEE	Power Supply Current	-48		-53		-53		mA			9		8		16	8		
I _{IH1}	Input Current High		295		475		475	μ A	9				8		16	9		
I _{IH2}	Input Current High		320		515		515	μ A	3-6, 9-13				8		16	3-6, 9-13		
I _{IL}	Input Current	0.5		0.3		0.5		μ A		3-6 9-13			8		16	3-6, 9-13		

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Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW									
		+ 25 °C		+ 125 °C		- 55 °C			Pinouts referenced are for DIL package, check Pin Assignments V _{CC} = 2.0 V, Output Load = 100 Ω to GND									
		Subgroup 9	Subgroup 10	Subgroup 11	Subgroup 10	Subgroup 11	Subgroup 11											
t _{TLH}	Rise Time	0.7	2.0	0.7	2.2	0.7	2.2	ns	V _{IN}	V _{OUT}	V _{CC}	VEEL	P.U.T.	1, 2	8	16	8	1, 2, 14, 15
t _{THL}	Fall Time	0.7	2.0	0.7	2.2	0.7	2.2	ns	V _{IN}	V _{OUT}	V _{CC}	VEEL	P.U.T.	1, 2	8	16	8	1, 2, 14, 15
t _{pLH}	Propagation Delay Data to Output	0.5	1.8	0.5	2.2	0.5	1.9	ns	V _{IN}	V _{OUT}	V _{CC}	VEEL	P.U.T.	3 - 6	1, 2, 10 - 13	16	8	1, 2, 14, 15
t _{pLH}	Propagation Delay Data to Output	0.5	1.8	0.5	2.2	0.5	1.9	ns	V _{IN}	V _{OUT}	V _{CC}	VEEL	P.U.T.	3 - 6	1, 2, 10 - 13	16	8	1, 2, 14, 15
t _{pHL}	Propagation Delay Select to Output	1.0	2.7	1.0	3.0	1.0	2.7	ns	V _{IN}	V _{OUT}	V _{CC}	VEEL	P.U.T.	3 - 6, 10 - 13	1, 2	16	8	1, 2, 14, 15
t _{pLH}	Propagation Delay Select to Output	1.0	2.7	1.0	3.0	1.0	2.7	ns	V _{IN}	V _{OUT}	V _{CC}	VEEL	P.U.T.	3 - 6, 10 - 13	1, 2	16	8	1, 2, 14, 15