



STD60NF55L

N-CHANNEL 55V - 0.012Ω - 60A DPAK
STripFET™ II POWER MOSFET

TYPE	V _{DSS}	R _{D(on)}	I _D
STD60NF55L	55V	< 0.015Ω	60A

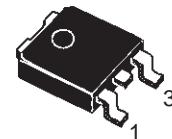
- TYPICAL R_{D(on)} = 0.012Ω
- LOW THRESHOLD DRIVE
- ADD SUFFIX "T4" FOR ORDERING IN TAPE & REEL

DESCRIPTION

This Power Mosfet is the latest development of STMicroelectronics unique "Single Feature Size™" strip-based process. The resulting transistor shows extremely high packing density for low on-resistance, rugged avalanche characteristics and less critical alignment steps therefore a remarkable manufacturing reproducibility..

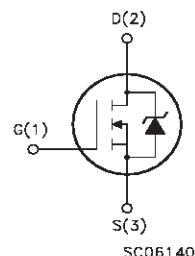
APPLICATIONS

- AUTOMOTIVE
- MOTOR CONTROL



DPAK
TO-252

INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V _{DS}	Drain-source Voltage (V _{GS} = 0)	55	V
V _{DGR}	Drain-gate Voltage (R _{GS} = 20 kΩ)	55	V
V _{GS}	Gate- source Voltage	± 15	V
I _D	Drain Current (continuous) at T _C = 25°C	60	A
I _D	Drain Current (continuous) at T _C = 100°C	42	A
I _{DM} (I ₎	Drain Current (pulsed)	240	A
P _{TOT}	Total Dissipation at T _C = 25°C	110	W
	Derating Factor	0.73	W/°C
dv/dt (1)	Peak Diode Recovery voltage slope	16	V/ns
E _{AS} (2)	Single Pulse Avalanche Energy	400	mJ
T _{stg}	Storage Temperature	– 55 to 175	°C
T _j	Operating Junction Temperature		

(●) Pulse width limited by safe operating area

(1) I_{SD} ≤ 40A, di/dt ≤ 350A/μs, V_{DD} ≤ V_{(BR)DSS}, T_j ≤ T_{JMAX}.

(2) Starting T_j = 25°C, I_D = 30A, V_{DD} = 20V

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THERMAL DATA

Rthj-case	Thermal Resistance Junction-case Max	1.36	°C/W
Rthj-amb	Thermal Resistance Junction-ambient Max	62.5	°C/W
T _L	Maximum Lead Temperature For Soldering Purpose	275	°C

ELECTRICAL CHARACTERISTICS (TCASE = 25 °C UNLESS OTHERWISE SPECIFIED)

OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V(BR)DSS	Drain-source Breakdown Voltage	I _D = 250 μA, V _{GS} = 0	55			V
I _{DSS}	Zero Gate Voltage Drain Current (V _{GS} = 0)	V _{DS} = Max Rating V _{DS} = Max Rating, T _C = 125 °C			1 10	μA μA
I _{GSS}	Gate-body Leakage Current (V _{DS} = 0)	V _{GS} = ± 15 V			±100	nA

ON (1)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V _{GS(th)}	Gate Threshold Voltage	V _{DS} = V _{GS} , I _D = 250 μA	1		2	V
R _{D(on)}	Static Drain-source On Resistance	V _{GS} = 10 V, I _D = 30 A V _{GS} = 5 V, I _D = 30 A		0.012 0.014	0.015 0.017	Ω Ω

DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g _{fs} (1)	Forward Transconductance	V _{DS} = 10 V, I _D = 30 A		35		S
C _{iss}	Input Capacitance	V _{DS} = 25 V, f = 1 MHz, V _{GS} = 0		1950		pF
C _{oss}	Output Capacitance			390		pF
C _{rss}	Reverse Transfer Capacitance			130		pF

ELECTRICAL CHARACTERISTICS (CONTINUED)

SWITCHING ON

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on Delay Time	$V_{DD} = 25 \text{ V}$, $I_D = 30 \text{ A}$		30		ns
t_r	Rise Time	$R_G = 4.7\Omega$, $V_{GS} = 4.5\text{V}$ (see test circuit, Figure 3)		180		ns
Q_g Q_{gs} Q_{gd}	Total Gate Charge Gate-Source Charge Gate-Drain Charge	$V_{DD} = 40 \text{ V}$, $I_D = 60 \text{ A}$, $V_{GS} = 5 \text{ V}$		40 10 20		nC nC nC

SWITCHING OFF

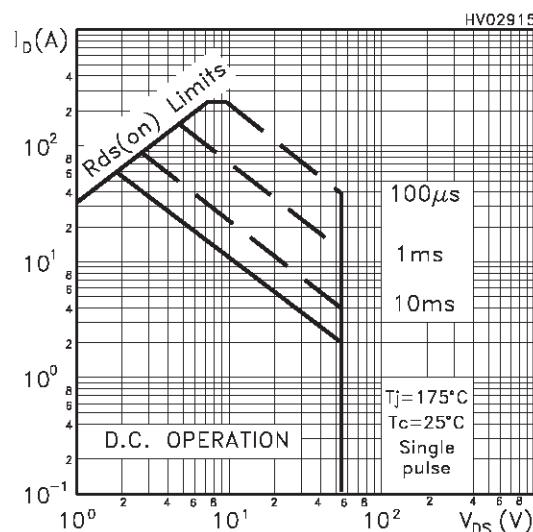
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(off)}$ t_f	Turn-off-Delay Time Fall Time	$V_{DD} = 25 \text{ V}$, $I_D = 30 \text{ A}$, $R_G = 4.7\Omega$, $V_{GS} = 4.5\text{V}$ (see test circuit, Figure 3)		80 35		ns ns

SOURCE DRAIN DIODE

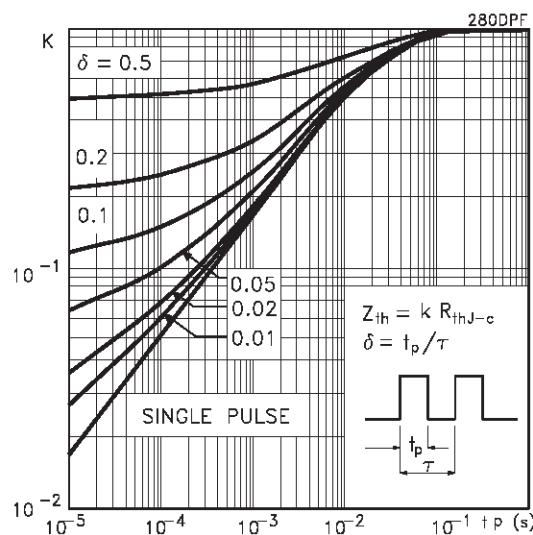
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain Current				60	A
$I_{SDM(2)}$	Source-drain Current (pulsed)				240	A
$V_{SD}(1)$	Forward On Voltage	$I_{SD} = 60 \text{ A}$, $V_{GS} = 0$			1.3	V
t_{rr} Q_{rr} I_{RRM}	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	$I_{SD} = 40 \text{ A}$, $dI/dt = 100 \text{ A}/\mu\text{s}$, $V_{DD} = 25 \text{ V}$, $T_j = 150^\circ\text{C}$ (see test circuit, Figure 5)		65 130 4		ns nC A

Note: 1. Pulsed: Pulse duration = 300 μs , duty cycle 1.5 %.
2. Pulse width limited by safe operating area.

Safe Operating Area

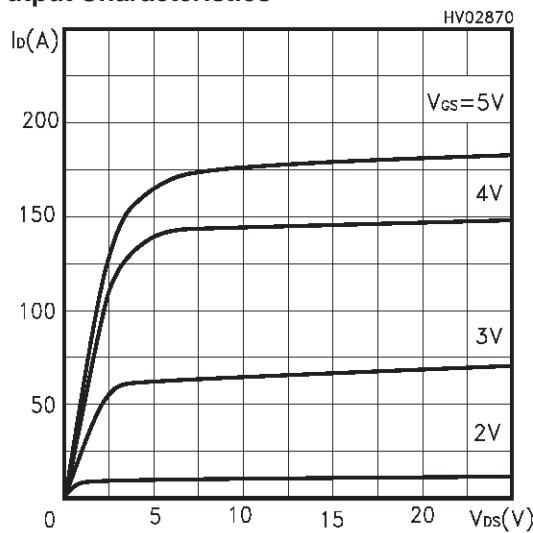


Thermal Impedance

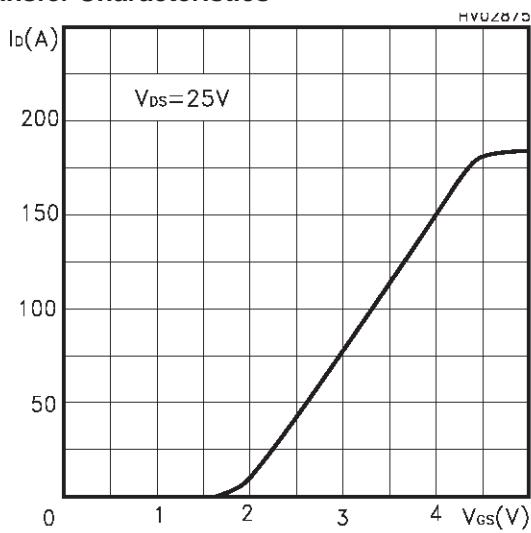


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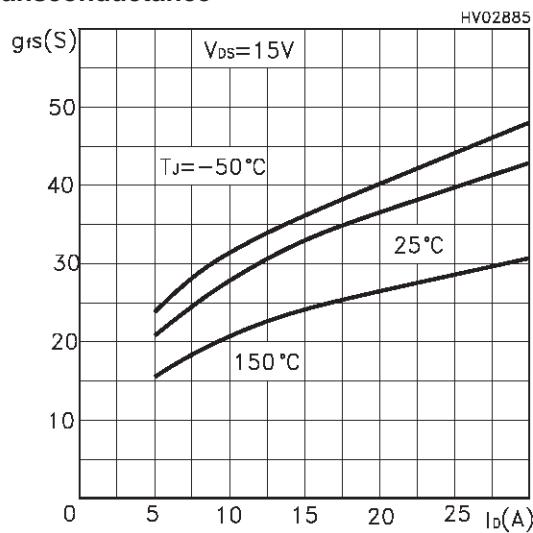
Output Characteristics



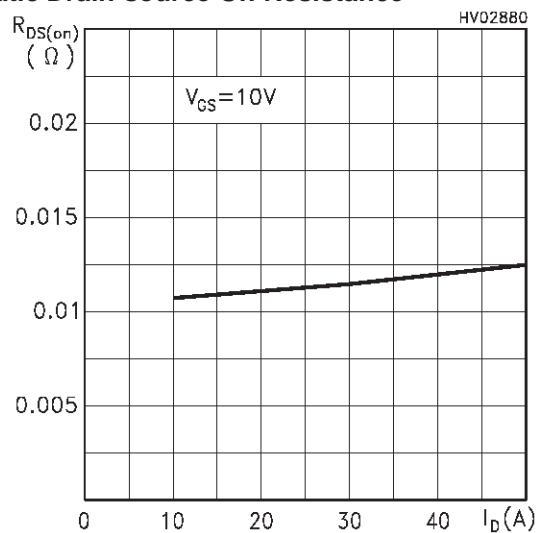
Transfer Characteristics



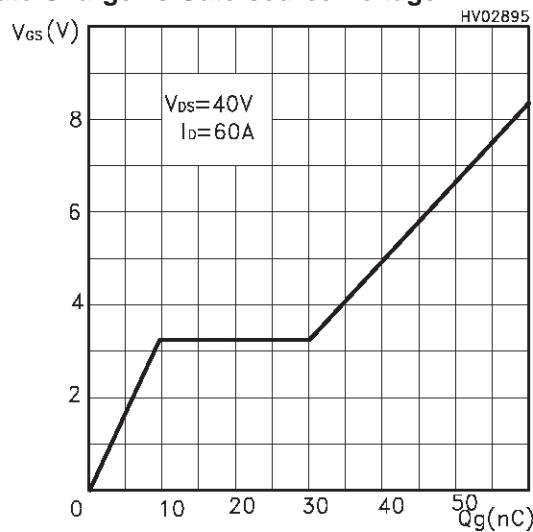
Transconductance



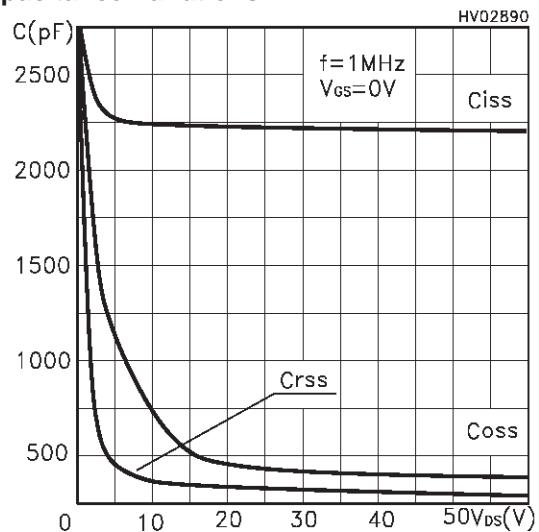
Static Drain-source On Resistance

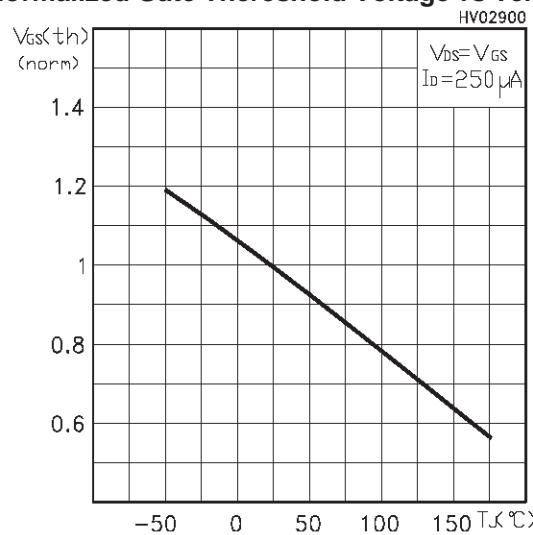
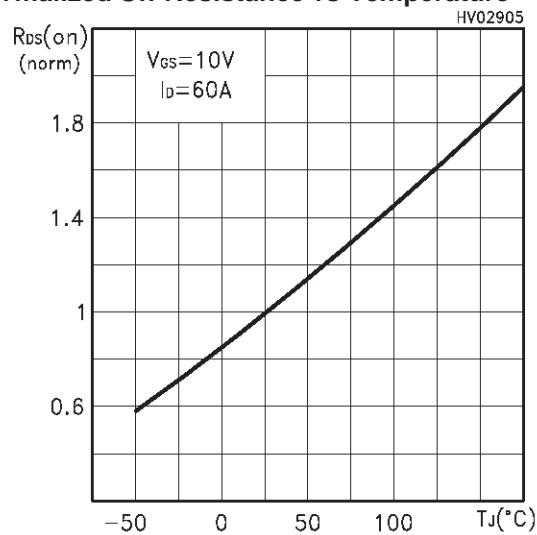
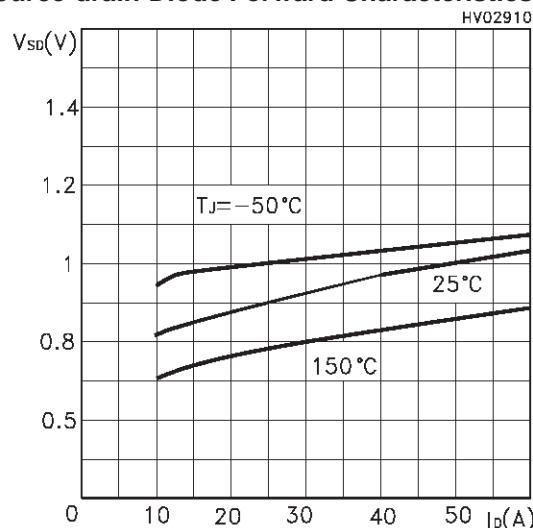


Gate Charge vs Gate-source Voltage



Capacitance Variations



Normalized Gate Threshold Voltage vs Temp.**Normalized On Resistance vs Temperature****Source-drain Diode Forward Characteristics**

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Fig. 1: Unclamped Inductive Load Test Circuit

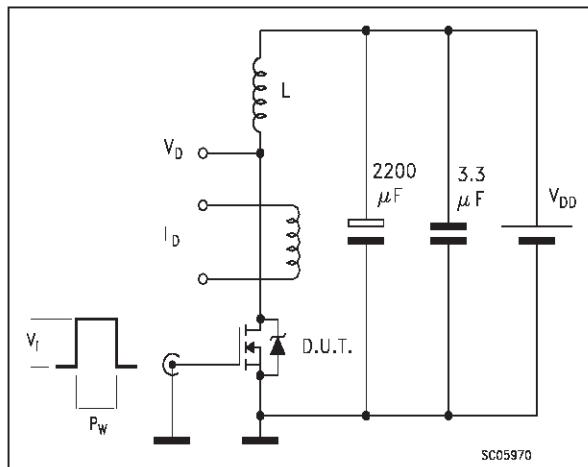


Fig. 2: Unclamped Inductive Waveform

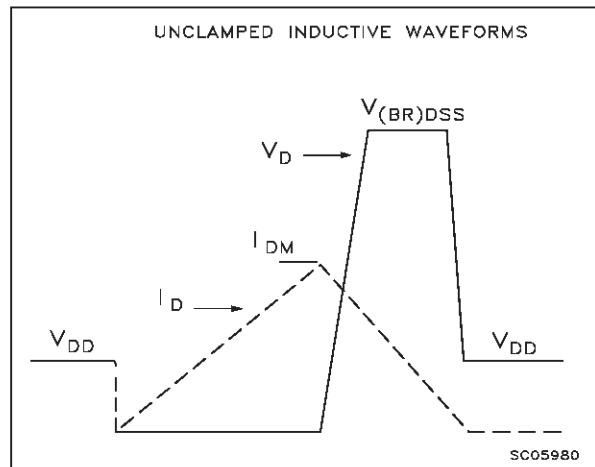


Fig. 3: Switching Times Test Circuit For Resistive Load

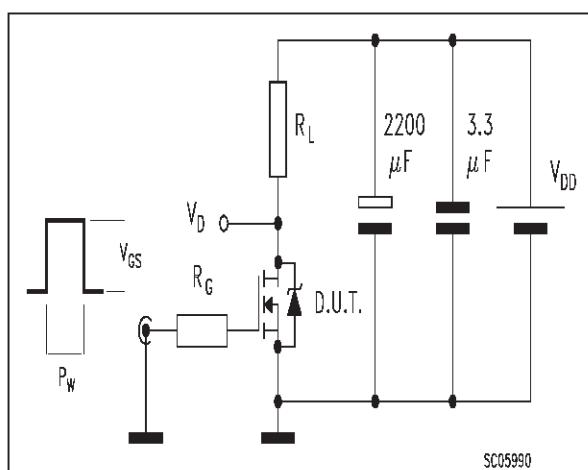


Fig. 4: Gate Charge test Circuit

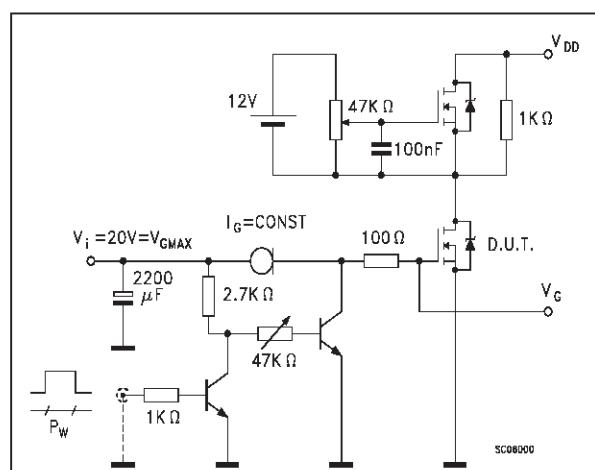
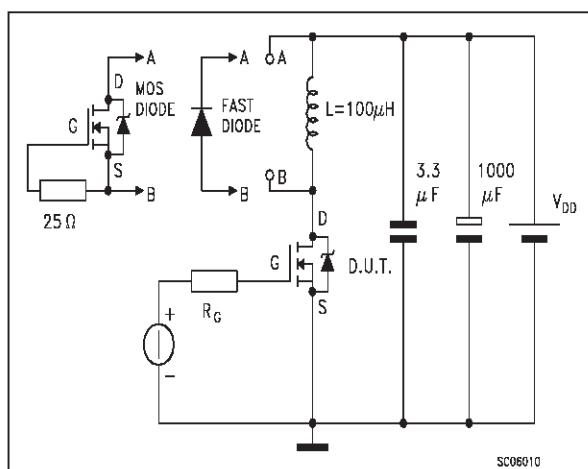
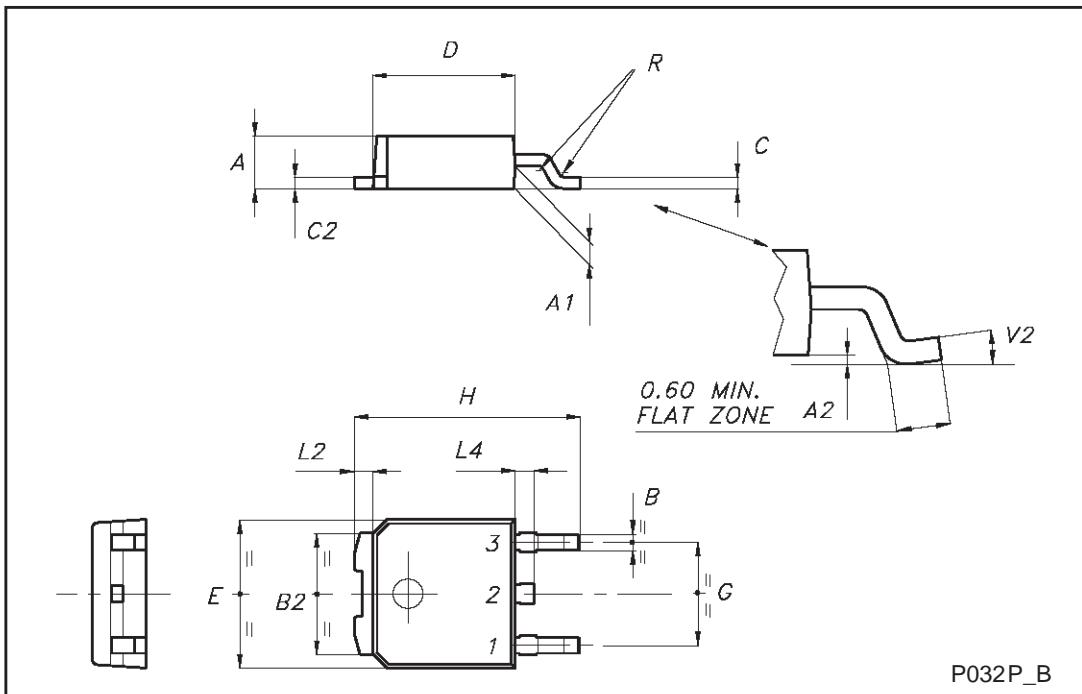


Fig. 5: Test Circuit For Inductive Load Switching And Diode Recovery Times

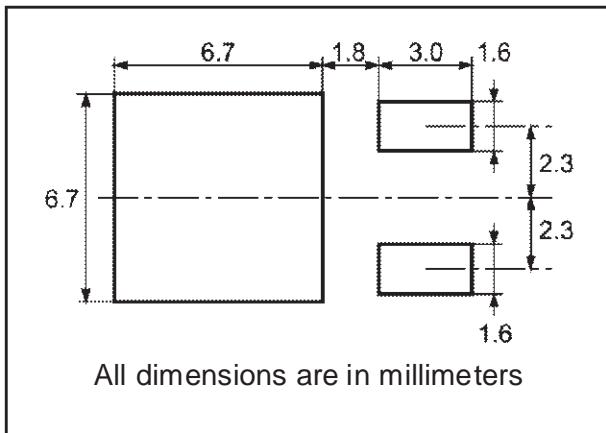
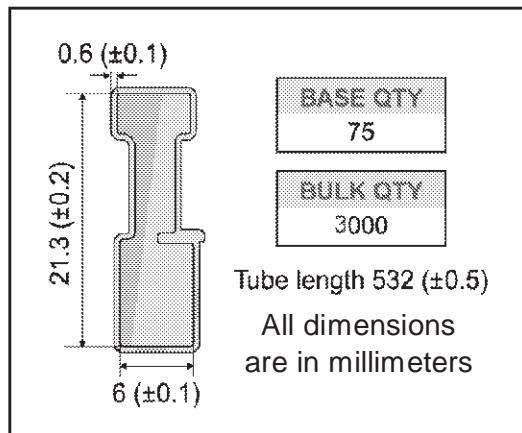
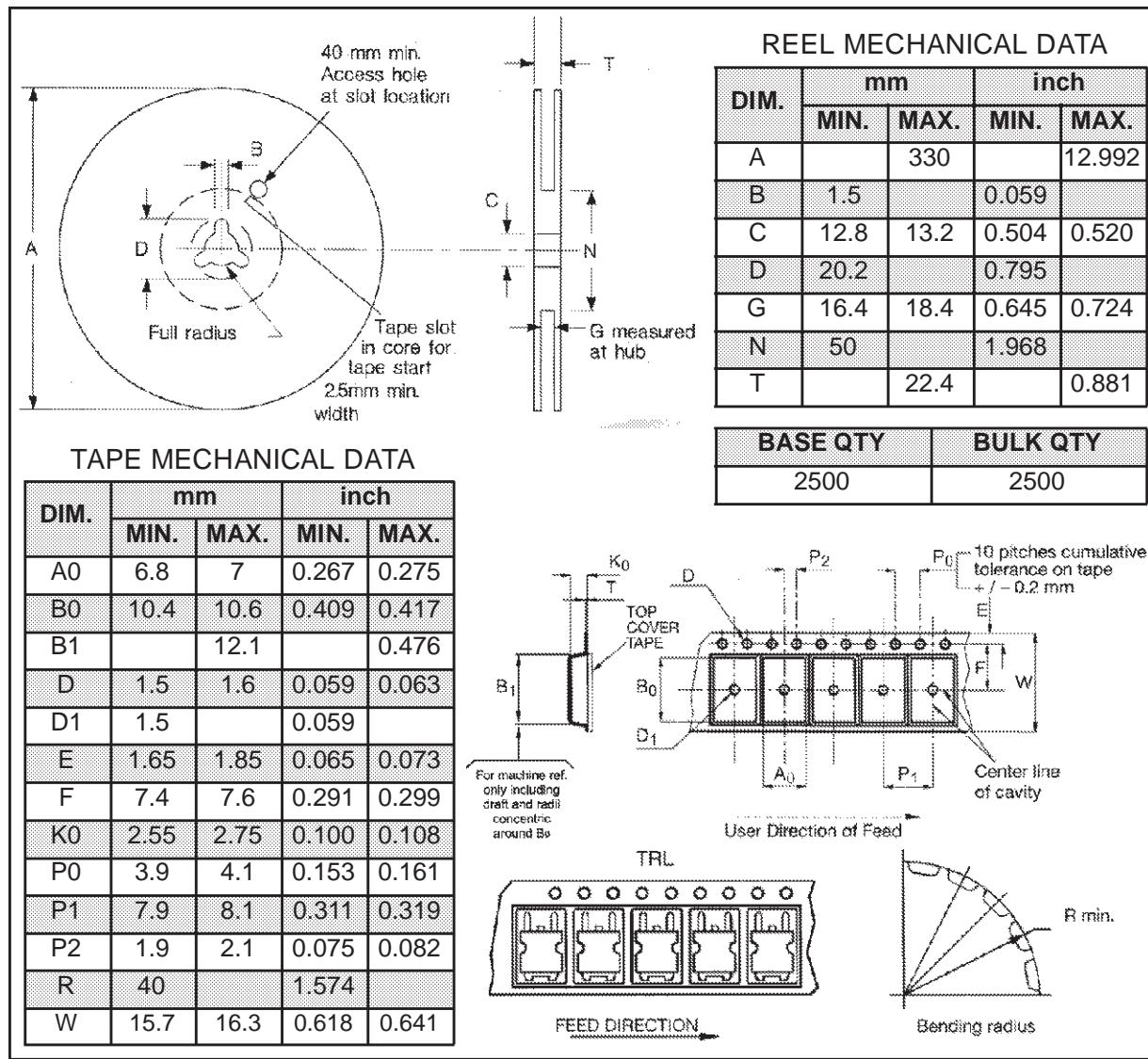


TO-252 (DPAK) MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	2.20		2.40	0.087		0.094
A1	0.90		1.10	0.035		0.043
A2	0.03		0.23	0.001		0.009
B	0.64		0.90	0.025		0.035
B2	5.20		5.40	0.204		0.213
C	0.45		0.60	0.018		0.024
C2	0.48		0.60	0.019		0.024
D	6.00		6.20	0.236		0.244
E	6.40		6.60	0.252		0.260
G	4.40		4.60	0.173		0.181
H	9.35		10.10	0.368		0.398
L2		0.8			0.031	
L4	0.60		1.00	0.024		0.039
V2	0°		8°	0°		0°



P032P_B

DPAK FOOTPRINT**TUBE SHIPMENT (no suffix)*****TAPE AND REEL SHIPMENT (suffix "T4")***

*On sales type

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