



Dual P-Channel 20-V (D-S) MOSFET

PRODUCT SUMMARY		
V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (mA)
-20	1.2 @ $V_{GS} = -4.5$ V	-350
	1.6 @ $V_{GS} = -2.5$ V	-300
	2.7 @ $V_{GS} = -1.8$ V	-150

TrenchFET[®]
MOSFETs
1.8-V Rated



ESD Protected
2000 V

FEATURES

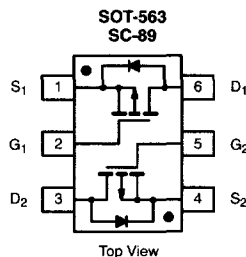
- Very Small Footprint
- High-Side Switching
- Low On-Resistance: 1.2 Ω
- Low Threshold: 0.8 V (typ)
- Fast Switching Speed: 14 ns
- 1.8-V Operation
- Gate-Source ESD Protection

BENEFITS

- Ease in Driving Switches
- Low Offset (Error) Voltage
- Low-Voltage Operation
- High-Speed Circuits
- Low Battery Voltage Operation

APPLICATIONS

- Drivers: Relays, Solenoids, Lamps, Hammers, Displays, Memories
- Battery Operated Systems
- Power Supply Converter Circuits
- Load/Power Switching Cell Phones, Pagers



Marking Code: B

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)					
Parameter		Symbol	5 secs	Steady State	Unit
Drain-Source Voltage		V_{DS}	-20		V
Gate-Source Voltage		V_{GS}	± 6		
Continuous Drain Current ($T_J = 150^\circ\text{C}$) ^a	$T_A = 25^\circ\text{C}$	I_D	-390	-370	mA
	$T_A = 85^\circ\text{C}$		-280	-265	
Pulsed Drain Current ^b		I_{DM}	-650		
Continuous Source Current (diode conduction) ^a		I_S	-450	-380	
Maximum Power Dissipation ^a	$T_A = 25^\circ\text{C}$	P_D	280	250	mW
	$T_A = 85^\circ\text{C}$		145	130	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	-55 to 150		$^\circ\text{C}$
Gate-Source ESD Rating (HBM, Method 3015)		ESD	2000		V

Notes

- Surface Mounted on FR4 Board.
- Pulse width limited by maximum junction temperature.



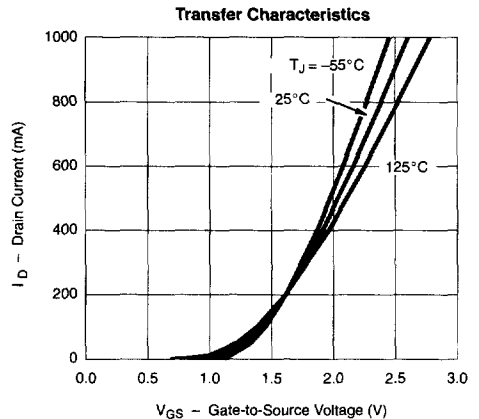
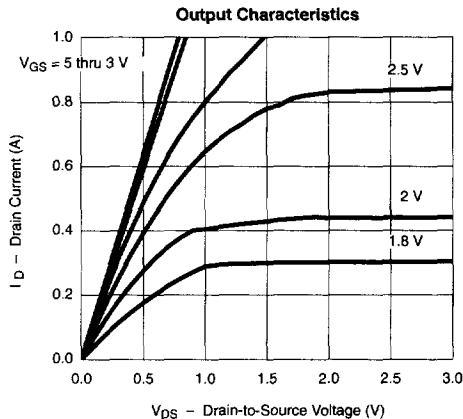
SPECIFICATIONS ($T_J = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)						
Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = -250 \mu\text{A}$	-0.45			V
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 4.5 \text{ V}$		± 1	± 2	μA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -16 \text{ V}, V_{GS} = 0 \text{ V}$		-0.3	-100	nA
		$V_{DS} = -16 \text{ V}, V_{GS} = 0 \text{ V}, T_J = 85^\circ\text{C}$			-5	μA
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} = -5 \text{ V}, V_{GS} = -4.5 \text{ V}$	-700			mA
Drain-Source On-State Resistance ^a	$r_{DS(on)}$	$V_{GS} = -4.5 \text{ V}, I_D = -350 \text{ mA}$		0.8	1.2	Ω
		$V_{GS} = -2.5 \text{ V}, I_D = -300 \text{ mA}$		1.2	1.6	
		$V_{GS} = -1.8 \text{ V}, I_D = -150 \text{ mA}$		1.8	2.7	
Forward Transconductance ^a	g_{fs}	$V_{DS} = -10 \text{ V}, I_D = -250 \text{ mA}$		0.4		S
Diode Forward Voltage ^a	V_{SD}	$I_S = -150 \text{ mA}, V_{GS} = 0 \text{ V}$		-0.8	-1.2	V
Dynamic^b						
Total Gate Charge	Q_g	$V_{DS} = -10 \text{ V}, V_{GS} = -4.5 \text{ V}, I_D = -250 \text{ mA}$		1500		μC
Gate-Source Charge	Q_{gs}			150		
Gate-Drain Charge	Q_{gd}			450		
Turn-On Time	t_{ON}	$V_{DD} = -10 \text{ V}, R_L = 47 \Omega$ $I_D \approx -200 \text{ mA}, V_{GEN} = -4.5 \text{ V}, R_G = 10 \Omega$		14		ns
Turn-Off Time	t_{OFF}			46		

Notes

- a. Pulse test; pulse width $\leq 300 \mu\text{s}$, duty cycle $\leq 2\%$.
- b. Guaranteed by design, not subject to production testing.

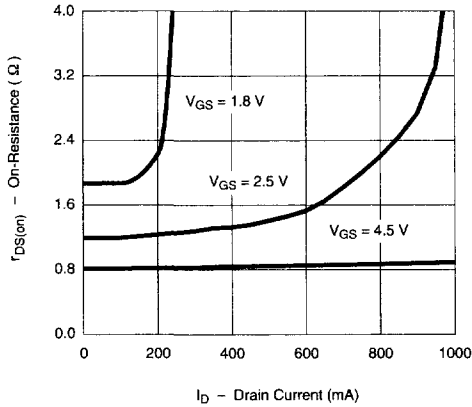
TYPICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ UNLESS NOTED)

For the following graphs, p-channel negative polarities for all voltage and current values are represented as positive values.

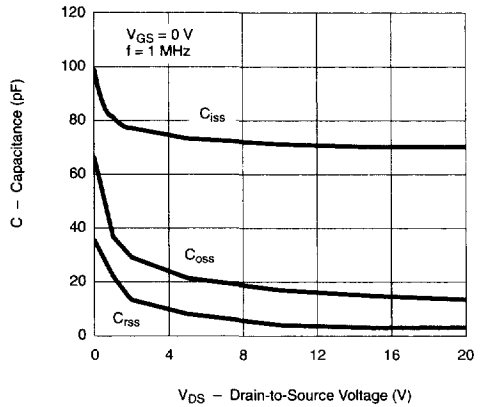


TYPICAL CHARACTERISTICS (T_A = 25°C UNLESS NOTED)

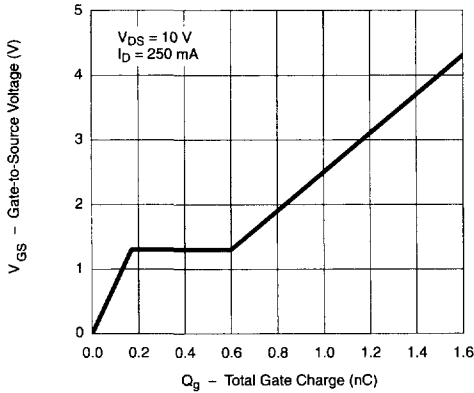
On-Resistance vs. Drain Current



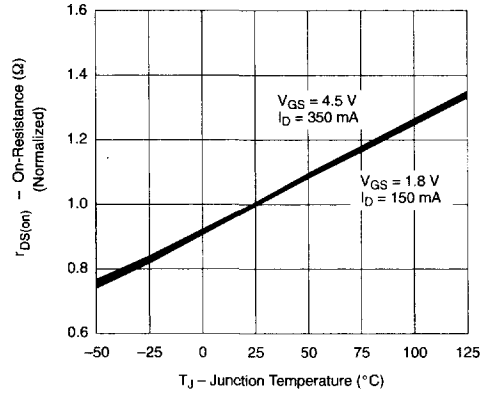
Capacitance



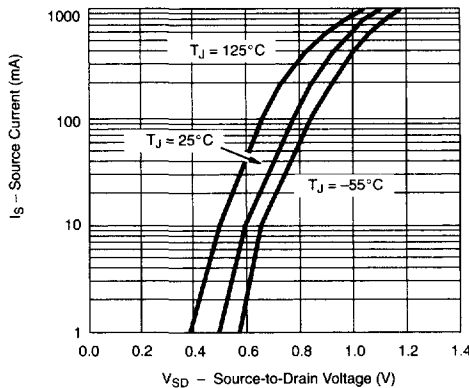
Gate Charge



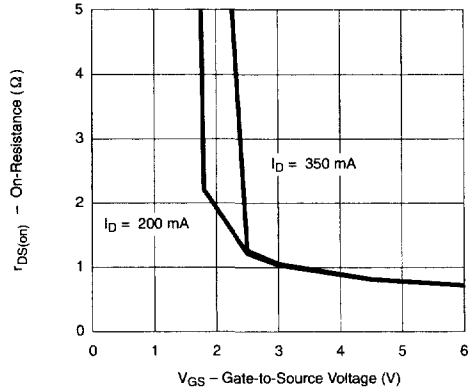
On-Resistance vs. Junction Temperature



Source-Drain Diode Forward Voltage

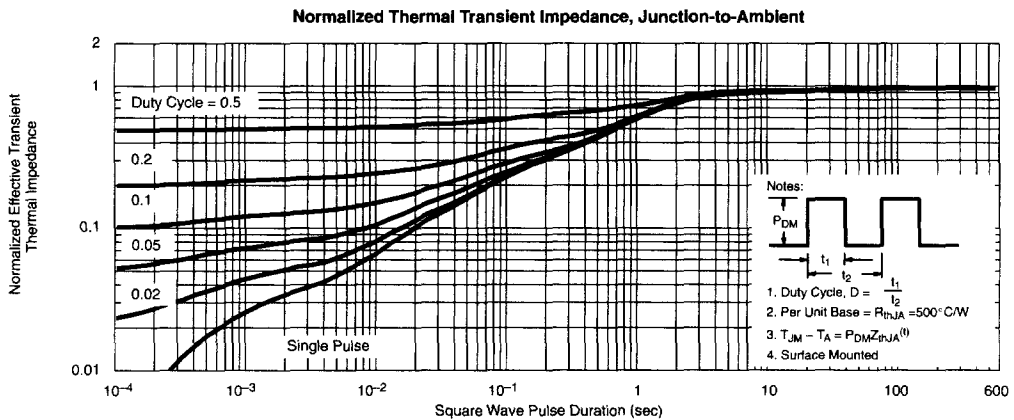
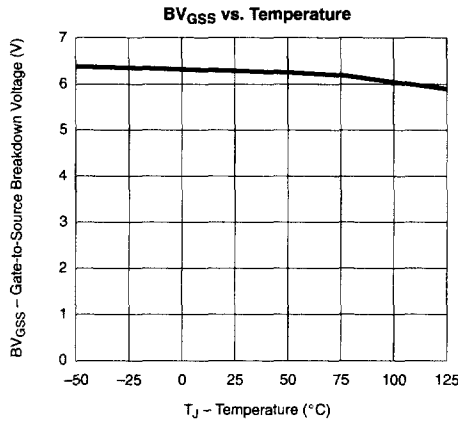
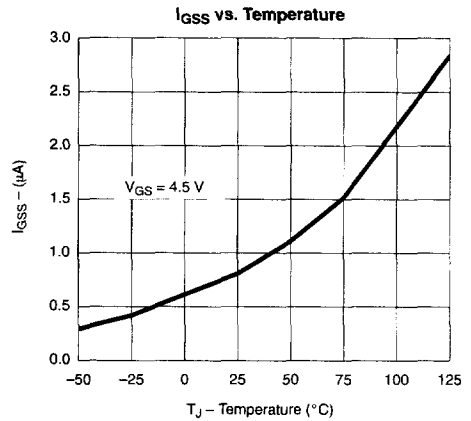
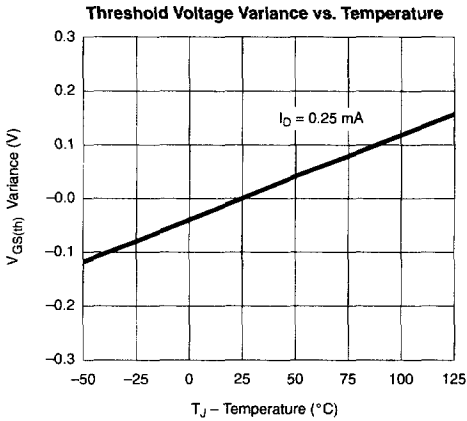


On-Resistance vs. Gate-to-Source Voltage





TYPICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ UNLESS NOTED)



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LITTLE FOOT MOSFETS