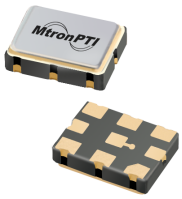
# M31x Series Multiple Frequency VCXO

## 5x7 mm, 3.3/2.5/1.8 Volt, LVPECL/LVDS/CML/HCMOS Output



**Features:**

- Multiple Output Frequencies (2, 3, or 4) - Selectable
- *QiK Chip™* Technology
- Superior Jitter Performance (comparable to SAW based)
- Frequencies from 50 MHz - 1.4 GHz (LVDS/LVPECL/CML) and 10 - 150 MHz (CMOS)

**Phase Lock Loop Applications:**

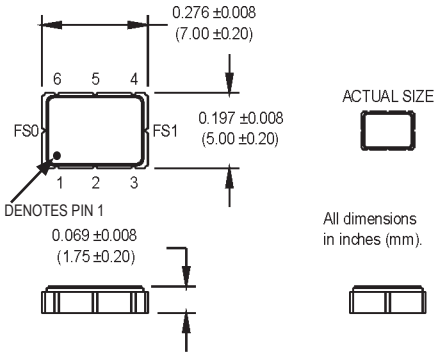
- Where more than one selectable frequency is required for different global regions, FEC (Forward Error Correction) or selectable funcionality are required.
- Telecommunications such as SONET / SDH / DWDM / FEC / SERDES / OC-3 thru OC-192
- Wireless base stations / WLAN / Gigabit Ethernet
- Avionic flight controls and military communications

**Ordering Information**

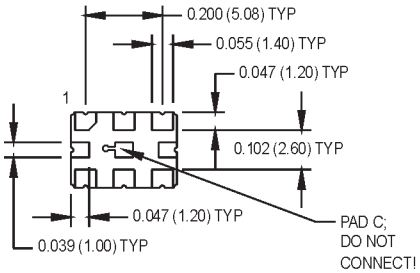
M31 x x x x x x x -SXXX

- **Product Series**
- **Number of Frequencies**
  - **2:** Two Selectable Frequencies
  - **3:** Three Selectable Frequencies
  - **4:** Four Selectable Frequencies
- **Supply Voltage**
  - **0:** 3.3 V
  - **1:** 2.5 V
  - **2:** 1.8 V
- **Operating Temperature**
  - **2:** -40°C to +85°C
  - **6:** -20°C to +70°C
- **Absolute Pull Range (APR)**
  - **A:** ±50 ppm **B:** ±100 ppm
- **Enable/Disable Function**
  - **G:** Enable High (Pad 2)
  - **M:** Enable Low (Pad 2)
- **Logic Type**
  - **P:** LVPECL
  - **L:** LVDS
  - **M:** CML
  - **C:** HCMOS
- **Package/Lead Configuration**
  - **N:** 5 x 7 mm Leadless
- **Factory Assigned to Accommodate Customer Specified Frequencies - Contact Factory**

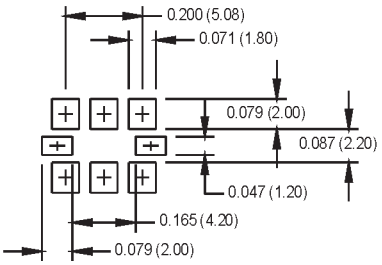
M3120Sxxx, M3121Sxxx, M3122Sxxx
M3130Sxxx, M3131Sxxx, M3132Sxxx
M3140Sxxx, M3141Sxxx, M3142Sxxx
Contact factory for datasheets.




Pad1: Voltage Control
Pad2: Enable/Disable (or N/C)
Pad3: Ground
Pad4: Output Q (LVPECL, LVDS, CML)
Pad5: Output $\overline{Q}$ (LVPECL, LVDS, CML)
Pad6: Vcc
PadA: FS0
PadB: FS1
PadC: Do not connect!




SUGGESTED SOLDER PAD LAYOUT




| Frequency Select Truth Table | | |
|---|---|---|
| | **FS1** | **FS0** |
| Frequency 1 | High | High |
| Frequency 2 | High | Low |
| Frequency 3 | Low | High |
| Frequency 4 | Low | Low |

NOTE: Logic Low = 20% Vcc max.
Logic High = 80% Vcc min.

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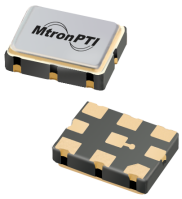
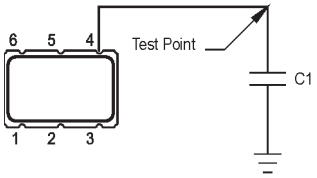
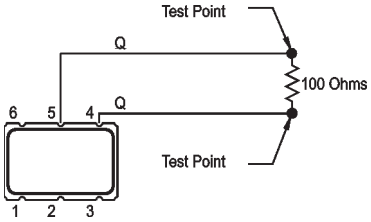


| | PARAMETER | Symbol | Min. | Typ. | Max. | Units | Condition/Notes |
|---|---|---|---|---|---|---|---|
| Electrical Specifications | Frequency Range | F | <br>50<br>10 | | <br>1400<br>125 | <br>MHz<br>MHz | See Note 1<br>LVPECL/LVDS/CML<br>HCMOS |
| | Operating Temperature | TA | -20°C to +70°C or -40°C to +85°C | | | | Customer Specified |
| | Storage Temperature | TS | -55 | | +125 | °C | |
| | Frequency Stability | ΔF/F | | ±25 | | ppm | |
| | Aging<br>1st Year<br>Thereafter (per year) | | <br>-3<br>-1 | | <br>+3<br>+1 | <br>ppm<br>ppm | |
| | Pullability/APR | | ±50 ppm or ±100 ppm | | | | See Note 2–Customer Specified |
| | Gain Transfer Function | | | 90<br>135 | | ppm/V<br>ppm/V | For ± 50 ppm APR<br>For ± 100 ppm APR |
| | Control Voltage | Vc | 0.18<br>0.25<br>0.30 | 0.90<br>1.25<br>1.65 | 1.62<br>2.25<br>3.0 | V<br>V<br>V | @ 1.8V Vcc<br>@ 2.5V Vcc<br>@ 3.3V Vcc |
| | Linearity | | | 1 | 5 | % | Positive Monotonic |
| | Modulation Bandwidth | fm | 20 | | | KHz | -3 dB bandwidth |
| | Input Impedance | Zin | 500k | 1M | | Ohms | @ DC |
| | Supply Voltage | Vcc | 1.71<br>2.375<br>3.135 | 1.8<br>2.5<br>3.3 | 1.89<br>2.625<br>3.465 | V<br>V<br>V | |
| | Input Current | Icc | | | 125<br>80 | mA<br>mA | LVPECL/LVDS/CML<br>HCMOS |
| | Load | | | | | | See Note 3 |
| | | | 50 Ohms to (Vcc –2) Vdc<br>100 Ohm differential load | | | | LVPECL Waveform<br>LVDS/CML Waveform |
| | | | | | 15 | pF | CMOS Waveform |
| | Symmetry (Duty Cycle) | | 45 | | 55 | % | @ 50% of waveform |
| | Output Skew | | | | 80 | ps | LVPECL |
| | | | | | 20 | ps | LVDS, CML |
| | Differential Voltage | | 350<br>0.7 | 425<br>0.95 | 500<br>1.20 | mVppd<br>Vpp | LVDS<br>CML |
| | Common Mode Output Voltage | Vcm | | 1.2 | | V | LVDS |
| | Logic "1" Level | Voh | Vcc -1.02 | | | V | LVPECL |
| | | | 90% Vdd | | | | HCMOS |
| | Logic "0" Level | Vol | | | Vcc -1.63 | V | LVPECL |
| | | | | | 10% Vdd | | HCMOS |
| | Rise/Fall Time | Tr/Tf | | 0.23 | 0.35 | ns | @ 20/80% LVPECL |
| | | | | | 6.0 | ns | Ref. 10%-90% Vdd HCMOS |
| | Enable Function<br>Option G | | 80% Vcc min. or N/C: output active<br>20% Vcc max: output disables to high-Z | | | | Customer Specified (Pad 2) |
| | Enable Function<br>Option M | | 20% Vcc max: output active<br>80% Vcc min: output disables to high-Z | | | | Customer Specified (Pad 2) |
| | Frequency Selection | | See Truth Table | | | | |
| | Settling Time | | | | 10 | ms | To within ± 1 ppm of frequency |
| | Start up Time | | | | 10 | ms | |
| | Phase Jitter<br>@ 622.08 MHz<br>@ 125 MHz | <br>ϕJ<br>ϕJ | | 0.50 | <br><br>1.0 | <br>ps RMS<br>ps RMS | Integrated 12 kHz – 20 MHz<br>HCMOS (12kHz – 20 MHz) |
| Environmental | | | | | | | |
| | Mechanical Shock | Per MIL-STD-202, Method 213, Condition C (100 g's, 6 mS duration, ½ sinewave) | | | | | |
| | Vibration | Per MIL-STD-202, Method 201 & 204 (10 g's from 10-2000 Hz) | | | | | |
| | Hermeticity | Per MIL-STD-202, Method 112, ($1x10^{-8}$ atm. cc/s of Helium) | | | | | |
| | Thermal Cycle | Per MIL-STD-883, Method 1010, Condition B (-55°C to +125°C, 15 min. dwell, 10 cycles) | | | | | |
| | Solderability | Per EIAJ-STD-002 | | | | | |
| | Max. Soldering Cond. | See solder profile, Figure 1 | | | | | |

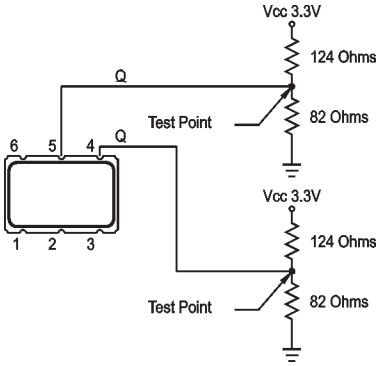
Note 1: Contact factory for exact frequency availability over 945 MHz.
Note 2: APR specification is inclusive of initial tolerance, deviation over temperature, shock, vibration, supply voltage, and aging for one year at 50°C mean ambient temperature.
Note 3: See Load Circuit Diagram in this Datasheet. Consult factory with nonstandard output load requirements.



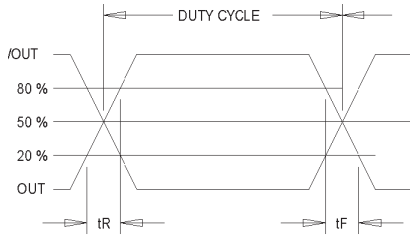

HCMOS Load Circuit




LVDS Load Circuit




3.3 V LVPECL Load Circuit




Output Waveform: LVDS / CML / LVPECL

# MtronPTI Lead Free Solder Profile