High Voltage Synchronous Current Mode Step-Down Controller with Adjustable Operating Frequency

FEATURES

- **High Voltage Operation: Up to 60V**
- **Synchronizable Up to 600kHz**
- **Adjustable Constant Frequency: 100kHz to 500kHz**
- **Output Voltages Up to 36V**
- Adaptive Nonoverlap Circuitry Prevents Switch Shoot-Through
- Reverse Inductor Current Inhibit for Discontinuous Operation Improves Efficiency with Light Loads
- Programmable Soft-Start
- 120µA No Load Quiescent Current
- 10µA Shutdown Supply Current
- 1% Regulation Accuracy
- Standard Gate N-Channel Power MOSFETs
- Current Limit Unaffected by Duty Cycle
- Reverse Overcurrent Protection
- 16-Lead Thermally Enhanced TSSOP Package

APPLICATIONS

- 12V and 42V Automotive and Heavy Equipment
- 48V Telecom Power Supplies
- Avionics and Industrial Control Systems
- Distributed Power Converters

DESCRIPTION

The LT®3845 is a high voltage, synchronous, current mode controller used for medium to high power, high efficiency supplies. It offers a wide 4V to 60V input range (7.5V minimum start-up voltage). An onboard regulator simplifies the biasing requirements by providing IC power directly from V_{IN}.

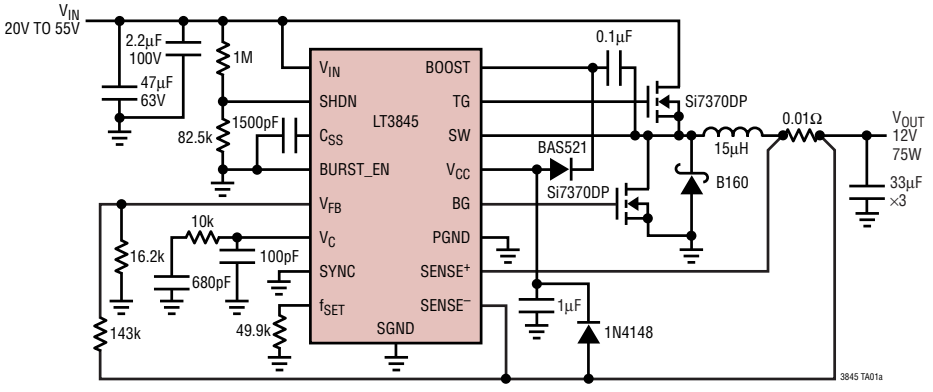
Burst Mode® operation maintains high efficiency at light loads by reducing IC quiescent current to 120µA. Light load efficiency is also improved with the reverse inductor current inhibit function which supports discontinuous operation.

Additional features include adjustable fixed operating frequency that can be synchronized to an external clock for noise sensitive applications, gate drivers capable of driving large N-channel MOSFETs, a precision undervoltage lockout, 10µA shutdown current, short-circuit protection and a programmable soft-start.

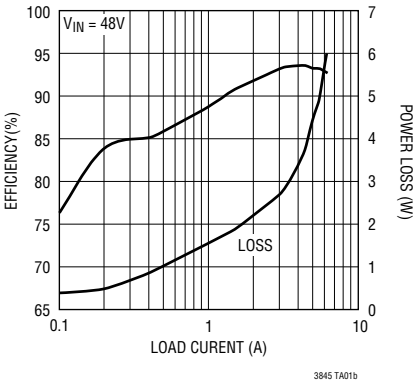
The LT3845 is available in a 16-lead thermally enhanced TSSOP package.

TYPICAL APPLICATION

High Voltage Step-Down Regulator 48V to 12V at 75W



Efficiency and Power Loss vs Load Current

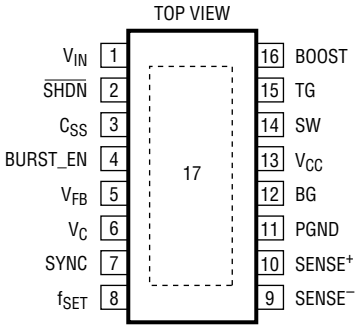


ABSOLUTE MAXIMUM RATINGS

(Note 1)

Input Supply Voltage (V_{IN}) 65V
Boosted Supply Voltage (BOOST) 80V
Switch Voltage (SW) (Note 8) ..... 65V to –2V
Differential Boost Voltage
(BOOST to SW) 24V
Bias Supply Voltage (V_{CC}) 24V
$SENSE^+$ and $SENSE^-$ Voltages 40V
Differential Sense Voltage
($SENSE^+$ to $SENSE^-$) ..... 1V to –1V
BURST_EN Voltage 24V
SYNC, V_C, V_{FB}, C_{SS}, and $\overline{SHDN}$ Voltages 5V
$\overline{SHDN}$ Pin Currents 1mA
Operating Junction Temperature Range (Note 2)
LT3845E (Note 3) ..... –40°C to 125°C
LT3845I ..... –40°C to 125°C
Storage Temperature ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



FE PACKAGE
16-LEAD PLASTIC TSSOP

T_{JMAX} = 125°C, θ_{JA} = 40°C/W, θ_{JC} = 10°C/W
EXPOSED PAD (PIN 17) IS SGND, MUST BE SOLDERED TO PCB

ORDER PART NUMBER	FE PART MARKING*
LT3845EFE LT3845IFE	3845FE 3845FE

Order Options Tape and Reel: Add #TR
Lead Free: Add #PBF Lead Free Tape and Reel: Add #TRPBF
Lead Free Part Marking: http://www.linear.com/leadfree/

Consult LTC Marketing for parts specified with wider operating temperature ranges.
*The temperature grade is identified by a label on the shipping container.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 20V, V_{CC} = BOOST = BURST_EN = 10V, $\overline{SHDN}$ = 2V, R_{SET} = 49.9kΩ, $SENSE^-$ = $SENSE^+$ = 10V, SGND = PGND = SW = SYNC = 0V, unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IN} Operating Voltage Range (Note 4)		●	4		60	V
V_{IN} Minimum Start Voltage		●			7.5	V
V_{IN} UVLO Threshold (Falling)		●	3.6	3.8	4	V
V_{IN} UVLO Threshold Hysteresis				670		mV
V_{IN} Supply Current	V_{CC} > 9V			20		µA
V_{IN} Burst Mode Current	$V_{\overline{BURST\_EN}}$ = 0V, V_{FB} = 1.35V			20		µA
V_{IN} Shutdown Current	V_{SHDN} = 0V	●		9	15	µA
BOOST Operating Voltage Range		●			75	V
BOOST Operating Voltage Range (Note 5)	$V_{BOOST} – V_{SW}$	●			20	V
BOOST UVLO Threshold (Rising)	$V_{BOOST} – V_{SW}$			5		V
BOOST UVLO Threshold Hysteresis	$V_{BOOST} – V_{SW}$			400		mV
BOOST Supply Current (Note 6)				1.4		mA
BOOST Burst Mode Current	$V_{\overline{BURST\_EN}}$ = 0V			0.1		µA
BOOST Shutdown Current	V_{SHDN} = 0V			0.1		µA
V_{CC} Operating Voltage Range (Note 5)		●			20	V
V_{CC} Output Voltage	Over Full Line and Load Range	●		8	8.3	V
V_{CC} UVLO Threshold (Rising)				6.25		V
V_{CC} UVLO Threshold Hysteresis				500		mV
V_{CC} Supply Current (Note 6)		●		3	3.7	mA
V_{CC} Burst Mode Current	$V_{\overline{BURST\_EN}}$ = 0V			100		µA
V_{CC} Shutdown Current	V_{SHDN} = 0V			20		µA
V_{CC} Current Limit		●	–40	–150		mA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 20V, V_{CC} = BOOST = BURST_EN = 10V, $\overline{SHDN}$ = 2V, R_{SET} = 49.9kΩ, $SENSE^-$ = $SENSE^+$ = 10V, SGND = PGND = SW = SYNC = 0V, unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Error Amp Reference Voltage	Measured at V_{FB} Pin	 ●	1.224 1.215	1.231	1.238 1.245	V V
V_{FB} Pin Input Current	V_{FB} = 1.231V			25		nA
$\overline{SHDN}$ Enable Threshold (Rising) $\overline{SHDN}$ Threshold Hysteresis		●	1.3	1.35 120	1.4	V mV
Sense Pins Common Mode Range Current Limit Sense Voltage Reverse Protect Sense Voltage Reverse Current Inhibit Offset	 $V_{SENSE^+} - V_{SENSE^-}$ $V_{SENSE^+} - V_{SENSE^-}$, $V_{BURST\_EN} = V_{CC}$ V_{BURST_EN} = 0V or $V_{BURST\_EN} = V_{FB}$	● ●	0 90	 100 –100 10	36 115	V mV mV mV
Input Current (I_{SENSE^+} + I_{SENSE^-})	$V_{SENSE(CM)}$ = 0V $V_{SENSE(CM)}$ = 2V $V_{SENSE(CM)}$ > 4V			800 –20 –300		µA µA µA
Operating Frequency		 ●	290 270	300	310 330	kHz kHz
Minimum Programmable Frequency Maximum Programmable Frequency		● ●	 500		100	kHz kHz
External Sync Frequency Range		●	100		600	kHz
SYNC Input Resistance				40		kΩ
SYNC Voltage Threshold		●		1.4	2	V
Soft-Start Capacitor Control Current				2		µA
Error Amp Transconductance		●	270	340	410	µS
Error Amp DC Voltage Gain				62		dB
Error Amp Sink/Source Current				±30		µA
TG, BG Drive On Voltage (Note 7) TG, BG Drive Off Voltage	C_{LOAD} = 3300pF C_{LOAD} = 3300pF			9.8 0.1		V V
TG, BG Drive Rise/Fall Time	10% to 90% or 90% to 10%, C_{LOAD} = 3300pF			50		ns
Minimum TG Off Time		●		350	650	ns
Minimum TG On Time		●		250	400	ns
Gate Drive Nonoverlap Time	TG Fall to BG Rise BG Fall to TG Rise			200 150		ns ns

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LT3845 includes overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperature will exceed 125°C when overtemperature protection is active. Continuous operation above the specified maximum operating junction temperature may impair device reliability.

Note 3: The LT3845E is guaranteed to meet performance specifications from 0°C to 125°C junction temperature. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LT3845I is guaranteed over the full –40°C to 125°C operating junction temperature range.

Note 4: V_{IN} voltages below the start-up threshold (7.5V) are only supported when the V_{CC} is externally driven above 6.5V.

Note 5: Operating range is dictated by MOSFET absolute maximum V_{GS}.

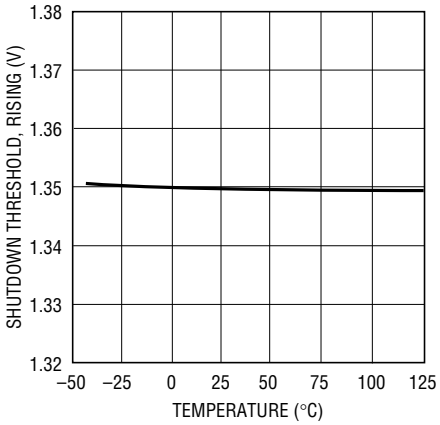
Note 6: Supply current specification does not include switch drive currents. Actual supply currents will be higher.

Note 7: DC measurement of gate drive output "ON" voltage is typically 8.6V. Internal dynamic bootstrap operation yields typical gate "ON" voltages of 9.8V during standard switching operation. Standard operation gate "ON" voltage is not tested but guaranteed by design.

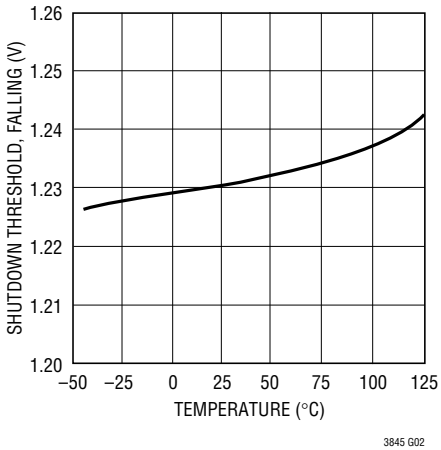
Note 8: The –2V absolute maximum on the SW pin is a transient condition. It is guaranteed by design and not subject to test.

TYPICAL PERFORMANCE CHARACTERISTICS

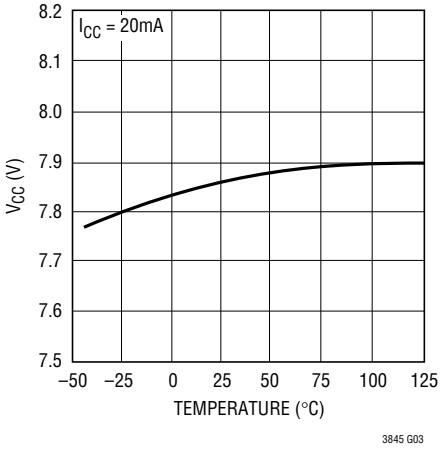
Shutdown Threshold (Rising) vs Temperature



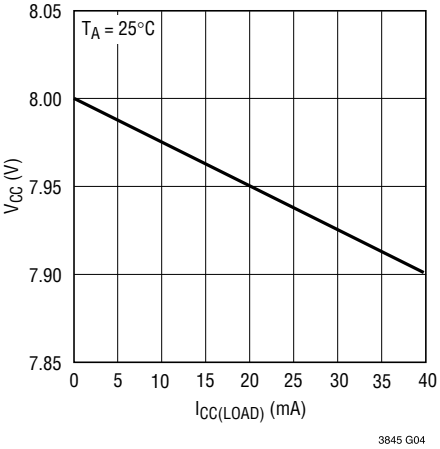
Shutdown Threshold (Falling) vs Temperature



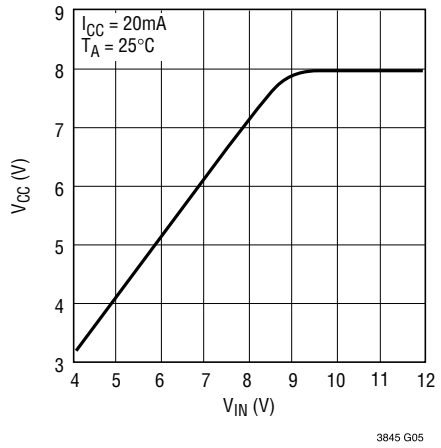
V_{CC} vs Temperature



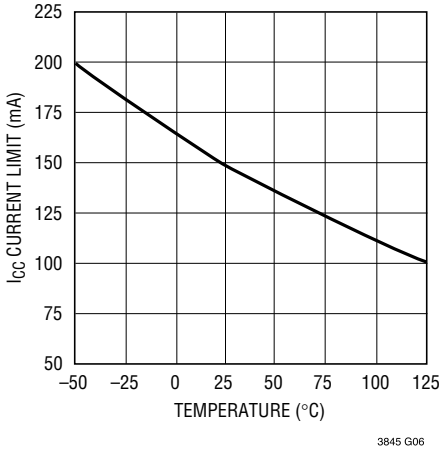
V_{CC} vs $I_{CC(LOAD)}$



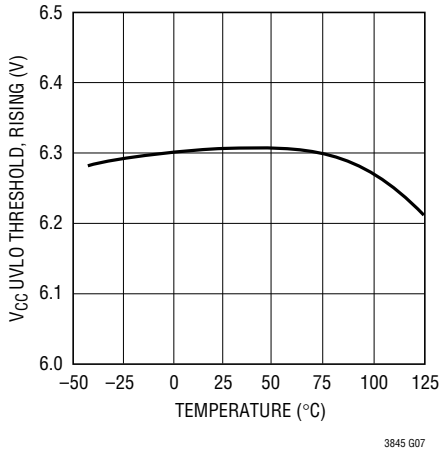
V_{CC} vs V_{IN}



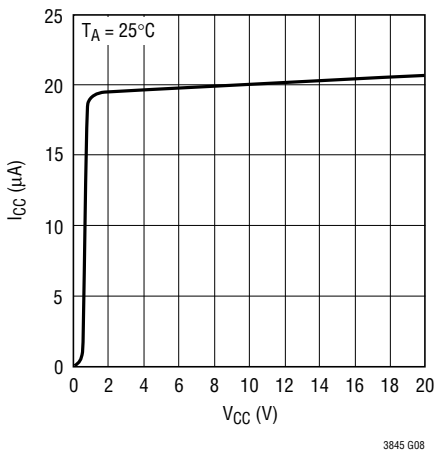
I_{CC} Current Limit vs Temperature



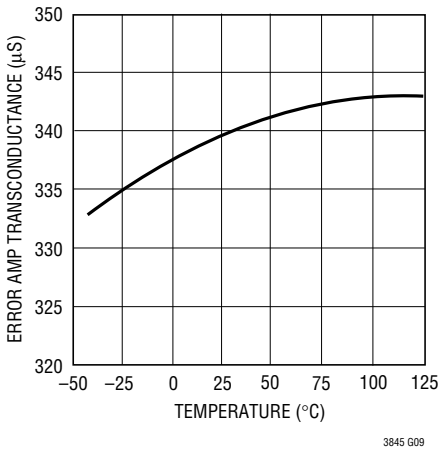
V_{CC} UVLO Threshold (Rising) vs Temperature



I_{CC} vs V_{CC} ($\overline{SHDN}$ = 0V)

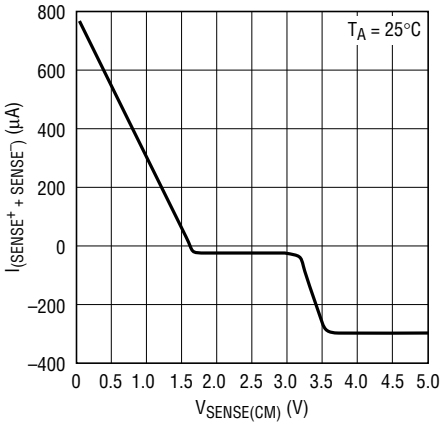


Error Amp Transconductance vs Temperature

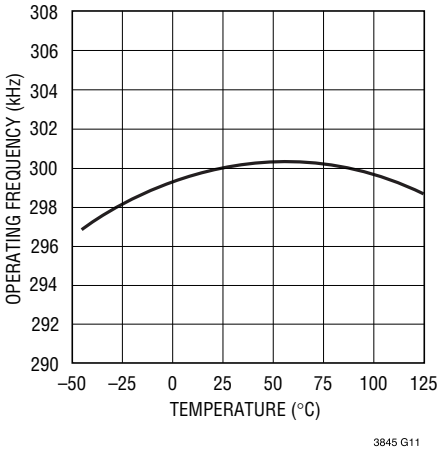


TYPICAL PERFORMANCE CHARACTERISTICS

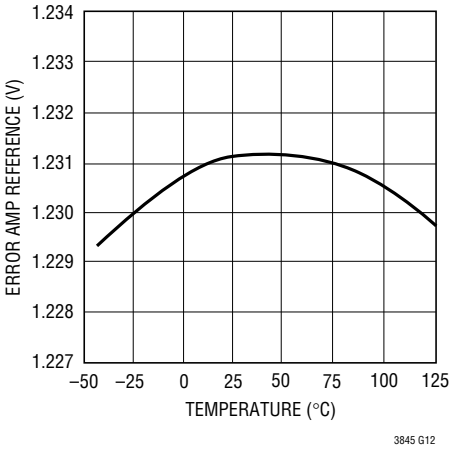
$I_{(SENSE^+ + SENSE^-)}$ vs $V_{SENSE(CM)}$



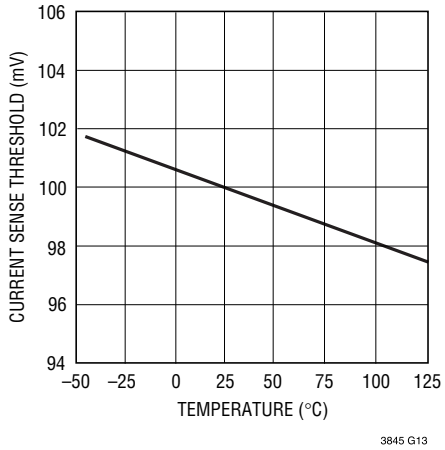
Operating Frequency vs Temperature



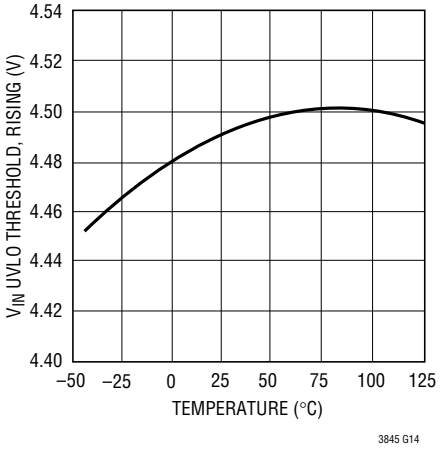
Error Amp Reference vs Temperature



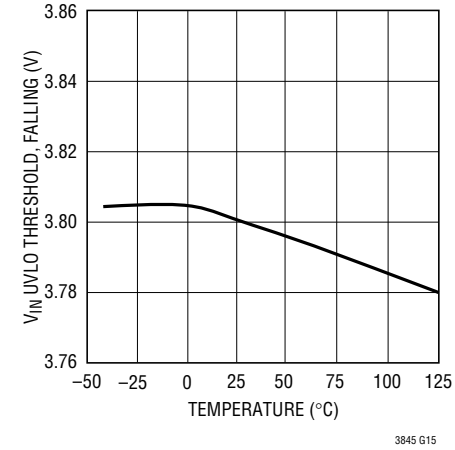
Maximum Current Sense Threshold vs Temperature



V_{IN} UVLO Threshold (Rising) vs Temperature



V_{IN} UVLO Threshold (Falling) vs Temperature



PIN FUNCTIONS

V_{IN} (Pin 1): The V_{IN} pin is the main supply pin and should be decoupled to SGND with a low ESR capacitor (at least 0.1µF) located close to the pin.

$\overline{SHDN}$ (Pin 2): The $\overline{SHDN}$ pin has a precision IC enable threshold of 1.35V (rising) with 120mV of hysteresis. It is used to implement an undervoltage lockout (UVLO) circuit. See Application Information section for implementing a UVLO function. When the $\overline{SHDN}$ pin is pulled below a transistor V_{BE} (0.7V), a low current shutdown mode is entered, all internal circuitry is disabled and the V_{IN} supply current is reduced to approximately 9µA. Typical pin input bias current is <10nA and the pin is internally clamped to 6V. If the function is not used, this pin may be tied to V_{IN} through a high value resistor.

C_{SS} (Pin 3): The soft-start pin is used to program the supply soft-start function. Use the following formula to calculate C_{SS} for a given output voltage slew rate:

$$C_{SS} = 2\mu A(t_{SS}/1.231V)$$

The pin should be left unconnected when not using the soft-start function.

BURST_EN (Pin 4): Burst Mode Operation Enable Pin. This pin also controls reverse-current inhibit mode of operation. When the pin voltage is below 0.5V, Burst Mode operation and reverse-current inhibit functions are enabled. When the pin voltage is above 0.5V, Burst Mode operation is disabled, but reverse-current inhibit operation is maintained. In this mode of operation (BURST_EN = V_{FB}) there is a 1mA minimum load requirement. Reverse-current inhibit is disabled when the pin voltage is above 2.5V. This pin is typically shorted to ground to enable Burst Mode operation and reverse-current inhibit, shorted to V_{FB} to disable Burst Mode operation while enabling reverse-current inhibit, and connected to V_{CC} pin to disable both functions. See Applications Information section.

V_{FB} (Pin 5): The output voltage feedback pin, V_{FB}, is externally connected to the supply output voltage via a resistive divider. The V_{FB} pin is internally connected to the inverting input of the error amplifier. In regulation, V_{FB} is 1.231V.

V_C (Pin 6): The V_C pin is the output of the error amplifier whose voltage corresponds to the maximum (peak) switch current per oscillator cycle. The error amplifier is typically configured as an integrator by connecting an RC network from the V_C pin to SGND. This circuit creates the dominant pole for the converter regulation control loop. Specific integrator characteristics can be configured to optimize transient response. When Burst Mode operation is enabled (see Pin 4 description), an internal low impedance clamp on the V_C pin is set at 100mV below the burst threshold, which limits the negative excursion of the pin voltage. Therefore, this pin cannot be pulled low with a low impedance source. If the V_C pin must be externally manipulated, do so through a 1kΩ series resistance.

SYNC (Pin 7): The Sync pin provides an external clock input for synchronization of the internal oscillator. R_{SET} is set such that the internal oscillator frequency is 10% to 25% below the external clock frequency. If unused the Sync pin is connected to SGND. For more information see "Oscillator Sync" in the Application Information section of this datasheet.

f_{SET} (Pin 8): The f_{SET} pin programs the oscillator frequency with an external resistor, R_{SET}. The resistor is required even when supplying external sync clock signal. See the Applications Information section for resistor value selection details.

$SENSE^-$ (Pin 9): The $SENSE^-$ pin is the negative input for the current sense amplifier and is connected to the V_{OUT} side of the sense resistor for step-down applications. The sensed inductor current limit is set to ±100mV across the SENSE inputs.

$SENSE^+$ (Pin 10): The $SENSE^+$ pin is the positive input for the current sense amplifier and is connected to the inductor side of the sense resistor for step-down applications. The sensed inductor current limit is set to ±100mV across the SENSE inputs.

PGND (Pin 11): The PGND pin is the high-current ground reference for internal low side switch driver and the V_{CC} regulator circuit. Connect the pin directly to the negative terminal of the V_{CC} decoupling capacitor. See the Application Information section for helpful hints on PCB layout of grounds.

PIN FUNCTIONS

BG (Pin 12): The BG pin is the gate drive for the bottom N-channel MOSFET. Since very fast high currents are driven from this pin, connect it to the gate of the power MOSFET with a short and wide, typically 0.02" width, PCB trace to minimize inductance.

V_{CC} (Pin 13): The V_{CC} pin is the internal bias supply decoupling node. Use a low ESR, 1µF or greater ceramic capacitor to decouple this node to PGND. Most internal IC functions are powered from this bias supply. An external diode connected from V_{CC} to the BOOST pin charges the bootstrapped capacitor during the off-time of the main power switch. Back driving the V_{CC} pin from an external DC voltage source, such as the V_{OUT} output of the regulator supply, increases overall efficiency and reduces power dissipation in the IC. In shutdown mode this pin sinks 20µA until the pin voltage is discharged to 0V.

SW (Pin 14): Reference for V_{BOOST} Supply and High Current Return for Bootstrapped Switch.

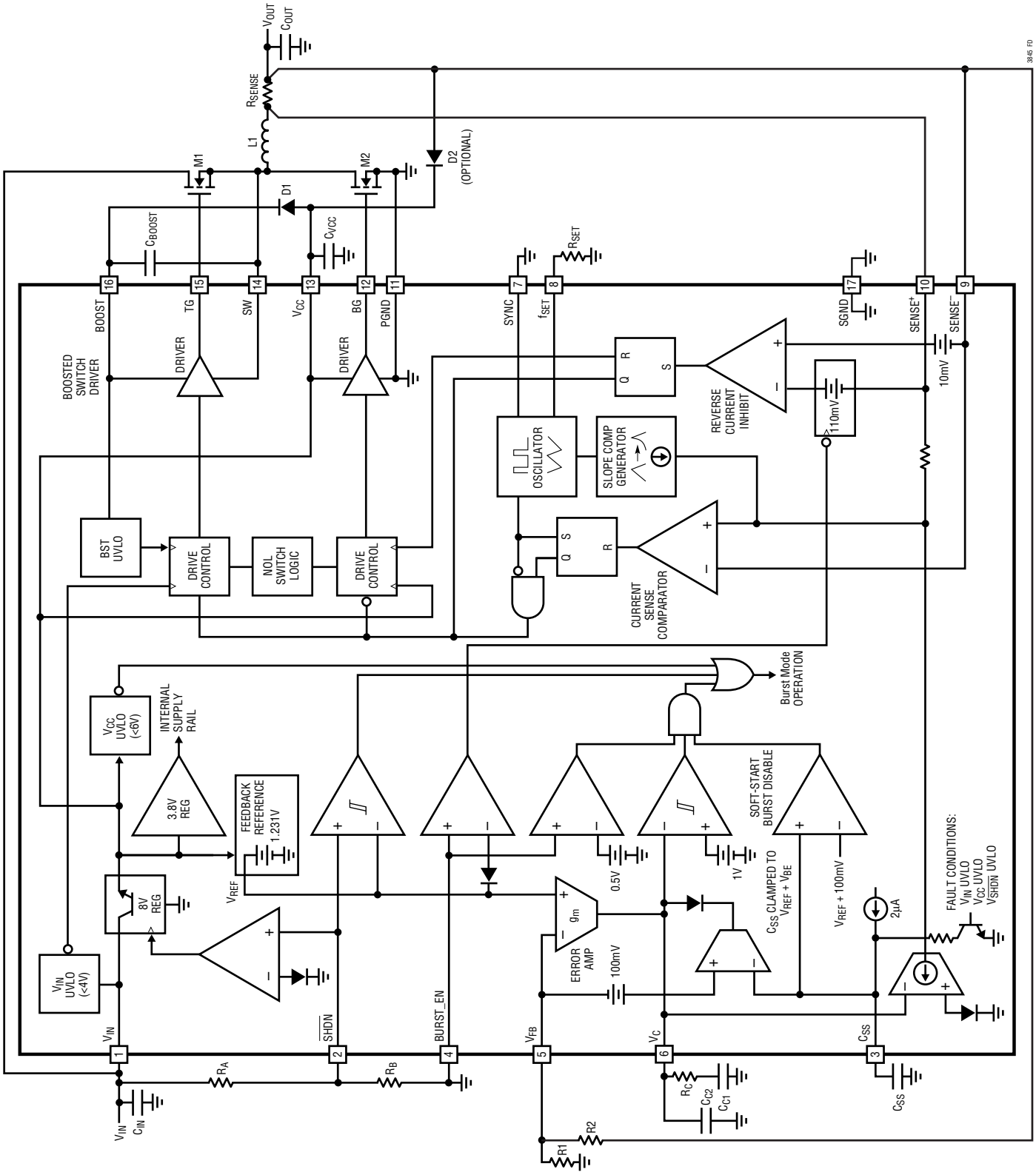
TG (Pin 15): The TG pin is the bootstrapped gate drive for the top N-Channel MOSFET. Since very fast high currents are driven from this pin, connect it to the gate of the power MOSFET with a short and wide, typically 0.02" width, PCB trace to minimize inductance.

BOOST (Pin 16): The BOOST pin is the supply for the bootstrapped gate drive and is externally connected to a low ESR ceramic boost capacitor referenced to SW pin. The recommended value of the BOOST capacitor,C_{BOOST}, is at least 50 times greater than the total gate capacitance of the topside MOSFET. In most applications 0.1µF is adequate. The maximum voltage that this pin sees is V_{IN} + V_{CC}, ground referred.

SGND (Pin 17): The SGND pin is the low noise ground reference. It should be connected to the $-V_{OUT}$ side of the output capacitors. Careful layout of the PCB is necessary to keep high currents away from this SGND connection. See the Application Information section for helpful hints on PCB layout of grounds.

Exposed Pad (SGND) (Pin 17): The exposed leadframe is internally connected to the SGND pin. Solder the exposed pad to the PCB ground for electrical contact and optimal thermal performance.

BLOCK DIAGRAM



APPLICATIONS INFORMATION

Overview

The LT3845 is a high input voltage range step-down synchronous DC/DC converter controller IC that uses a programmable constant frequency, current mode architecture with external N-channel MOSFET switches.

The LT3845 has provisions for high efficiency, low load operation for battery-powered applications. Burst Mode operation reduces total average input quiescent currents to 120µA during no load conditions. A low current shutdown mode can also be activated, reducing quiescent current to 10µA. Burst Mode operation can be disabled if desired.

A reverse-current inhibit feature allows increased efficiencies during light loads through nonsynchronous operation. This feature disables the synchronous switch if inductor current approaches zero. If full time synchronous operation is desired, this feature can be disabled.

Much of the IC's internal circuitry is biased from an internal linear regulator. The output of this regulator is the V_{CC} pin, allowing bypassing of the internal regulator. The associated internal circuitry can be powered from the output of the converter, increasing overall converter efficiency. Using externally derived power also eliminates the IC's power dissipation associated with the internal V_{IN} to V_{CC} regulator.

Theory of Operation (See Block Diagram)

The LT3845 senses converter output voltage via the V_{FB} pin. The difference between the voltage on this pin and an internal 1.231V reference is amplified to generate an error voltage on the V_C pin which is used as a threshold for the current sense comparator.

During normal operation, the LT3845 internal oscillator runs at the programmed frequency. At the beginning of each oscillator cycle, the switch drive is enabled. The switch drive stays enabled until the sensed switch current exceeds the V_C derived threshold for the current sense comparator and, in turn, disables the switch driver. If the current comparator threshold is not obtained for the entire oscillator cycle, the switch driver is disabled at the end of the cycle for 350ns, typical. This minimum off-time mode of operation assures regeneration of the BOOST bootstrapped supply.

Power Requirements

The LT3845 is biased using an internal linear regulator to generate operational voltages from the V_{IN} pin. Virtually all of the circuitry in the LT3845 is biased via this internal linear regulator output (V_{CC}). This pin is decoupled with a low ESR, 1µF capacitor to PGND.

The V_{CC} regulator generates an 8V output provided there is ample voltage on the V_{IN} pin. The V_{CC} regulator has approximately 1V of dropout, and will follow the V_{IN} pin with voltages below the dropout threshold.

The LT3845 has a start-up requirement of $V_{IN} > 7.5V$. This assures that the onboard regulator has ample headroom to bring the V_{CC} pin above its UVLO threshold. The V_{CC} regulator can only source current, so forcing the V_{CC} pin above its 8V regulated voltage allows use of externally derived power for the IC, minimizing power dissipation in the IC. Using the onboard regulator for start-up, then deriving power for V_{CC} from the converter output maximizes conversion efficiencies and is common practice. If V_{CC} is maintained above 6.5V using an external source, the LT3845 can continue to operate with V_{IN} as low as 4V.

The LT3845 operates with 3mA quiescent current from the V_{CC} supply. This current is a fraction of the actual V_{CC} quiescent currents during normal operation. Additional current is produced from the MOSFET switching currents for both the boosted and synchronous switches and are typically derived from the V_{CC} supply.

Because the LT3845 uses a linear regulator to generate V_{CC}, power dissipation can become a concern with high V_{IN} voltages. Gate drive currents are typically in the range of 5mA to 15mA per MOSFET, so gate drive currents can create substantial power dissipation. It is advisable to derive V_{CC} and V_{BOOST} power from an external source whenever possible.

The onboard V_{CC} regulator will provide gate drive power for start-up under all conditions with total MOSFET gate charge loads up to 180nC. The regulator can operate the LT3845 continuously, provided the power dissipation of the regulator does not exceed 250mW. The power dissipaton of the regulator is calculated as follows:

$$P_{D(REG)} = (V_{IN} - 8V) \bullet (f_{SW} \bullet Q_{G(TOTAL)} + 3mA)$$

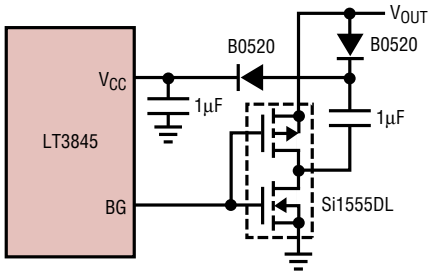
APPLICATIONS INFORMATION

where $Q_{G(TOTAL)}$ is the total MOSFET gate charge of the TG and BG.

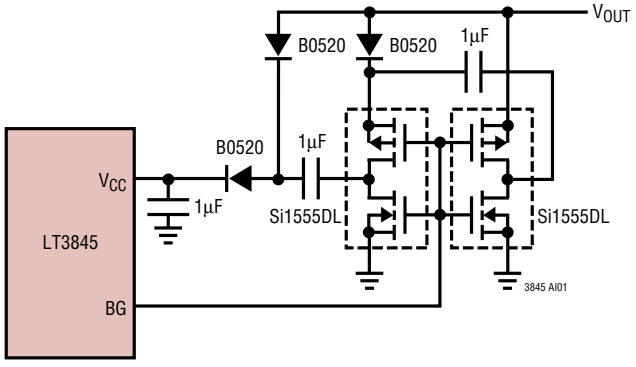
In applications where these conditions are exceeded, V_{CC} must be derived from an external source after start-up. Maximum continuous regulator power dissipation may be exceeded for short duration V_{IN} transients.

In LT3845 converter applications with output voltages in the 9V to 20V range, back-feeding V_{CC} and V_{BOOST} from the converter output is trivial, accomplished by connecting diodes from the output to these supply pins. Deriving these supplies from output voltages greater than 20V will require additional regulation to reduce the feedback voltage. Outputs lower than 9V will require step-up techniques to increase the feedback voltage to something greater than the 8V V_{CC} regulated output. Low power boost switchers are sometimes used to provide the step-up function, but a simple charge-pump can perform this function in many instances.

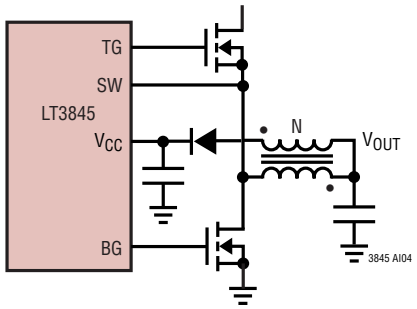
Charge Pump Doubler



Charge Pump Tripler



Inductor Auxiliary Winding



Burst Mode

The LT3845 employs low current Burst Mode functionality to maximize efficiency during no load and low load conditions. Burst Mode operation is enabled by shorting the BURST_EN pin to SGND. Burst Mode operation can be disabled by shorting BURST_EN to either V_{FB} or V_{CC}.

When the required switch current, sensed via the V_C pin voltage, is below 15% of maximum, the Burst Mode operation is employed and that level of sense current is latched onto the IC control path. If the output load requires less than this latched current level, the converter will overdrive the output slightly during each switch cycle. This overdrive condition is sensed internally and forces the voltage on the V_C pin to continue to drop. When the voltage on V_C drops 150mV below the 15% load level, switching is disabled and the LT3845 shuts down most of its internal circuitry, reducing total quiescent current to 120µA. When the converter output begins to fall, the V_C pin voltage begins to climb. When the voltage on the V_C pin climbs back to the 15% load level, the IC returns to normal operation and switching resumes. An internal clamp on the V_C pin is set at 100mV below the switch disable threshold, which limits the negative excursion of the pin voltage, minimizing the converter output ripple during Burst Mode operation.

During Burst Mode operation, V_{IN} pin current is 20µA and V_{CC} current is reduced to 100µA. If no external drive is provided for V_{CC}, all V_{CC} bias currents originate from the

APPLICATIONS INFORMATION

V_{IN} pin, giving a total V_{IN} current of 120µA. Burst current can be reduced further when V_{CC} is driven using an output derived source, as the V_{CC} component of V_{IN} current is then reduced by the converter buck ratio.

Reverse-Current Inhibit

The LT3845 contains a reverse-current inhibit feature to maximize efficiency during light load conditions. This mode of operation allows discontinuous operation and pulse-skipping mode at light loads. Refer to Figure 1.

This feature is enabled with Burst Mode operation, and can also be enabled while Burst Mode operation is disabled by shorting the BURST_EN pin to V_{FB}.

When reverse-current inhibit is enabled, the LT3845 sense amplifier detects inductor currents approaching zero and disables the synchronous switch for the remainder of the switch cycle. If the inductor current is allowed to go negative before the synchronous switch is disabled, the switch node could inductively kick positive with a high dv/dt. The LT3845 prevents this by incorporating a 10mV positive offset at the sense inputs.

With the reverse-current inhibit feature enabled, an LT3845 converter will operate much like a nonsynchronous converter during light loads. Reverse-current inhibit reduces resistive losses associated with inductor ripple currents, which improves operating efficiencies during light-load conditions.

An LT3845 DC/DC converter that is operating in reverse-current inhibit mode has a minimum load requirement of 1mA (BURST_EN = V_{FB}). Since most applications use output-generated power for the LT3845, this requirement is met by the bias currents of the IC, however, for applications that do not derive power from the output, this requirement is easily accomplished by using a 1.2k resistor connected from V_{FB} to ground as one of the converter output voltage programming resistors (R1). There are no minimum load restrictions when in Burst Mode operation (BURST_EN < 0.5V) or continuous conduction mode (BURST_EN > 2.5V).

Soft-Start

The soft-start function controls the slew rate of the power supply output voltage during start-up. A controlled output voltage ramp minimizes output voltage overshoot, reduces inrush current from the V_{IN} supply, and facilitates supply sequencing. A capacitor, C_{SS}, connected from the C_{SS} pin to SGND, programs the slew rate. The capacitor is charged from an internal 2µA current source producing a ramped voltage. The capacitor voltage overrides the internal reference to the error amplifier. If the V_{FB} pin voltage exceeds the C_{SS} pin voltage then the current threshold set by the DC control voltage, V_C, is decreased and the inductor current is lowered. This in turn decreases the output voltage slew rate allowing the C_{SS} pin voltage ramp to catch up to the V_{FB} pin voltage. An internal 100mV offset is added to the V_{FB} pin voltage relative to the C_{SS} pin voltage so that

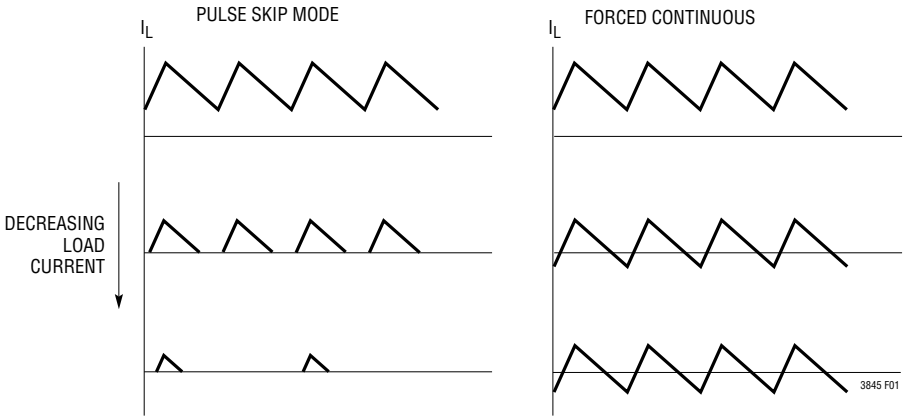


Figure 1. Inductor Current vs Mode

APPLICATIONS INFORMATION

at start-up the soft-start circuit will discharge the V_C pin voltage below the DC control voltage equivalent to zero inductor current. This will reduce the input supply inrush current. The soft-start circuit is disabled once the C_{SS} pin voltage has been charged to 200mV above the internal reference of 1.231V.

During a V_{IN} UVLO, V_{CC} UVLO or $\overline{SHDN}$ UVLO event, the C_{SS} pin voltage is discharged with a 50µA current source. In normal operation the C_{SS} pin voltage is clamped to a diode above the V_{FB} pin voltage. Therefore, the value of the C_{SS} capacitor is relevant to how long of a fault event will retrigger a soft-start. If any of the above UVLO conditions occur, the C_{SS} pin voltage will be discharged with a 50µA current source. There is a diode worth of voltage headroom to ride through the fault before the C_{SS} pin voltage enters its active region and the soft-start function is enabled.

Also, since the C_{SS} pin voltage is clamped to a diode above the V_{FB} pin voltage, during a short circuit the C_{SS} pin voltage is pulled low because the V_{FB} pin voltage is low. Once the short has been removed the V_{FB} pin voltage starts to recover. The soft-start circuit takes control of the output voltage slew rate once the V_{FB} pin voltage has exceeded the slowly ramping C_{SS} pin voltage, reducing the output voltage overshoot during a short circuit recovery.

Adaptive Nonoverlap (NOL) Output Stage

The FET driver output stages implement adaptive nonoverlap control. This feature maintains a constant dead time, preventing shoot-through switch currents, independent of the type, size or operating conditions of the external switch elements.

Each of the two switch drivers contains a NOL control circuit, which monitors the output gate drive signal of the other switch driver. The NOL control circuits interrupt the "turn on" command to their associated switch driver until the other switch gate is fully discharged.

Antislope Compensation

Most current mode switching controllers use slope compensation to prevent current mode instability. The LT3845 is no exception. A slope-compensation circuit imposes an artificial ramp on the sensed current to increase the rising slope as duty cycle increases. Unfortunately, this additional ramp corrupts the sensed current value, reducing the achievable current limit value by the same amount as the added ramp represents. As such, current limit is typically reduced as duty cycles increase. The LT3845 contains circuitry to eliminate the current limit reduction typically associated with slope compensation. As the slope-compensation ramp is added to the sensed current, a similar ramp is added to the current limit threshold reference. The end result is that current limit is not compromised, so an LT3845 converter can provide full power regardless of required duty cycle.

Shutdown

The LT3845 $\overline{SHDN}$ pin uses a bandgap generated reference threshold of 1.35V. This precision threshold allows use of the $\overline{SHDN}$ pin for both logic-level controlled applications and analog monitoring applications such as power supply sequencing.

The LT3845 operational status is primarily controlled by a UVLO circuit on the V_{CC} regulator pin. When the IC is enabled via the $\overline{SHDN}$ pin, only the V_{CC} regulator is enabled. Switching remains disabled until the UVLO threshold is achieved at the V_{CC} pin, when the remainder of the IC is enabled and switching commences.

Because an LT3845 controlled converter is a power transfer device, a voltage that is lower than expected on the input supply could require currents that exceed the sourcing capabilities of that supply, causing the system to lock up in an undervoltage state. Input supply start-up protection can be achieved by enabling the $\overline{SHDN}$ pin using a resistive divider from the V_{IN} supply to ground. Setting the divider output to 1.35V when that supply is at an adequate voltage prevents an LT3845 converter from drawing large currents until the input supply is able to provide the required power. 120mV of input hysteresis on the $\overline{SHDN}$ pin allows for almost 10% of input supply droop before disabling the converter.

R_{SENSE} Selection

The current sense resistor, R_{SENSE}, monitors the inductor current of the supply (See Typical Application on front page). Its value is chosen based on the maximum required output load current. The LT3845 current sense amplifier

APPLICATIONS INFORMATION

has a maximum voltage threshold of, typically, 100mV. Therefore, the peak inductor current is 100mV/R_{SENSE}. The maximum output load current, $I_{OUT(MAX)}$, is the peak inductor current minus half the peak-to-peak ripple current, ΔI_L.

Allowing adequate margin for ripple current and external component tolerances, R_{SENSE} can be calculated as follows:

$$R_{SENSE} = \frac{70mV}{I_{OUT(MAX)}}$$

Typical values for R_{SENSE} are in the range of 0.005Ω to 0.05Ω.

Operating Frequency

The choice of operating frequency is a trade off between efficiency and component size. Low frequency operation improves efficiency by reducing MOSFET switching losses and gate charge losses. However, lower frequency operation requires more inductance for a given amount of ripple current, resulting in a larger inductor size and higher cost. If the ripple current is allowed to increase, larger output capacitors may be required to maintain the same output ripple. For converters with high step-down V_{IN} to V_{OUT} ratios, another consideration is the minimum on-time of the LT3845 (see the Minimum On-time Considerations section). A final consideration for operating frequency is that in noise-sensitive communications systems, it is often desirable to keep the switching noise out of a sensitive frequency band. The LT3845 uses a constant frequency architecture that can be programmed over a 100kHz to 500kHz range with a single resistor from the f_{SET} pin to ground, as shown in Figure 2. The nominal voltage on the f_{SET} pin is 1V and the current that flows from this pin is used to charge an internal oscillator capacitor. The value of R_{SET} for a given operating frequency can be chosen from Figure 2 or from the following equation:

$$R_{SET(k\Omega)} = 8.4 \bullet 10^4 \bullet f_{SW}^{(-1.31)}$$

Table 1 lists typical resistor values for common operating frequencies.

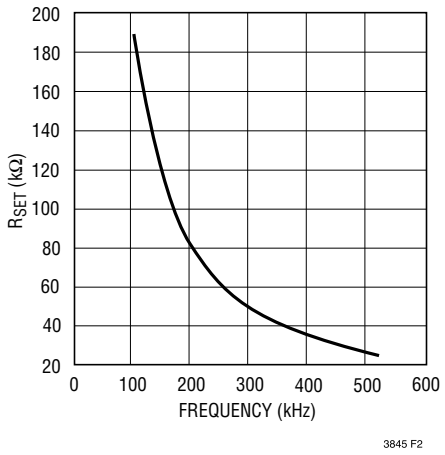


Figure 2. Timing Resistor (R_{SET}) Value

Table 1. Recommended 1% Standard Values

R_{SET}	f_{SW}
191kΩ	100kHz
118kΩ	150kHz
80.6kΩ	200kHz
63.4kΩ	250kHz
49.9kΩ	300kHz
40.2kΩ	350kHz
33.2kΩ	400kHz
27.4kΩ	450kHz
23.2kΩ	500kHz

Inductor Selection

The critical parameters for selection of an inductor are minimum inductance value, volt-second product, saturation current and/or RMS current.

For a given ΔI_L, The minimum inductance value is calculated as follows:

$$L \geq V_{OUT} \bullet \frac{V_{IN(MAX)} - V_{OUT}}{f_{SW} \bullet V_{IN(MAX)} \bullet \Delta I_L}$$

f_{SW} is the switch frequency.

The typical range of values for ΔI_L is $(0.2 \bullet I_{OUT(MAX)})$ to $(0.5 \bullet I_{OUT(MAX)})$, where $I_{OUT(MAX)}$ is the maximum load current of the supply. Using $\Delta I_L = 0.3 \bullet I_{OUT(MAX)}$ yields a good design compromise between inductor performance versus inductor size and cost. A value of $\Delta I_L = 0.3 \bullet I_{OUT(MAX)}$ produces a ±15% of $I_{OUT(MAX)}$ ripple current around the DC output current of the supply. Lower values of ΔI_L require larger and more costly magnetics. Higher values of ΔI_L

APPLICATIONS INFORMATION

will increase the peak currents, requiring more filtering on the input and output of the supply. If ΔI_L is too high, the slope compensation circuit is ineffective and current mode instability may occur at duty cycles greater than 50%. To satisfy slope compensation requirements the minimum inductance is calculated as follows:

$$L_{MIN} > V_{OUT} \bullet \frac{2DC_{MAX} - 1}{DC_{MAX}} \bullet \frac{R_{SENSE} \bullet 8.33}{f_{SW}}$$

The magnetics vendors specify either the saturation current, the RMS current or both. When selecting an inductor based on inductor saturation current, use the peak current through the inductor, $I_{OUT(MAX)} + \Delta I_L/2$. The inductor saturation current specification is the current at which the inductance, measured at zero current, decreases by a specified amount, typically 30%.

When selecting an inductor based on RMS current rating, use the average current through the inductor, $I_{OUT(MAX)}$. The RMS current specification is the RMS current at which the part has a specific temperature rise, typically 40°C, above 25°C ambient.

After calculating the minimum inductance value, the volt-second product, the saturation current and the RMS current for your design, select an off-the-shelf inductor. Contact the Application group at Linear Technology for further support.

For more detailed information on selecting an inductor, please see the "Inductor Selection" section of Linear Technology Application Note 44.

MOSFET Selection

The selection criteria of the external N-channel standard level power MOSFETs include on resistance ($R_{DS(ON)}$), reverse transfer capacitance (C_{RSS}), maximum drain source voltage (V_{DSS}), total gate charge (Q_G) and maximum continuous drain current.

For maximum efficiency, minimize $R_{DS(ON)}$ and C_{RSS}. Low $R_{DS(ON)}$ minimizes conduction losses while low C_{RSS} minimizes transition losses. The problem is that $R_{DS(ON)}$ is inversely related to C_{RSS}. In selecting the top MOSFET balancing the transition losses with the conduction losses is a good idea while the bottom MOSFET is dominated by the conduction loss, which is worse during a short-circit condition or at a very low duty cycle.

Calculate the maximum conduction losses of the MOSFETs:

$$P_{COND(TOP)} = I_{OUT(MAX)}^2 \bullet \frac{V_{OUT}}{V_{IN}} \bullet R_{DS(ON)}$$

$$P_{COND(BOT)} = I_{OUT(MAX)}^2 \bullet \frac{V_{IN} - V_{OUT}}{V_{IN}} \bullet R_{DS(ON)}$$

Note that $R_{DS(ON)}$ has a large positive temperature dependence. The MOSFET manufacturer's data sheet contains a curve, $R_{DS(ON)}$ vs Temperature.

In the main MOSFET, transition losses are proportional to V_{IN}^2 and can be considerably large in high voltage applications (V_{IN} > 20V). Calculate the maximum transition losses:

$$P_{TRAN(TOP)} = k \bullet V_{IN}^2 \bullet I_{OUT(MAX)} \bullet C_{RSS} \bullet f_{SW}$$

where k is a constant inversely related to the gate driver current, approximated by k = 2 for LT3845 applications.

The total maximum power dissipations of the MOSFET are:

$$P_{TOP(TOTAL)} = P_{COND(MAIN)} + P_{TRAN(MAIN)}$$

$$P_{BOT(TOTAL)} = P_{COND(SYNC)}$$

To achieve high supply efficiency, keep the total power dissipation in each switch to less than 3% of the total output power. Also, complete a thermal analysis to ensure that the MOSFET junction temperature is not exceeded.

$$T_J = T_A + P_{(TOTAL)} \bullet \theta_{JA}$$

where θ_{JA} is the package thermal resistance and T_A is the ambient temperature. Keep the calculated T_J below the maximum specified junction temperature, typically 150°C.

Note that when V_{IN} is high and f_{SW} is high, the transition losses may dominate. A MOSFET with higher $R_{DS(ON)}$ and lower C_{RSS} may provide higher efficiency. MOSFETs with higher voltage V_{DSS} specification usually have higher $R_{DS(ON)}$ and lower C_{RSS}.

APPLICATIONS INFORMATION

Choose the MOSFET V_{DSS} specification to exceed the maximum voltage across the drain to the source of the MOSFET, which is $V_{IN(MAX)}$ plus any additional ringing on the switch node. Ringing on the switch node can be greatly reduced with good PCB layout and, if necessary, an RC snubber.

In some applications, parasitic FET capacitances couple the negative going switch node transient onto the bottom gate drive pin of the LT3845, causing a negative voltage in excess of the Absolute Maximum Rating to be imposed on that pin. Connection of a catch Schottky diode from this pin to ground will eliminate this effect. A 1A current rating is typically sufficient of the diode.

The internal V_{CC} regulator is capable of sourcing up to 40mA limiting the maximum total MOSFET gate charge, Q_G, to 35mA/f_{SW}. The Q_G vs V_{GS} specification is typically provided in the MOSFET data sheet. Use Q_G at V_{GS} of 8V. If V_{CC} is back driven from an external supply, the MOSFET drive current is not sourced from the internal regulator of the LT3845 and the Q_G of the MOSFET is not limited by the IC. However, note that the MOSFET drive current is supplied by the internal regulator when the external supply back driving V_{CC} is not available such as during start-up or short circuit.

The manufacturer's maximum continuous drain current specification should exceed the peak switch current, $I_{OUT(MAX)} + \Delta I_L/2$.

During the supply start-up, the gate drive levels are set by the V_{CC} voltage regulator, which is approximately 8V. Once the supply is up and running, the V_{CC} can be back driven by an auxiliary supply such as V_{OUT}. It is important not to exceed the manufacturer's maximum V_{GS} specification. A standard level threshold MOSFET typically has a V_{GS} maximum of 20V.

Input Capacitor Selection

A local input bypass capacitor is required for buck converters because the input current is pulsed with fast rise and fall times. The input capacitor selection criteria are based on the bulk capacitance and RMS current capability. The bulk capacitance will determine the supply input ripple voltage. The RMS current capability is used to prevent overheating the capacitor.

The bulk capacitance is calculated based on maximum input ripple, ΔV_{IN}:

$$C_{IN(BULK)} = \frac{I_{OUT(MAX)} \bullet V_{OUT}}{\Delta V_{IN} \bullet f_{SW} \bullet V_{IN(MIN)}}$$

ΔV_{IN} is typically chosen at a level acceptable to the user. 100mV to 200mV is a good starting point. Aluminum electrolytic capacitors are a good choice for high voltage, bulk capacitance due to their high capacitance per unit area.

The capacitor's RMS current is:

$$I_{CIN(RMS)} = I_{OUT} \sqrt{\frac{V_{OUT}(V_{IN} - V_{OUT})}{(V_{IN})^2}}$$

If applicable, calculate it at the worst case condition, $V_{IN} = 2V_{OUT}$. The RMS current rating of the capacitor is specified by the manufacturer and should exceed the calculated $I_{CIN(RMS)}$. Due to their low ESR (Equivalent Series Resistance), ceramic capacitors are a good choice for high voltage, high RMS current handling. Note that the ripple current ratings from aluminum electrolytic capacitor manufacturers are based on 2000 hours of life. This makes it advisable to further derate the capacitor or to choose a capacitor rated at a higher temperature than required.

The combination of aluminum electrolytic capacitors and ceramic capacitors is an economical approach to meeting the input capacitor requirements. The capacitor voltage rating must be rated greater than $V_{IN(MAX)}$. Multiple capacitors may also be paralleled to meet size or height requirements in the design. Locate the capacitor very close to the MOSFET switch and use short, wide PCB traces to minimize parasitic inductance.

Output Capacitor Selection

The output capacitance, C_{OUT}, selection is based on the design's output voltage ripple, ΔV_{OUT} and transient load requirements. ΔV_{OUT} is a function of ΔI_L and the C_{OUT} ESR. It is calculated by:

$$\Delta V_{OUT} = \Delta I_L \bullet \left(ESR + \frac{1}{(8 \bullet f_{SW} \bullet C_{OUT})} \right)$$

APPLICATIONS INFORMATION

The maximum ESR required to meet a ΔV_{OUT} design requirement can be calculated by:

$$ESR(MAX) = \frac{(\Delta V_{OUT})(L)(f_{SW})}{V_{OUT} \bullet \left(1 - \frac{V_{OUT}}{V_{IN(MAX)}}\right)}$$

Worst-case ΔV_{OUT} occurs at highest input voltage. Use paralleled multiple capacitors to meet the ESR requirements. Increasing the inductance is an option to lower the ESR requirements. For extremely low ΔV_{OUT}, an additional LC filter stage can be added to the output of the supply. Application Note 44 has some good tips on sizing an additional output filter.

Output Voltage Programming

A resistive divider sets the DC output voltage according to the following formula:

$$R2 = R1\left(\frac{V_{OUT}}{1.231V} - 1\right)$$

The external resistor divider is connected to the output of the converter as shown in Figure 3. Tolerance of the feedback resistors will add additional error to the output voltage.

Example: V_{OUT} = 12V; R1 = 10kΩ

$$R2 = 10k\Omega\left(\frac{12V}{1.231V} - 1\right) = 87.48k\Omega - \text{use } 86.6k\Omega\ 1\%$$

The V_{FB} pin input bias current is typically 25nA, so use of extremely high value feedback resistors could cause a converter output that is slightly higher than expected. Bias current error at the output can be estimated as:

$$\Delta V_{OUT(BIAS)} = 25nA \bullet R2$$

Supply UVLO and Shutdown

The SHDN pin has a precision voltage threshold with hysteresis which can be used as an undervoltage lockout threshold (UVLO) for the power supply. Undervoltage lockout keeps the LT3845 in shutdown until the supply input voltage is above a certain voltage programmed by the user. The hysteresis voltage prevents noise from falsely tripping UVLO.

Resistors are chosen by first selecting R_B. Then

$$R_A = R_B \bullet \left(\frac{V_{SUPPLY(ON)}}{1.35V} - 1\right)$$

$V_{SUPPLY(ON)}$ is the input voltage at which the undervoltage lockout is disabled and the supply turns on.

Example: Select R_B = 49.9kΩ, $V_{SUPPLY(ON)}$ = 14.5V (based on a 15V minimum input voltage)

$$R_A = 49.9k\Omega \bullet \left(\frac{14.5V}{1.35V} - 1\right)$$
$$= 486.1k\Omega \text{ (499k}\Omega \text{ resistor is selected)}$$

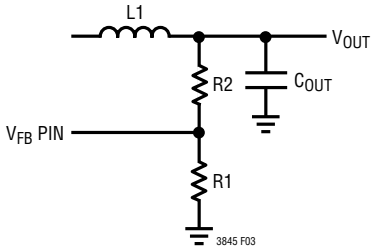


Figure 3. Output Voltage Feedback Divider

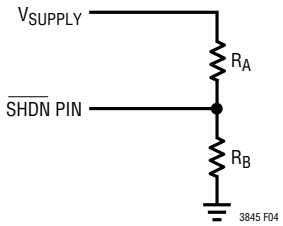


Figure 4. Undervoltage Feedback Divider

APPLICATIONS INFORMATION

If low supply current in standby mode is required, select a higher value of R_B.

The supply turn off voltage is 9% below turn on. In the example the $V_{SUPPLY(OFF)}$ would be 13.2V.

If additional hysteresis is desired for the enable function, an external positive feedback resistor can be used from the LT3845 regulator output.

The shutdown function can be disabled by connecting the $\overline{SHDN}$ pin to the V_{IN} through a large value pull-up resistor. This pin contains a low impedance clamp at 6V, so the $\overline{SHDN}$ pin will sink current from the pull-up resistor(R_{PU}):

$$I_{\overline{SHDN}} = \frac{V_{IN} - 6V}{R_{PU}}$$

Because this arrangement will clamp the $\overline{SHDN}$ pin to the 6V, it will violate the 5V absolute maximum voltage rating of the pin. This is permitted, however, as long as the absolute maximum input current rating of 1mA is not exceeded. Input $\overline{SHDN}$ pin currents of <100µA are recommended: a 1MΩ or greater pull-up resistor is typically used for this configuration.

Soft-Start

The desired soft-start time (t_{SS}) is programmed via the C_{SS} capacitor as follows:

$$C_{SS} = \frac{2\mu A \bullet t_{SS}}{1.231V}$$

The amount of time in which the power supply can withstand a V_{IN}, V_{CC} or $V_{\overline{SHDN}}$ UVLO fault condition (t_{FAULT}) before the C_{SS} pin voltage enters its active region is approximated by the following formula:

$$t_{FAULT} = \frac{C_{SS} \bullet 0.65V}{50\mu A}$$

Oscillator SYNC

The oscillator can be synchronized to an external clock. Set the R_{SET} resistor at least 10% below the desired sync frequency.

It is recommended that the SYNC pin be driven with a square wave that has amplitude greater than 2V, pulse width greater than 1µs and rise time less than 500ns. The rising edge of the sync wave form triggers the discharge of the internal oscillator capacitor.

Minimum On-Time Considerations (Buck Mode)

Minimum on-time $t_{ON(MIN)}$ is the smallest amount of time that the LT3845 is capable of turning the top MOSFET on and off again. It is determined by internal timing delays and the amount of gate charge required turning on the top MOSFET. Low duty cycle applications may approach this minimum on-time limit and care should be taken to ensure that:

$$t_{ON} = \frac{V_{OUT}}{V_{IN} \bullet f_{SW}} > t_{ON(MIN)}$$

where $t_{ON(MIN)}$ is 400ns worst case.

If the duty cycle falls below what can be accommodated by the minimum on-time, the LT3845 will begin to skip cycles. The output will be regulated, but the ripple current and ripple voltage will increase. If lower frequency operation is acceptable, the on-time can be increased above $t_{ON(MIN)}$ for the same step-down ratio.

Layout Considerations

The LT3845 is typically used in DC/DC converter designs that involve substantial switching transients. The switch drivers on the IC are designed to drive large capacitances and, as such, generate significant transient currents themselves. Careful consideration must be made regarding supply bypass capacitor locations to avoid corrupting the ground reference used by IC.

Typically, high current paths and transients from the input supply and any local drive supplies must be kept isolated from SGND, to which sensitive circuits such as the error amp reference and the current sense circuits are referred.

Effective grounding can be achieved by considering switch current in the ground plane, and the return current paths of each respective bypass capacitor. The V_{IN} bypass return, V_{CC} bypass return, and the source of the synchronous

APPLICATIONS INFORMATION

FET carry PGND currents. SGND originates at the negative terminal of the V_{OUT} bypass capacitor, and is the small signal reference for the LT3845.

Don't be tempted to run small traces to separate ground paths. A good ground plane is important as always, but PGND referred bypass elements must be oriented such that transient currents in these return paths do not corrupt the SGND reference.

During the dead-time between switch conduction, the body diode of the synchronous FET conducts inductor current. Commutating this diode requires a significant charge contribution from the main switch. At the instant the body diode commutates, a current discontinuity is created and parasitic inductance causes the switch node to fly up in response to this discontinuity. High currents and excessive parasitic inductance can generate extremely fast dV/dt rise times. This phenomenon can cause avalanche breakdown in the synchronous FET body diode, significant inductive overshoot on the switch node, and shoot-through currents via parasitic turn-on of the synchronous FET. Layout practices and component orientations that minimize parasitic inductance on this node is critical for reducing these effects.

Ringing waveforms in a converter circuit can lead to device failure, excessive EMI, or instability. In many cases, you can damp a ringing waveform with a series RC network across the offending device. In LT3845 applications, any ringing will typically occur on the switch node, which can usually be reduced by placing a snubber across the synchronous FET. Use of a snubber network, however, should be considered a last resort. Effective layout practices typically reduce ringing and overshoot, and will eliminate the need for such solutions.

Effective grounding techniques are critical for successful DC/DC converter layouts. Orient power path components such that current paths in the ground plane do not cross through signal ground areas. Signal ground refers to the Exposed Pad on the backside of the LT3845 IC. SGND is referenced to the (–) terminal of the V_{OUT} decoupling capacitor and is used as the converter voltage feedback reference. Power ground currents are controlled on the LT3845 via the PGND pin, and this ground references the high current synchronous switch drive components, as well as the local V_{CC} supply. It is important to keep PGND and SGND voltages consistent with each other, so separating these grounds with thin traces is not recommended. When the synchronous FET is turned on, gate drive surge currents return to the LT3845 PGND pin from the FET source. The BOOST supply refresh surge currents also return through this same path. The synchronous FET must be oriented such that these PGND return currents do not corrupt the SGND reference. Problems caused by the PGND return path are generally recognized during heavy load conditions, and are typically evidenced as multiple switch pulses occurring during a single switch cycle. This behavior indicates that SGND is being corrupted and grounding should be improved. SGND corruption can often be eliminated, however, by adding a small capacitor (100pF to 200pF) across the synchronous switch FET from drain to source.

The high di/dt loop formed by the switch MOSFETs and the input capacitor (C_{IN}) should have short wide traces to minimize high frequency noise and voltage stress from inductive ringing. Surface mount components are preferred to reduce parasitic inductances from component leads. Connect the drain of the main switch MOSFET directly to the (+) plate of C_{IN}, and connect the source of the synchronous switch MOSFET directly to the (–) terminal of C_{IN}. This capacitor provides the AC current to the switch MOSFETs. Switch path currents can be controlled by orienting switch FETs, the switched inductor, and input and output decoupling capacitors in close proximity to each other.

Locate the V_{CC} and BOOST decoupling capacitors in close proximity to the IC. These capacitors carry the MOSFET drivers' high peak currents. Locate the small-signal components away from high frequency switching nodes (BOOST, SW, TG, V_{CC} and BG). Small-signal nodes are oriented on the left side of the LT3845, while high current switching nodes are oriented on the right side of the IC to simplify layout. This also helps prevent corruption of the SGND reference.

Connect the V_{FB} pin directly to the feedback resistors independent of any other nodes, such as the $SENSE^-$ pin. The feedback resistors should be connected between the (+) and (–) terminals of the output capacitor (C_{OUT}).

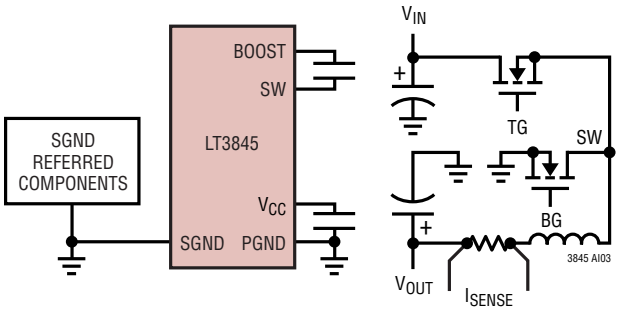
APPLICATIONS INFORMATION

Locate the feedback resistors in close proximity to the LT3845 to minimize the length of the high impedance V_{FB} node.

The SENSE$^-$ and SENSE$^+$ traces should be routed together and kept as short as possible.

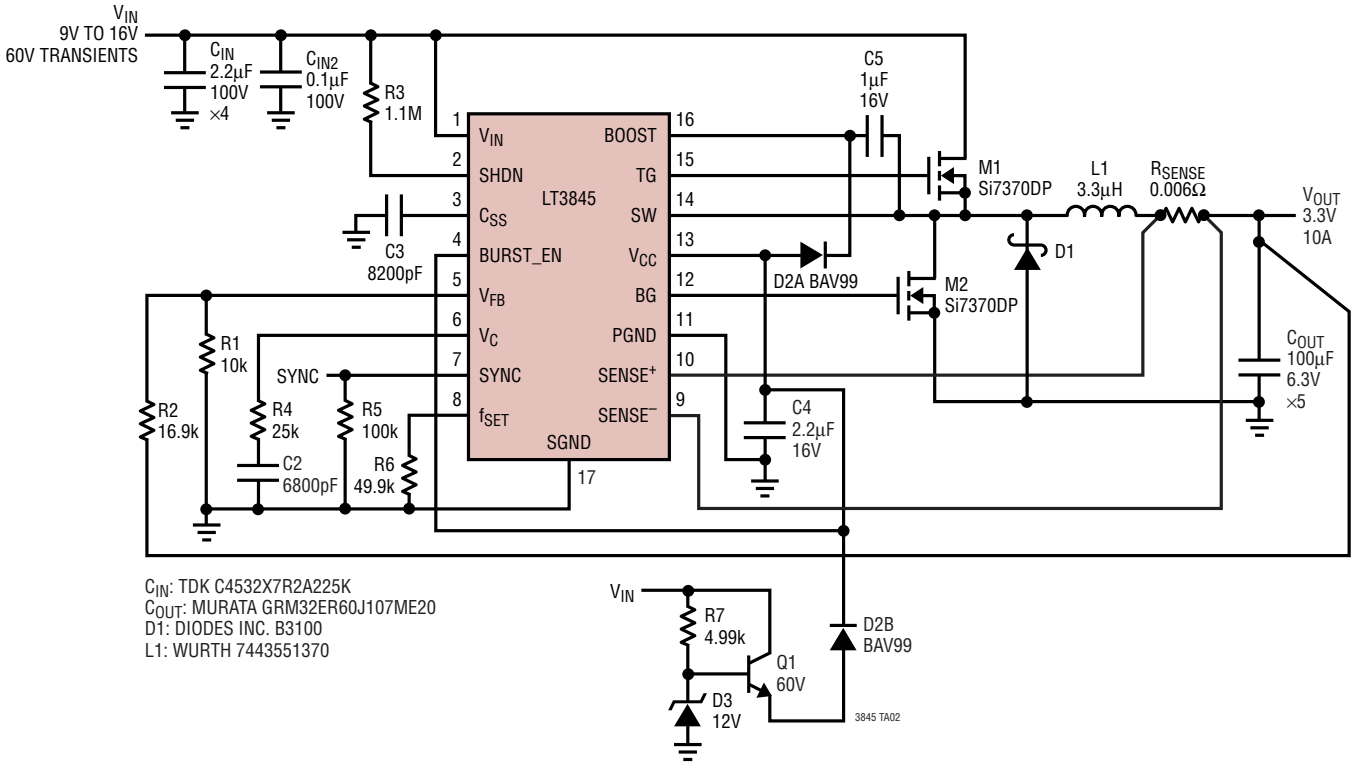
The LT3845 packaging has been designed to efficiently remove heat from the IC via the Exposed Pad on the backside of the package. The Exposed Pad is soldered to a copper footprint on the PCB. This footprint should be made as large as possible to reduce the thermal resistance of the IC case to ambient air.

Orientation of Components Isolates Power Path and PGND Currents, Preventing Corruption of SGND Reference

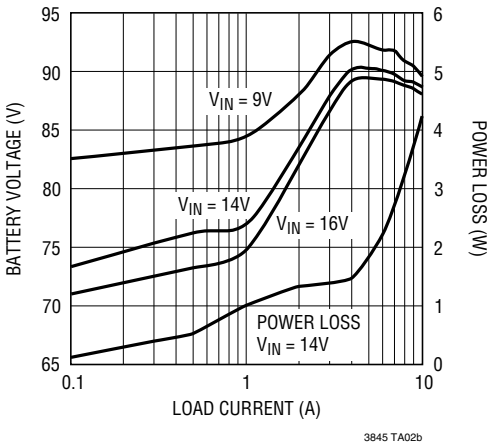


TYPICAL APPLICATIONS

9V-16V to 3.3V at 10A DC/DC Converter Capable of Withstanding 60V Transients, All Ceramic Capacitors and Soft-Start Enabled

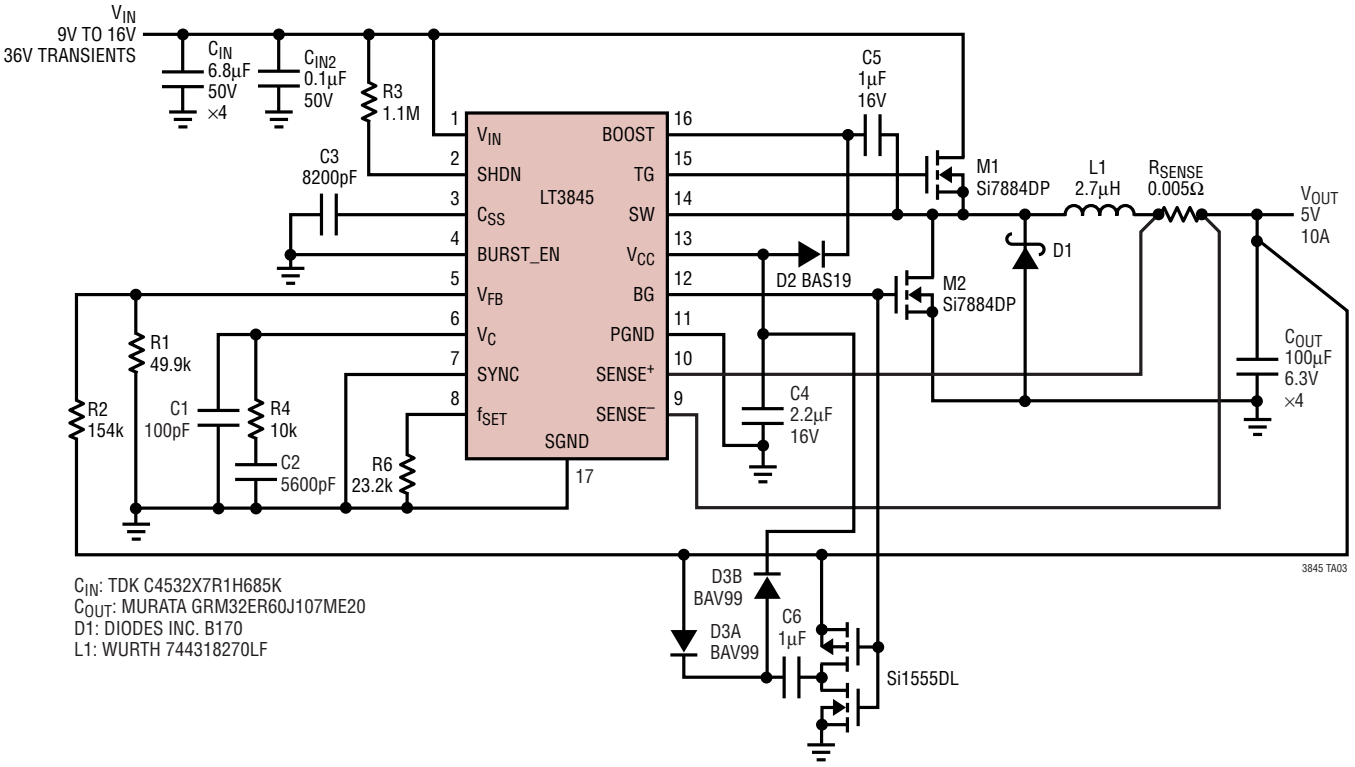


Efficiency and Power Loss



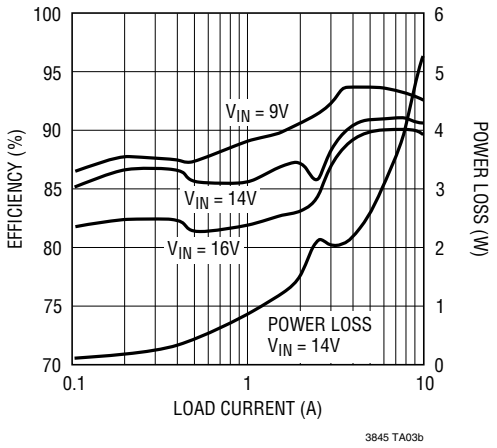
TYPICAL APPLICATIONS

9V-16V to 5V at 10A DC/DC Converter, 500kHz Frequency Operation, Capable of Withstanding 36V Transients, All Ceramic Capacitors, Soft-Start and Burst Mode Enabled



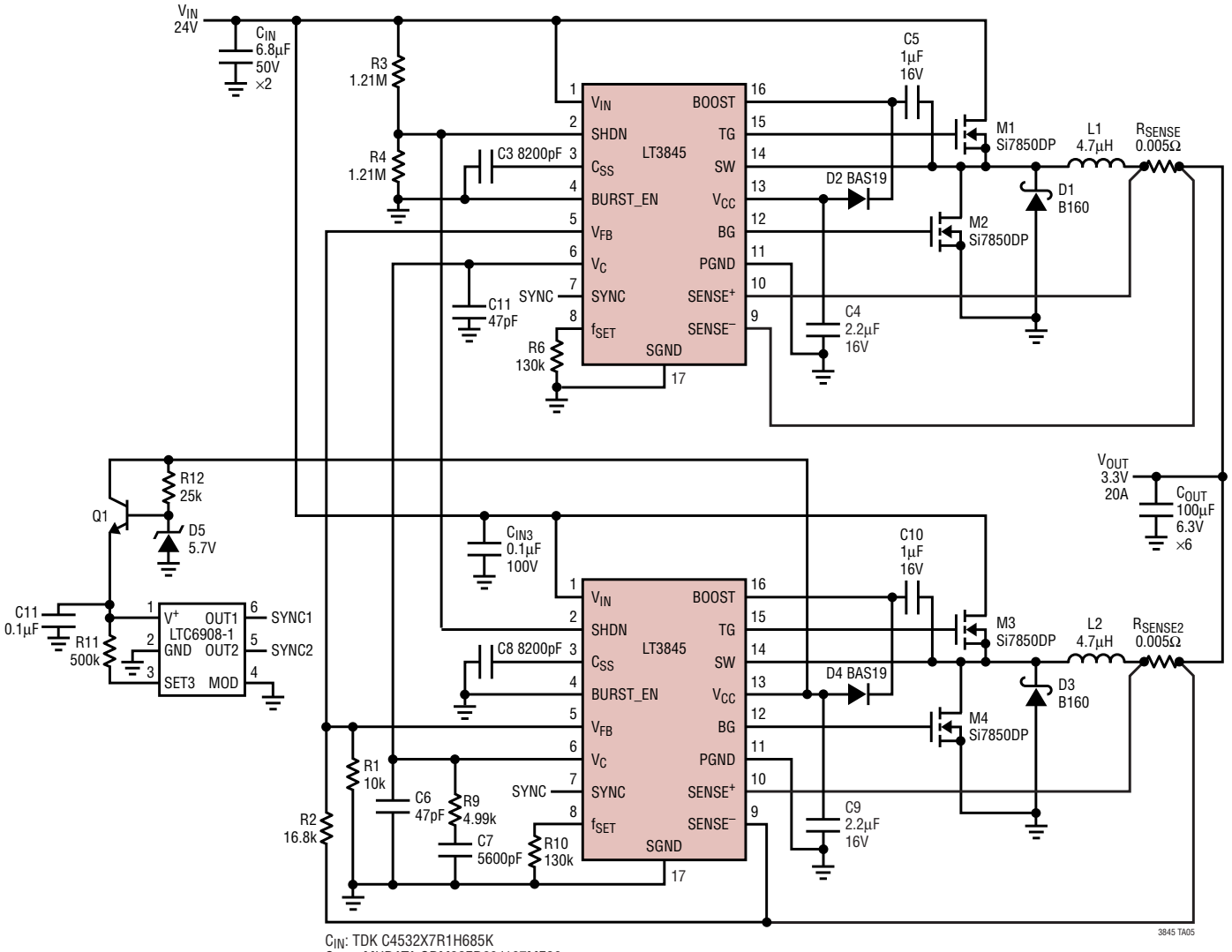
CIN: TDK C4532X7R1H685K
COUT: MURATA GRM32ER60J107ME20
D1: DIODES INC. B170
L1: WURTH 744318270LF

Efficiency and Power Loss



TYPICAL APPLICATIONS

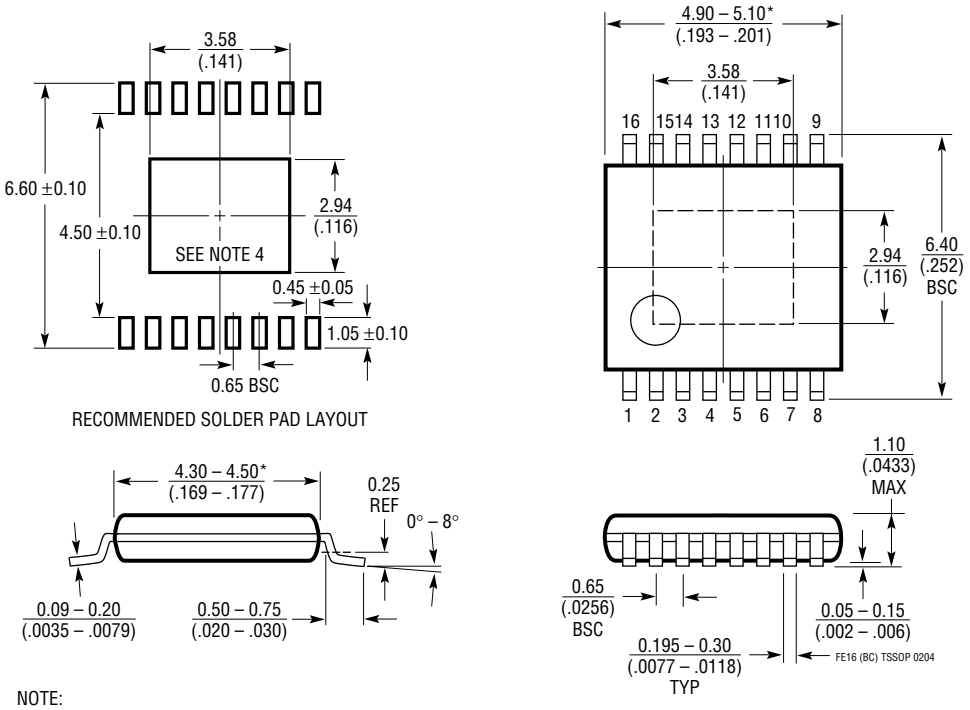
9V-24V to 3.3V, 2-Phase at 10A per Phase, DC/DC Converter with Spread Spectrum Operation



CIN: TDK C4532X7R1H685K
COUT: MURATA GRM32ER60J107ME20
D1, D3: DIODES, INC. B160
L1, L2: VISHAY IHLP-5050FD-01

PACKAGE DESCRIPTION

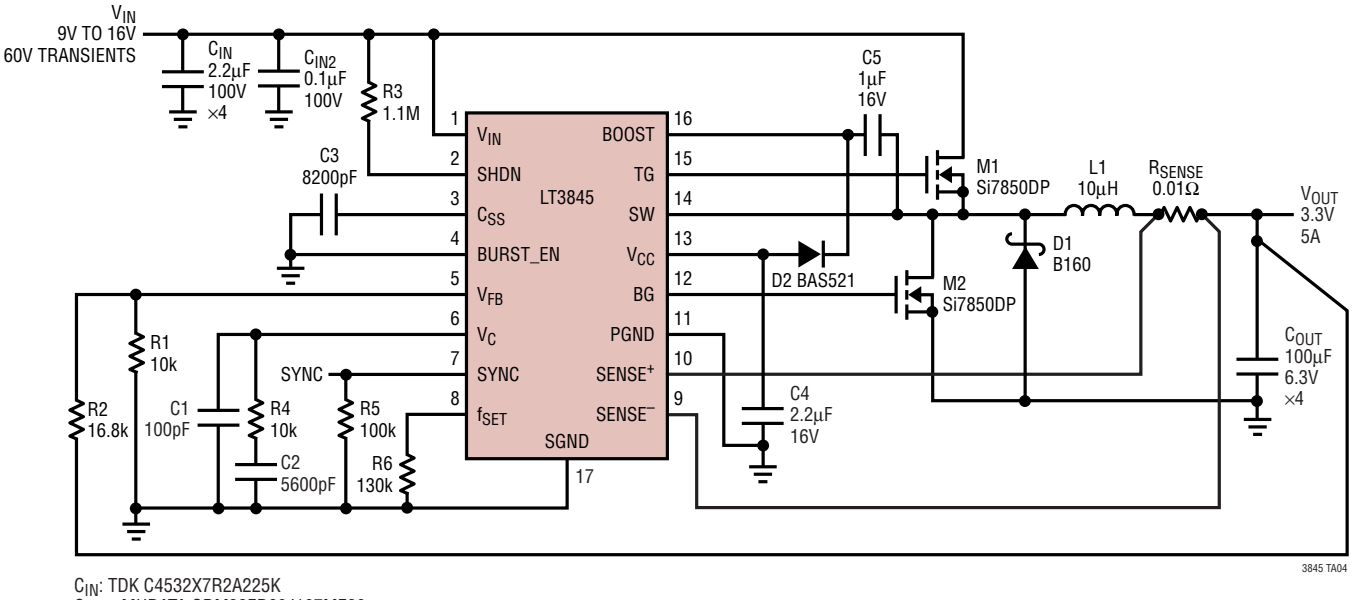
FE Package
16-Lead Plastic TSSOP (4.4mm)
(Reference LTC DWG # 05-08-1663)
Exposed Pad Variation BC



NOTE:
1. CONTROLLING DIMENSION: MILLIMETERS
2. DIMENSIONS ARE IN $\frac{\text{MILLIMETERS}}{(\text{INCHES})}$
3. DRAWING NOT TO SCALE
4. RECOMMENDED MINIMUM PCB METAL SIZE FOR EXPOSED PAD ATTACHMENT
*DIMENSIONS DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.150mm (.006") PER SIDE

TYPICAL APPLICATION

9V-16V to 3.3V at 5A DC/DC Converter, Frequency Synchronization Range 150kHz to 300kHz, Capable of Withstanding 60V Transients, All Ceramic Capacitors, Soft-Start and Burst Mode Enabled



C_{IN}: TDK C4532X7R2A225K
C_{OUT}: MURATA GRM32ER60J107ME20
L1: VISHAY IHLP-5050FD-01
M1, M2: VISHAY Si7850DP

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1339	High Power Synchronous DC/DC Controller	V_{IN} up to 60V, Drivers 10000pF Gate Capacitance, I_{OUT} = <20A
LTC®1624	Switching Controller	Buck, Boost, SEPIC, 3.5V ≤ V_{IN} ≤ 36V; 8-Lead SO Package
LTC1702A	Dual 2-Phase Synchronous DC/DC Controller	550kHz Operation, No R_{SENSE}, 3V = <V_{IN} = <7V, I_{OUT} = <20A
LTC1735	Synchronous Step-Down DC/DC Controller	3.5V = <V_{IN} = <36V, 0.8V = <V_{OUT} = <6V, Current Mode, I_{OUT} = <20A
LTC1778	No R_{SENSE}™ Synchronous DC/DC Controller	4V = <V_{IN} = <36V, Fast Transient Response, Current Mode, I_{OUT} = <20A
LT3010	50mA, 3V to 80V Linear Regulator	1.275V = <V_{OUT} = <60V, No Protection Diode Required, 8-Lead MSOP Package
LT3430/LT3431	Monolithic 3A, 200kHz/500kHz Step-Down Regulator	5.5V = <V_{IN} = <60V, 0.1Ω Saturation Switch, 16-Lead SSOP Package
LTC3703/LTC3703-5	100V Synchronous Switching Regulator Controllers	No R_{SENSE}, Voltage Mode Control, GN16 Package
LT3724	High Voltage Current Mode Switching Regulator Controllers	V_{IN} up to 60V, I_{OUT} ≤ 5A, 16-Lead TSSOP FE Package, Onboard Bias Regulator, Burst Mode Operation, 200kHz Operation
LT3800	High Voltage Synchronous Regulator Controller	V_{IN} up to 60V, I_{OUT} ≤ 20A, Current Mode, Onboard Bias Regulator, Burst Mode Operation, 16-Lead TSSOP FE Package
LT3844	High Voltage Current Mode Controller with Programmable Operating Frequency	V_{IN} up to 60V, I_{OUT} ≤ 5A, Onboard Bias Regulator, Burst Mode Operation, Sync Capability, 16-Lead TSSOP FE Package

No R_{SENSE} is a trademark of Linear Technology Corporation.

Linear Technology Corporation
1630 McCarthy Blvd., Milpitas, CA 95035-7417
(408) 432-1900 • FAX: (408) 434-0507 • www.linear.com

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