

DRAM MODULE

16 Mega Byte

KMM5364000AH Fast Page Mode

4Mx36 DRAM SIMM , 4K Refresh , 5V

Using 16M DRAM with 400 mil Package

GENERAL DESCRIPTION

The Samsung KMM5364000AH is a 4M bit x 36 Dynamic RAM high density memory module. The Samsung KMM5364000AH consists of nine CMOS 4Mx4bit DRAMs in 24-pin SOJ packages mounted on a 72-pin glass-epoxy substrate. A 0.22uF decoupling capacitor is mounted on the printed circuit board for each DRAM. The KMM5364000AH is a Single In-line Memory Module with edge connections and is intended for mounting into 72 pin edge connector sockets.

FEATURES

- Performance Range:

	tRAC	tCAC	tRC
KMM5364000AH - 5	50ns	13ns	90ns
KMM5364000AH - 6	60ns	15ns	110ns
KMM5364000AH - 7	70ns	20ns	130ns
KMM5364000AH - 8	80ns	20ns	150ns
- Fast Page Mode Operation
- ~~CAS~~-before-~~RAS~~ refresh capability
- ~~RAS~~-only and Hidden refresh capability
- TTL compatible inputs and outputs
- Single +5V±10% power supply
- 4096 cycles/64 ms refresh
- JEDEC standard PDPin & pinout
- PCB : Height(1250mil), single sided component

PIN CONFIGURATIONS

Pin	Symbol	Pin	Symbol
1	Vss	37	DQ19
2	DQ0	38	DQ20
3	DQ1	39	Vss
4	DQ2	40	CAS 0
5	DQ3	41	A10
6	DQ4	42	A11
7	DQ5	43	NC
8	DQ6	44	RAS 0
9	DQ7	45	NC
10	Vcc	46	DQ21
11	PD5	47	W
12	A0	48	Vss
13	A1	49	DQ22
14	A2	50	DQ23
15	A3	51	DQ24
16	A4	52	DQ25
17	A5	53	DQ26
18	A6	54	DQ27
19	OE	55	DQ28
20	DQ8	56	DQ29
21	DQ9	57	DQ30
22	DQ10	58	DQ31
23	DQ11	59	Vcc
24	DQ12	60	DQ32
25	DQ13	61	DQ33
26	DQ14	62	DQ34
27	DQ15	63	DQ35
28	A7	64	NC
29	DQ16	65	NC
30	Vcc	66	NC
31	A8	67	PD1
32	A9	68	PD2
33	NC	69	PD3
34	NC	70	PD4
35	DQ17	71	NC
36	DQ18	72	Vss

PIN NAMES

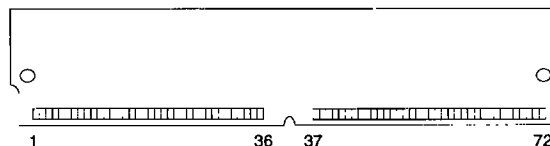
A0 - A11	Address Inputs
DQ0 - DQ35	Data In/Out
W	Read/Write Input
RAS 0	Row Address Strobe
CAS 0	Column Address Strobe
PD1 - PD5	Presence Detect
Vcc	Power(+5V)
Vss	Ground
NC	No Connection
OE	Output enable

PRESENCE DETECT PINS (Optional)

Pin	50NS	60NS	70NS	80NS
PD1	Vss	Vss	Vss	Vss
PD2	NC	NC	NC	NC
PD3	Vss	NC	Vss	NC
PD4	Vss	NC	NC	Vss
PD5	Vss	Vss	Vss	Vss

*Pin Connection Changing Available

PIN CONNECTIONS (Front View)



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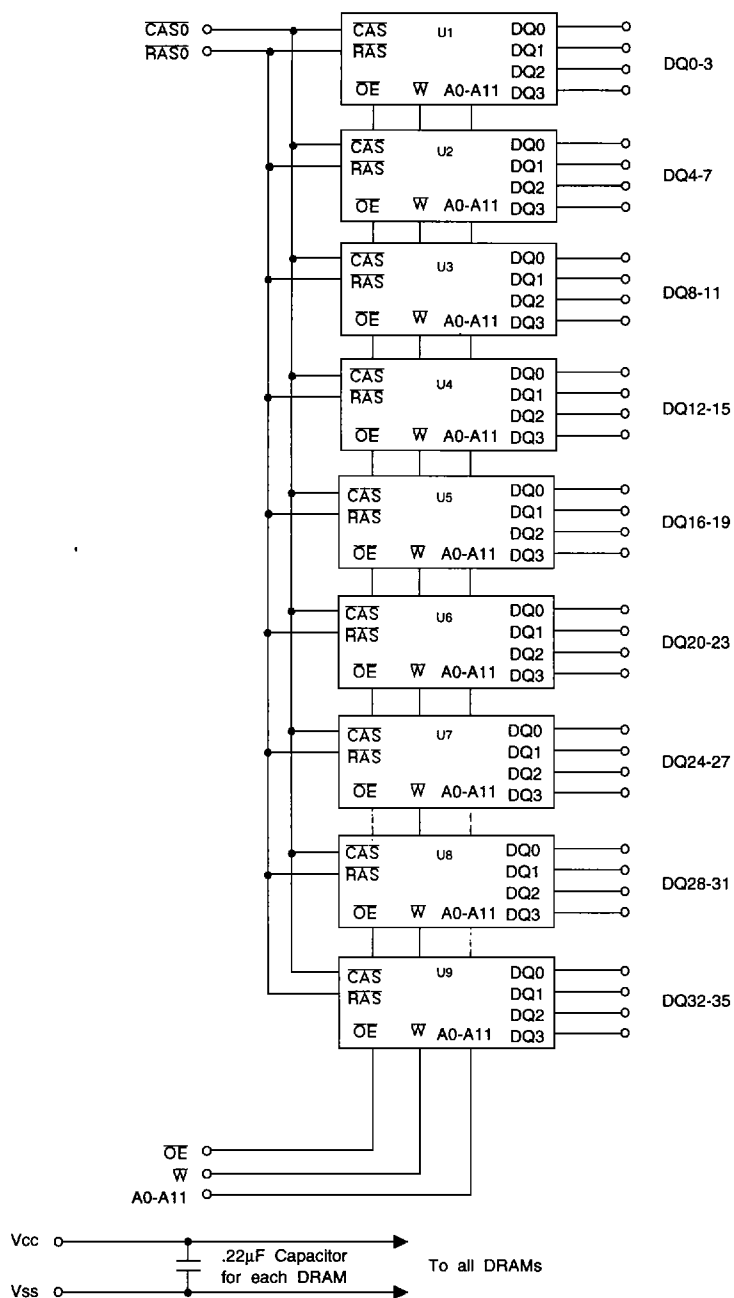
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FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS *

Item	Symbol	Rating	Unit
Voltage on any pin relative to Vss	VIN,VOUT	-1 to +7.0	V
Voltage on Vcc supply relative to Vss	Vcc	-1 to +7.0	V
Storage Temperature	Tstg	-55 to +150	°C
Power Dissipation	Pd	9	W
Short Circuit Output Current	Ios	50	mA

* Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for intended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to Vss, Ta = 0 to 70 °C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	Vcc	4.5	5.0	5.5	V
Ground	Vss	0	0	0	V
Input High Voltage	VIH	2.4	-	Vcc+1	V
Input Low Voltage	VIL	-1.0	-	0.8	V

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted.)

Parameter	Part No	Symbol	Min	Max	Unit
Operating Current * (RAS, CAS, Address cycling @tRC=min.)	KMM5364000AH - 5	ICC1	-	810	mA
	KMM5364000AH - 6		-	720	mA
	KMM5364000AH - 7		-	630	mA
	KMM5364000AH - 8		-	540	mA
Standby Current (RAS=CAS=W=VIH)		ICC2	-	18	mA
RAS Only Refresh Current * (CAS= VIH, RAS cycling @tRC =min.)	KMM5364000AH - 5	ICC3	-	810	mA
	KMM5364000AH - 6		-	720	mA
	KMM5364000AH - 7		-	630	mA
	KMM5364000AH - 8		-	540	mA
Fast Page Mode Current * (RAS=VIL, CAS cycling : tPC=min.)	KMM5364000AH - 5	ICC4	-	720	mA
	KMM5364000AH - 6		-	630	mA
	KMM5364000AH - 7		-	540	mA
	KMM5364000AH - 8		-	450	mA
Standby Current (RAS=CAS=W=Vcc-0.2V)		ICC5	-	9	mA
CAS-Before-RAS Refresh Current * (RAS and CAS cycling @tRC =min.)	KMM5364000AH - 5	ICC6	-	810	mA
	KMM5364000AH - 6		-	720	mA
	KMM5364000AH - 7		-	630	mA
	KMM5364000AH - 8		-	540	mA
Input Leakage Current (Any input 0 ≤ VIN ≤ Vcc+0.5V, all other pins not under test = 0 V.)		II(L)	-90	90	μA
Output Leakage Current (Data out is disabled, 0V ≤ Vout ≤ Vcc)		IO(L)	-10	10	μA
Output High Voltage Level (IOH = - 5mA)		VOH	2.4	-	V
Output Low Voltage Level (IOL = 4.2mA)		VOL	-	0.4	V

* NOTE : ICC1,ICC3,ICC4 and ICC6 are dependent on output loading and cycle rates. Specified values are obtained with the output open. ICC is specified as an average current. In ICC1 and ICC3, address can be changed maximum two times while RAS=VIL. In ICC4, address can be changed maximum once within one page mode cycle .

CAPACITANCE (Ta = 25°C , Vcc=5V , f = 1 MHz)

Item	Symbol	Min	Max	Unit
Input capacitance [A0-A11]	CIN1	-	70	pF
Input capacitance [W, OE]	CIN2	-	80	pF
Input capacitance [RAS0]	CIN3	-	80	pF
Input capacitance [CAS0]	CIN4	-	80	pF
Input/Output capacitance [DQ0-35]	CDQ1	-	17	pF

AC CHARACTERISTICS (0°C≤Ta≤70°C, Vcc=5.0V±10%. See notes 1,2.)

STANDARD OPERATION	Symbol	- 5		- 6		- 7		- 8		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Random read or write cycle time	tRC	90		110		130		150		ns	
Access time from RAS	tRAC	50		60		70		80		ns	3,4
Access time from CAS	tCAC	13		15		20		20		ns	3,4,5
Access time from column address	tAA	25		30		35		40		ns	3,11
CAS to output in Low-Z	tCLZ	0		0		0		0		ns	3
Output buffer turn-off delay	tOFF	0	13	0	15	0	20	0	20	ns	7
Transition time (rise and fall)	tT	3	50	3	50	3	50	3	50	ns	2
RAS precharge time	tRP	30		40		50		60		ns	
RAS pulse width	tRAS	50	10K	60	10K	70	10K	80	10K	ns	
RAS hold time	tRSH	13		15		20		20		ns	
CAS hold time	tCSH	50		60		70		80		ns	
CAS pulse width	tCAS	13	10K	15	10K	20	10K	20	10K	ns	
RAS to CAS delay time	tRCD	20	37	20	45	20	50	20	60	ns	4
RAS to column address delay time	tRAD	15	25	15	30	15	35	15	40	ns	11
CAS to RAS precharge time	tCRP	5		5		5		5		ns	
Row address set-up time	tASR	0		0		0		0		ns	
Row address hold time	tRAH	10		10		10		10		ns	
Column address set-up time	tASC	0		0		0		0		ns	
Column address hold time	tCAH	10		10		15		15		ns	
Column address hold referenced to RAS	tAR	40		45		55		60		ns	6
Column Address to RAS lead time	tRAL	25		30		35		40		ns	
Read command set-up time	tRCS	0		0		0		0		ns	
Read command hold referenced to CAS	tRCH	0		0		0		0		ns	9
Read command hold referenced to RAS	tRRH	0		0		0		0		ns	9
Write command hold time	tWCH	10		10		15		15		ns	
Write command hold referenced to RAS	tWCR	40		45		55		60		ns	6
Write command pulse width	tWP	10		10		15		15		ns	
Write command to RAS lead time	tRWL	15		15		20		20		ns	
Write command to CAS lead time	tCWL	13		15		20		20		ns	
Data-in set-up time	tDS	0		0		0		0		ns	10
Data-in hold time	tDH	10		10		15		15		ns	10
Data-in hold referenced to RAS	tDHR	40		45		55		60		ns	6
Refresh period	tREF		64		64		64		64	ms	
Write command set-up time	tWCS	0		0		0		0		ns	8
CAS setup time (C-B-R refresh)	tCSR	10		10		10		10		ns	
CAS hold time (C-B-R refresh)	tCHR	10		10		15		15		ns	
RAS precharge to CAS hold time	tRPC	5		5		5		5		ns	
Access time from CAS precharge	tCPA		30		35		40		45	ns	3
Fast Page mode cycle time	tPC	35		40		45		50		ns	
CAS precharge time (Fast page)	tCP	10		10		10		10		ns	
RAS pulse width (Fast page)	tRASP	50	200K	60	200K	70	200K	80	200K	ns	
W to RAS precharge time(C-B-R refresh)	tWRP	10		10		10		10		ns	
W to RAS hold time(C-B-R refresh)	tWRH	10		10		10		10		ns	
CAS precharge(C-B-R counter test)	tCPT	20		20		30		30		ns	

STANDARD OPERATION	Symbol	- 5		- 6		- 7		- 8		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
$\overline{OE}$ Access time	tOEA	13		15		20		20		ns	
$\overline{OE}$ to data delay	tOED	15		15		20		20		ns	
Output buffer turn off delay time from $\overline{OE}$	tOEZ	0	15	0	15	0	20	0	20	ns	
$\overline{OE}$ command hold time	tOEH	13		15		20		20		ns	
RAS hold time referenced to $\overline{OE}$	tROH	13		15		20		20		ns	

NOTES

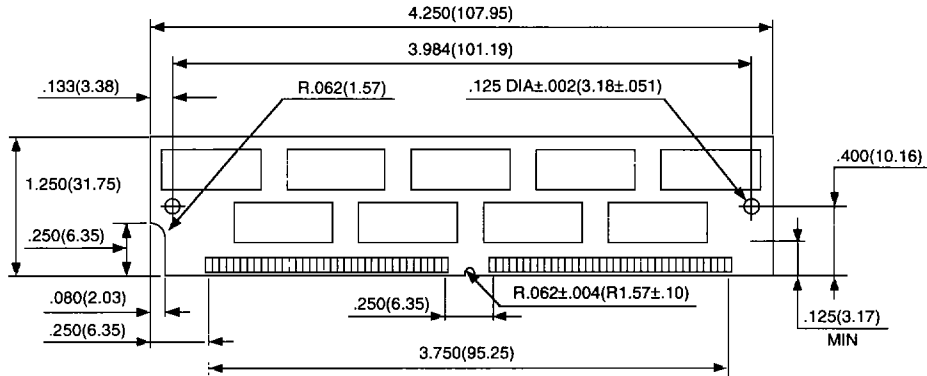
1. An initial pause of 200 μ s is required after power-up followed by any 8 RAS-only or CAS-before-RAS refresh cycles before proper device operation is achieved.
2. VIH (min) and VIL (max) are reference levels for measuring timing of input signals. Transition times are measured between VIH(min) and VIL(max) and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 100pF.
4. Operation within the tRCD(max) limit insures that tRAC(max) can be met. tRCD(max) is specified as a reference point only. If tRCD is greater than the specified tRCD(max) limit, then access time is controlled exclusively by tCAC.
5. Assumes that tRCD $\geq$ tRCD(max).
6. tAR, tWCR, tDHR are referenced to tRAD(MAX)
7. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to VOH or VOL.
8. tWCS is non restrictive operating parameter. It included in the data sheet as electrical characteristic only. If tWCS $\geq$ tWCS(min) the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle.
9. Either tRCH or tRRH must be satisfied for a read cycle.
10. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles.
11. Operation within the tRAD(max) limit insures that tRAC(max) can be met. tRAD(max) is specified as reference point only. If tRAD is greater than the specified tRAD(max) limit, then access time is controlled by tAA.

TIMING DIAGRAM

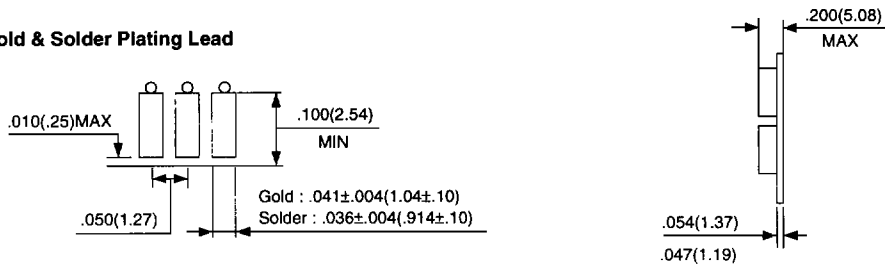
Please refer to attached timing chart (II) !

PACKAGE DIMENSIONS (Front View)

Units : Inches (millimeters)



Gold & Solder Plating Lead



Tolerances : ±.005(.13) unless otherwise specified

NOTE : The used device is 4Mx4 DRAM , SOJ .
DRAM Part No. : KM44C4000AJ (400 mil)

Revision History
Rev0.0 : 22 Dec. '93