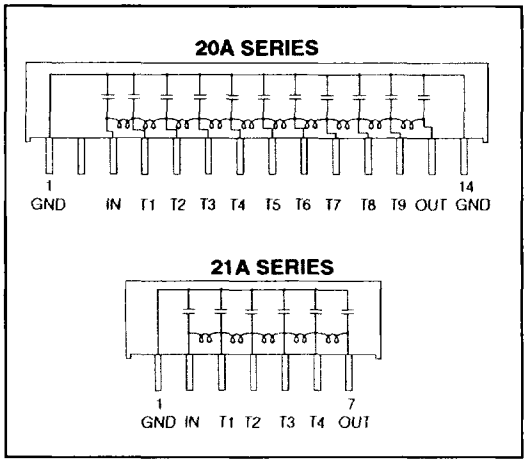
- ❒ **Lumped constant**
- ❒ **TTL and DTL compatible**
- ❒ **Automatic insertion**
- ❒ **Low distortion and low attenuation**
- ❒ **High reliability**

SINGLE - IN - LINE PACKAGES



description

The 20A and 21A series of Delay Lines are constructed from passive, lumped-constant components forming a delay line ladder. Two low profile single-in-line package styles are used to house 10 equally spaced delay taps and 5 equally spaced delay taps. Both types are suitable for high-density board designs. No termination resistor is included which allows for series connection of a number of delay lines for unequal tap designs. Direct drive from TTL and DTL is easily achieved with a minimum of design know-how.

absolute maximum ratings over operating free-air temperature range

Temperature coefficient of delay	±100ppm/C
Operating free-air temperature range	.0C to 70C
Storage temperature range	–55C to 125C
Operating voltage	50V DC
Characteristic impedance Zo	±10% of nominal
Distortion	±10%
Insulation resistance	1000MΩ min at 50V DC
Dielectric strength	50V DC
Min. pulse width as % of total delay	40%
Input pulse repetition rate PRR	3 x pulse width min.
Lead temperature 1.5mm from case for 10 seconds	300C

delay characteristics Ta = 25C, input test pulse voltage 3V,pulse width 3 x total delay, rise time 3ns, delay line termination ±1% of nominal Zo.

delay tolerance from input to tap ±2ns or ±5% whichever is greater

20A SERIES 10 Tap 14 Pin SIP Package style E

PART No. (1)	TOTAL DELAY (ns) ±5% (2)	TAP TO TAP DELAY (ns)	RISE TIME (ns) max.	ATTENUATION (%) max.
20A-30012	30	3 ± 1	5	2.5
20A-40012	40	4 ± 2	7	2.5
20A-50012	50	5 ± 2	9	3
20A-60012	60	6 ± 3	11	3.5
20A-70012	70	7 ± 3	12	3.5
20A-75012	75	7.5 ± 3	13	4
20A-80012	80	8 ± 3	14	4.5
20A-90012	90	9 ± 3	16	4.5
20A-10112	100	10 ± 3	18	4.5
20A-15112	150	15 ± 3	25	8
20A-20112	200	20 ± 3	35	10
20A-25112	250	25 ± 3	42	12

(1) For 100Ω impedance parts
(2) or ±0.5ns whichever is greater

Note: Delays measured between 50% points on leading edges of input and output signals.
Other impedances are available to special order.

21A SERIES 5 Tap 7 Pin SIP Package style F

PART No. (1)	TOTAL DELAY (ns) ±5% (2)	TAP TO TAP DELAY (ns)	RISE TIME (ns) max.	ATTENUATION (%) max.
21A-20012	20	4 ± 1	6	2
21A-25012	25	5 ± 2	7.8	2
21A-30012	30	6 ± 2	9	2
21A-40012	40	8 ± 2	12	2
21A-50012	50	10 ± 2	15	2
21A-60012	60	12 ± 3	18	2.5
21A-70012	70	14 ± 3	22	3
21A-75012	75	15 ± 3	22	3.5
21A-80012	80	16 ± 3	25	4
21A-90012	90	18 ± 3	28	4
21A-10112	100	20 ± 3	28	4

(1) For 100Ω impedance parts
(2) or ±0.5ns whichever is greater

Note: Delays measured between 50% points on leading edges of input and output signals.
Other impedances are available to special order.