## Serial E²PROM

FEATURES

- **2.7V to 5.5V Power Supply**
- **Low Power CMOS**
  - **—Active current less than 1 mA**
  - **—Standby current less than 50 µA**
- **Internally Organized 128 x 8**
- **2 Wire Serial Interface**
  - **—Bidirectional data transfer protocol**
- **Four Byte Page Write Mode**
- **Self Timed Write Cycle**
  - **—Typical write cycle time of 5 ms**
- **High Reliability**
  - **—Endurance: 1 million cycles**
  - **—Data retention: 100 years**
- **8-Pin Mini-DIP, 8-PIN MSOP, and 8-PIN SOIC packages**

DESCRIPTION

The X24C01 is a CMOS 1024 bit serial E²PROM, internally organized as 128 x 8. The X24C01 features a serial interface and software protocol allowing operation on a simple two wire bus.

Xicor E²PROMs are designed and tested for applications requiring extended endurance. Inherent data retention is greater than 100 years.

FUNCTIONAL DIAGRAM
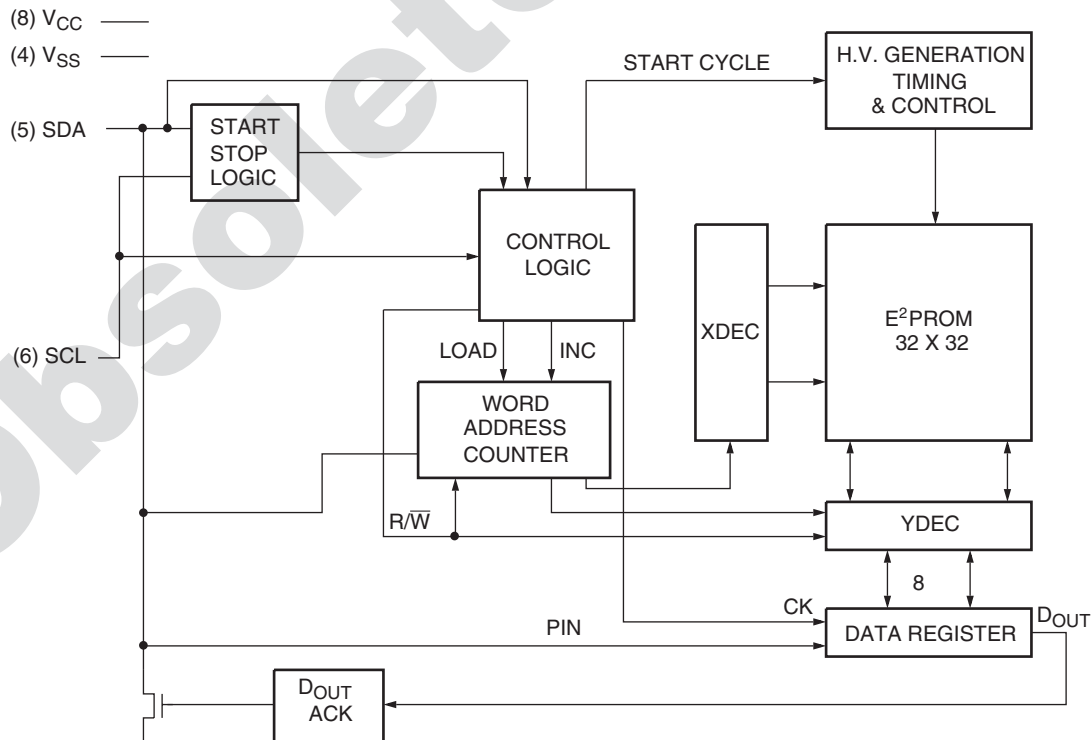
X24C01

PIN DESCRIPTIONS

Serial Clock (SCL)

The SCL input is used to clock all data into and out of the device.

Serial Data (SDA)

SDA is a bidirectional pin used to transfer data into and out of the device. It is an open drain output, and may be wire-ORed with any number of open drain or open collector outputs.

An open drain output requires the use of a pull-up resistor. For selecting typical values, refer to the Guidelines for Calculating Typical Values of Bus Pull-Up Resistors graph.
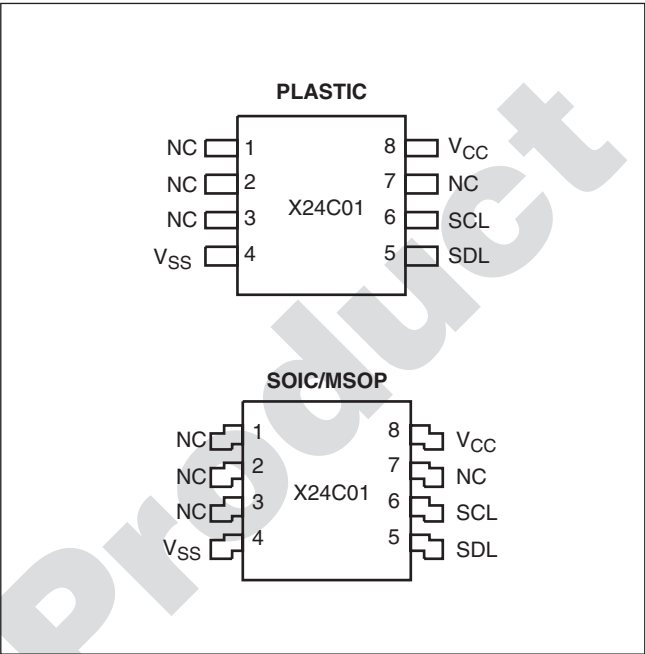
PIN NAMES

Symbol	Description
NC	No Connect
V_{SS}	Ground
V_{CC}	Supply Voltage
SDA	Serial Data
SCL	Serial Clock

A.C. CONDITIONS OF TEST

Input Pulse Levels	V_{CC} x 0.1 to V_{CC} x 0.9
Input Rise and Fall Times	10 ns
Input and Output Timing Levels	V_{CC} x 0.5

PIN CONFIGURATION

EQUIVALENT A.C. LOAD CIRCUIT
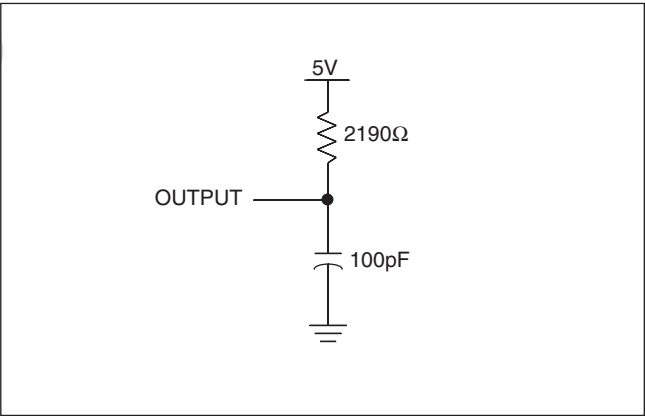
DEVICE OPERATION

The X24C01 supports a bidirectional bus oriented protocol. The protocol defines any device that sends data onto the bus as a transmitter and the receiving device as the receiver. The device controlling the transfer is a master and the device being controlled is the slave. The master will always initiate data transfers and provide the clock for both transmit and receive operations. Therefore, the X24C01 will be considered a slave in all applications.

Clock and Data Conventions

Data states on the SDA line can change only during SCL LOW. SDA state changes during SCL HIGH are reserved for indicating start and stop conditions. Refer to Figures 1 and 2.

Start Condition

All commands are preceded by the start condition, which is a HIGH to LOW transition of SDA when SCL is HIGH. The X24C01 continuously monitors the SDA and SCL lines for the start condition, and will not respond to any command until this condition has been met.

Figure 1. Data Validity
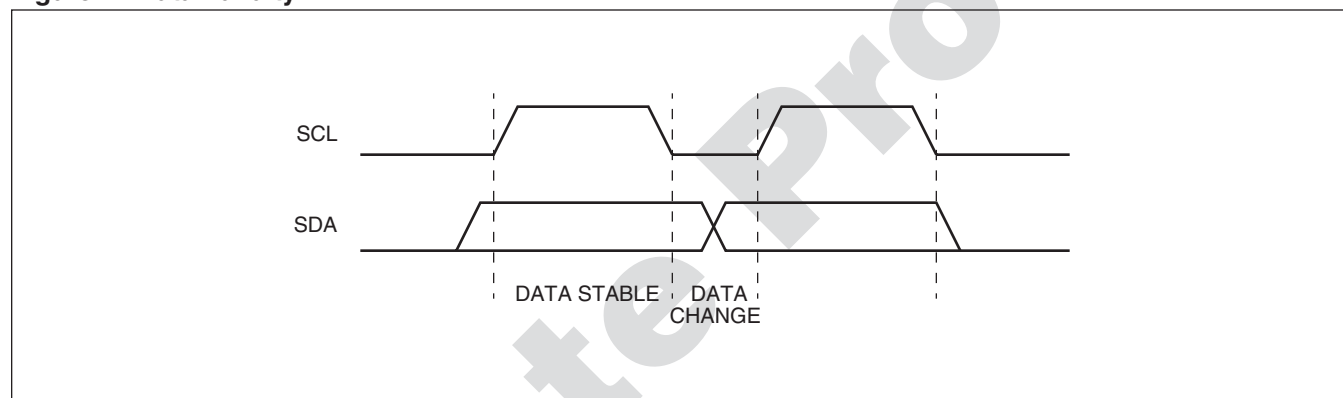
Stop Condition

All communications must be terminated by a stop condition, which is a LOW to HIGH transition of SDA when SCL is HIGH. The stop condition is also used by the X24C01 to place the device in the standby power mode after a read sequence. A stop condition can only be issued after the transmitting device has released the bus.

Acknowledge

Acknowledge is a software convention used to indicate successful data transfers. The transmitting device will release the bus after transmitting eight bits. During the ninth clock cycle the receiver will pull the SDA line LOW to acknowledge that it received the eight bits of data. Refer to Figure 3.

The X24C01 will respond with an acknowledge after recognition of a start condition, a seven bit word address and a R/$\overline{W}$ bit. If a write operation has been selected, the X24C01 will respond with an acknowledge after each byte of data is received.

In the read mode, the X24C01 will transmit eight bits of data, release the SDA line, and monitor the line for an acknowledge. If an acknowledge is detected and no stop condition is generated by the master, the X24C01 will continue to transmit data. If an acknowledge is not detected, the X24C01 will terminate further data transmissions. The master must then issue a stop condition to return the X24C01 to the standby power mode and place the device into a known state.
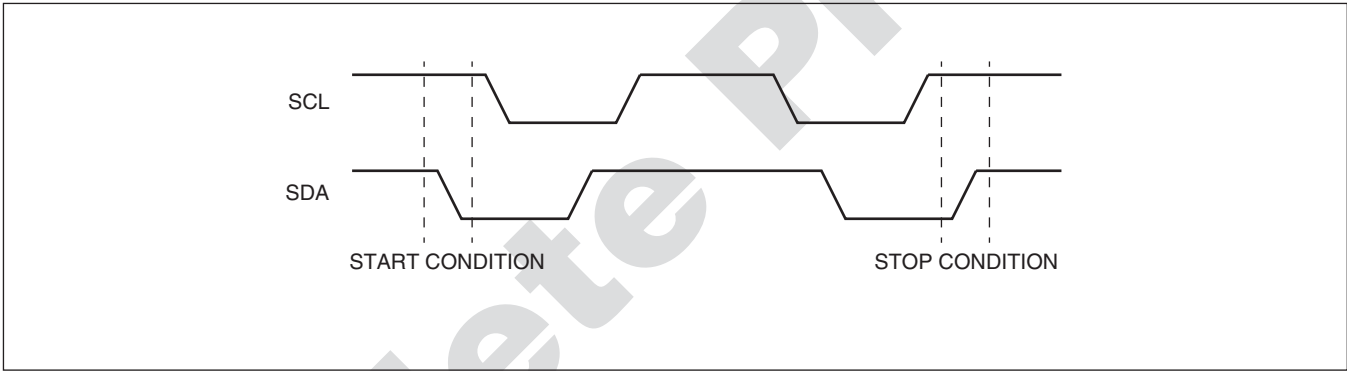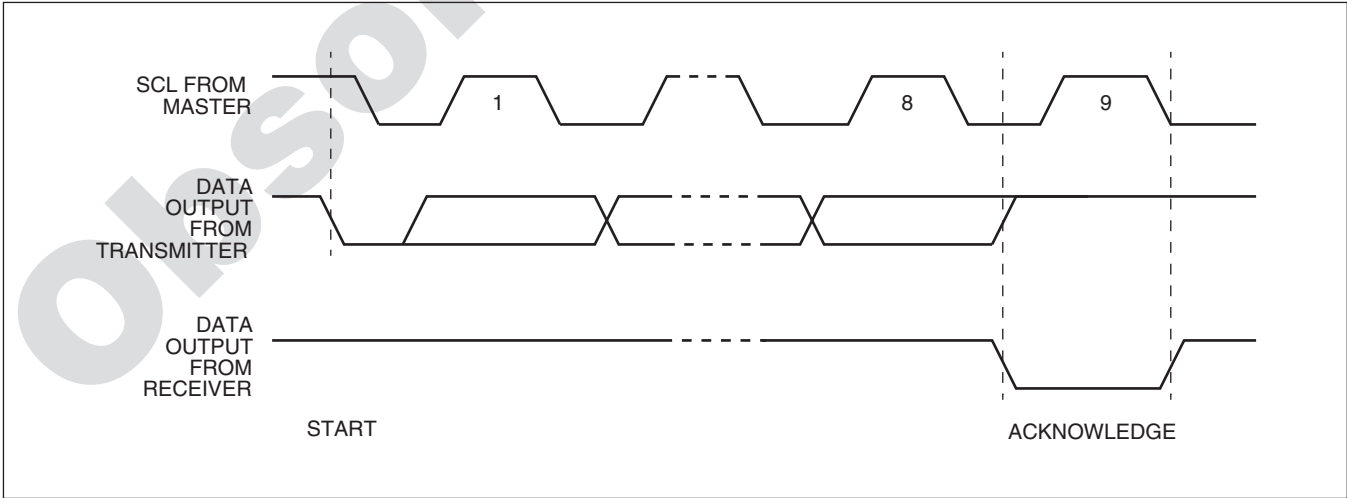
Figure 2. Definition of Start and Stop

Figure 3. Acknowledge Response From Receiver

WRITE OPERATIONS

Byte Write

To initiate a write operation, the master sends a start condition followed by a seven bit word address and a write bit. The X24C01 responds with an acknowledge, then waits for eight bits of data and then responds with an acknowledge. The master then terminates the transfer by generating a stop condition, at which time the X24C01 begins the internal write cycle to the non-volatile memory. While the internal write cycle is in progress, the X24C01 inputs are disabled, and the device will not respond to any requests from the master. Refer to Figure 4 for the address, acknowledge and data transfer sequence.

Page Write

The most significant five bits of the word address define the page address. The X24C01 is capable of a four byte page write operation. It is initiated in the same manner as the byte write operation, but instead of terminating the transfer of data after the first data byte, the master can transmit up to three more bytes. After the receipt of each data byte, the X24C01 will respond with an acknowledge.

After the receipt of each data byte, the two low order address bits are internally incremented by one. The high order five bits of the address remain constant. If the master should transmit more than four data bytes prior to generating the stop condition, the address counter will "roll over" and the previously transmitted data will be overwritten. As with the byte write operation, all inputs are disabled until completion of the internal write cycle. Refer to Figure 5 for the address, acknowledge and data transfer sequence.
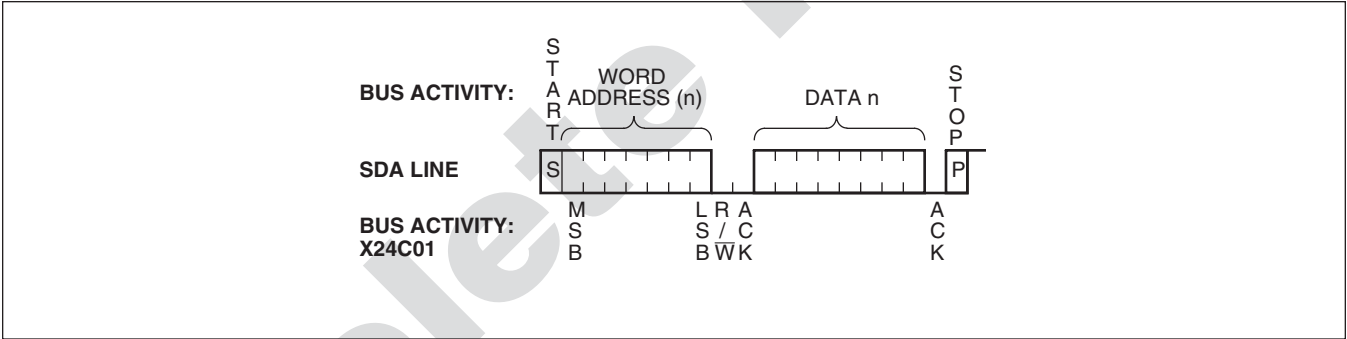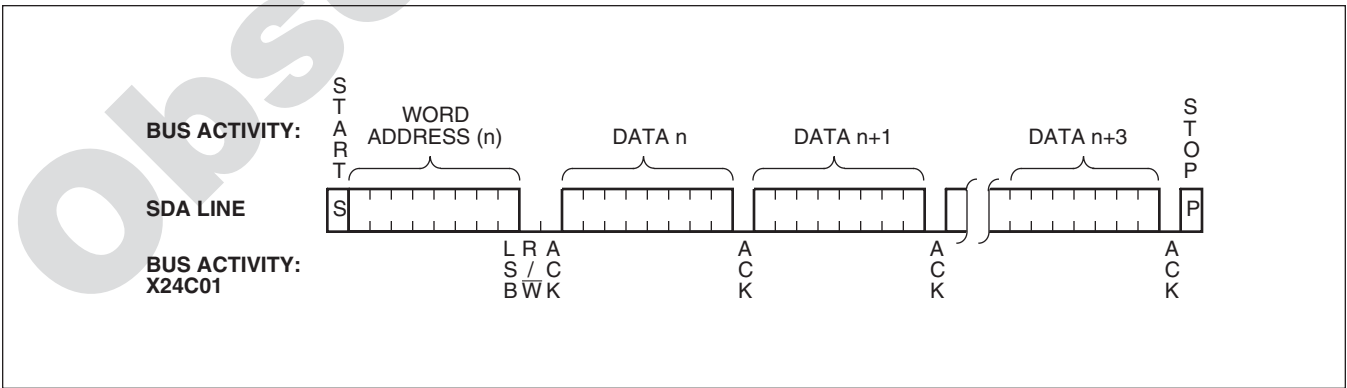
Figure 4. Byte Write

Figure 5. Page Write

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Acknowledge Polling

The disabling of the inputs can be used to take advantage of the typical 5 ms write cycle time. Once the stop condition is issued to indicate the end of the host's write operation, the X24C01 initiates the internal write cycle. ACK polling can be initiated immediately. This involves issuing the start condition followed by the word address for a write operation. If the X24C01 is still busy with the write operation, no ACK will be returned. If the X24C01 has completed the write operation an ACK will be returned, and the controller can then proceed with the next read or write operation.

READ OPERATIONS

Read operations are initiated in the same manner as write operations, with the exception that the $R/\overline{W}$ bit of the word address is set to a one. There are two basic read operations: byte read and sequential read.

It should be noted that the ninth clock cycle of the read operation is not a "don't care." To terminate a read operation, the master must either issue a stop condition during the ninth cycle or hold SDA HIGH during the ninth clock cycle and then issue a stop condition.

Byte Read

To initiate a read operation, the master sends a start condition followed by a seven bit word address and a read bit. The X24C01 responds with an acknowledge and then transmits the eight bits of data. The read operation is terminated by the master by not responding with an acknowledge and issuing a stop condition. Refer to Figure 7 for the start, word address, read bit, acknowledge and data transfer sequence.
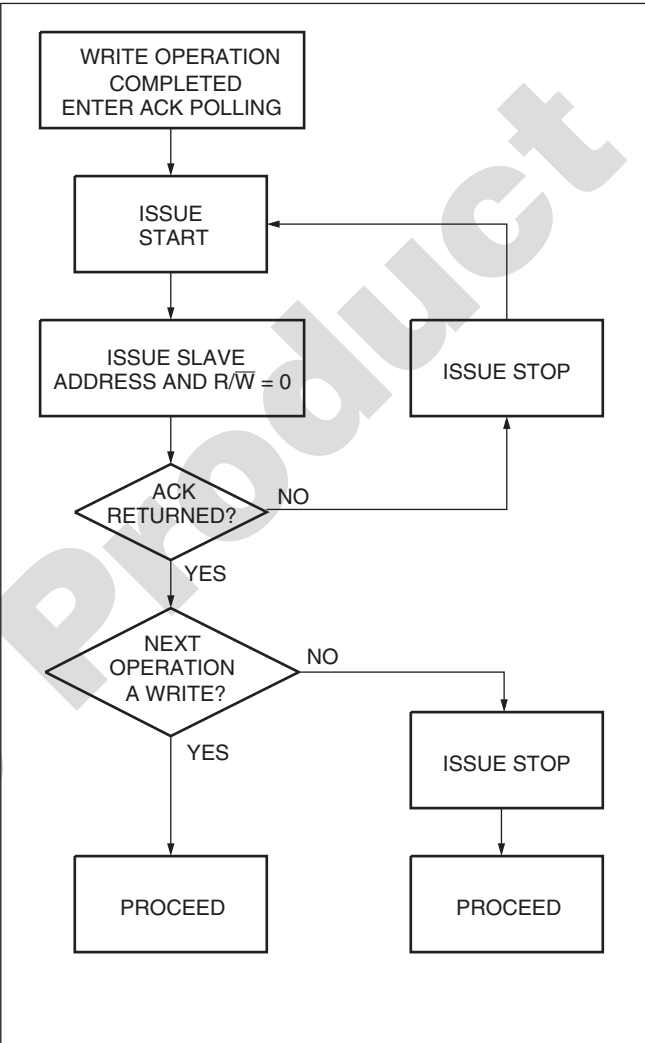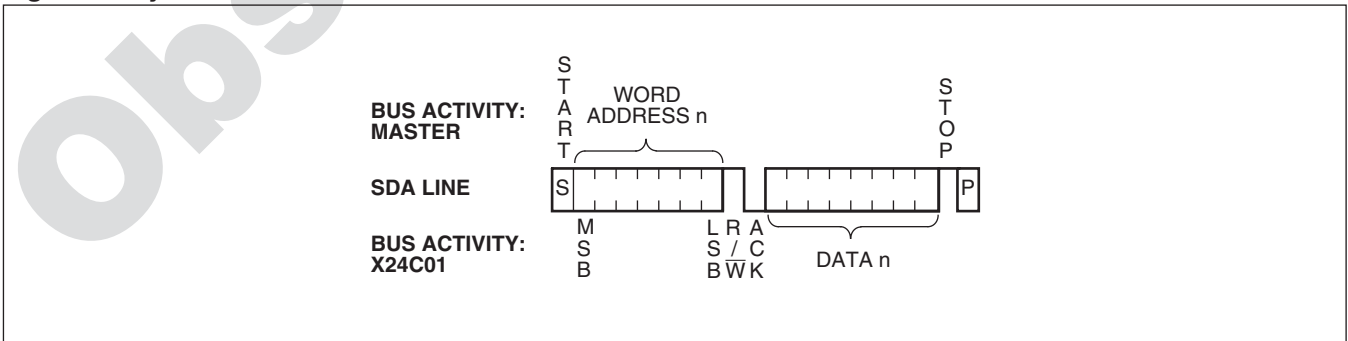
Figure 6. ACK Polling Sequence

Figure 7. Byte Read

Sequential Read

Sequential read is initiated in the same manner as the byte read. The first data byte is transmitted as with the byte read mode, however, the master now responds with an acknowledge, indicating it requires additional data. The X24C01 continues to output data for each acknowledge received. The read operation is terminated by the master by not responding with an acknowledge, and issuing a stop condition.

The data output is sequential, with the data from address n followed by the data from n + 1. The address counter for read operations increments all address bits, allowing the entire memory contents to be serially read during one operation. At the end of the address space (address 127) the counter "rolls over" to zero and the X24C01 continues to output data for each acknowledge received. Refer to Figure 8 for the address, acknowledge and data transfer sequence.
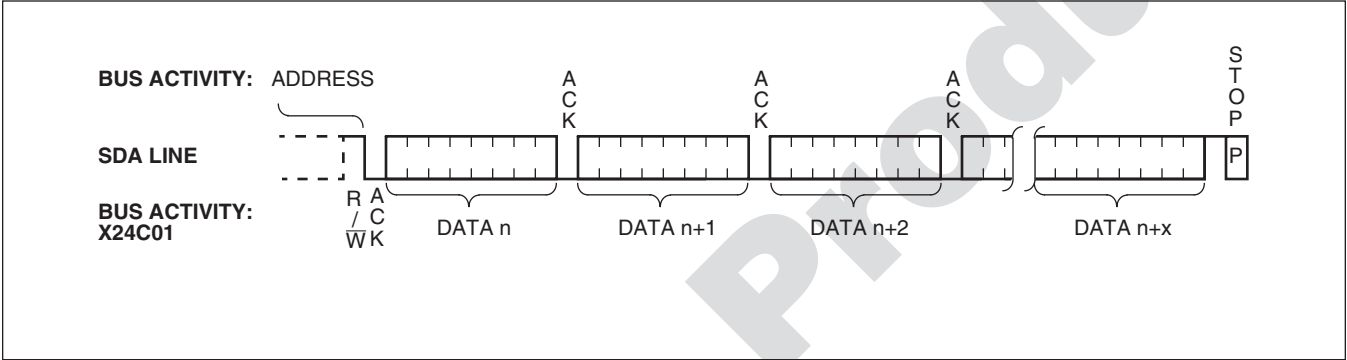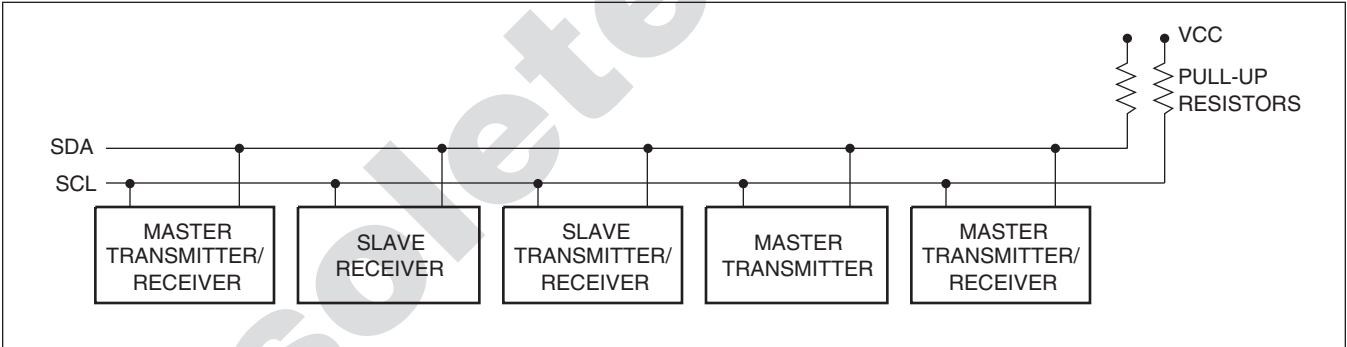
Figure 8. Sequential Read

Figure 9. Typical System Configuration

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ABSOLUTE MAXIMUM RATINGS

Temperature under bias ....–65°C to +135°C
Storage temperature ....–65°C to +150°C
Voltage on any pin with
   respect to VSS ....–1.0V to +7.0V
D.C. output current .... 5 mA
Lead temperature...
   (soldering, 10 Seconds)................................300°C

RECOMMENDED OPERATING CONDITIONS

Temperature	Min.	Max.
Commercial	0°C	70°C
Industrial	–40°C	+85°C
Military	–55°C	+125°C

COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only; functional operation of the device (at these or any other conditions above those indicated in the operational sections of this specification) is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Supply Voltage	Limits
X24C01	4.5V to 5.5V
X24C01-3.5	3.5V to 5.5V
X24C01-3	3.0V to 5.5V
X24C01-2.7	2.7V to 5.5V

D.C. OPERATING CHARACTERISTICS (Over recommended operating conditions, unless otherwise specified)

Symbol	Parameter	LIMITS Min.	LIMITS Max.	Units	Test Conditions
I_{CC}[1]	V_{CC} supply current (read)		1	mA	SCL = V_{CC} x 0.1/V_{CC} x 0.9 Levels @ 100 KHz, SDA = Open
I_{CC}[2]	V_{CC} supply current (write)		2		
I_{SB1}[1]	V_{CC} standby current		100	µA	SCL = SDA = V_{CC}, V_{CC} = 5V ± 10%
I_{SB2}[1]	V_{CC} standby current		50	µA	SCL = SDA = V_{CC}, V_{CC} = 2.7V
I_{LI}	Input leakage current		10	µA	V_{IN} = GND to V_{CC}
I_{LO}	Output leakage current		10	µA	V_{OUT} = GND to V_{CC}
V_{IL}[2]	Input low voltage	–1.0	V_{CC} x 0.3	V	
V_{IH}[2]	Input high voltage	V_{CC} x 0.7	V_{CC} + 0.5	V	
V_{OL}	Output low voltage		0.4	V	I_{OL} = 2.1 mA

CAPACITANCE T_A = 25°C, F = 1.0 MHz, V_{CC} = 5V

Symbol	Parameter	Max.	Units	Test Conditions
$C_{I/O}$[3]	Input/Output capacitance (SDA)	8	pF	$V_{I/O}$ = 0V
C_{IN}[3]	Input capacitance (SCL)	6	pF	V_{IN} = 0V

Notes: (1) Must perform a stop command prior to measurement.
       (2) V_{IL} min. and V_{IH} max. are for reference only and are not tested.
       (3) This parameter is periodically sampled and not 100% tested.

A.C. CHARACTERISTICS (Over recommended operating conditions, unless otherwise specified)

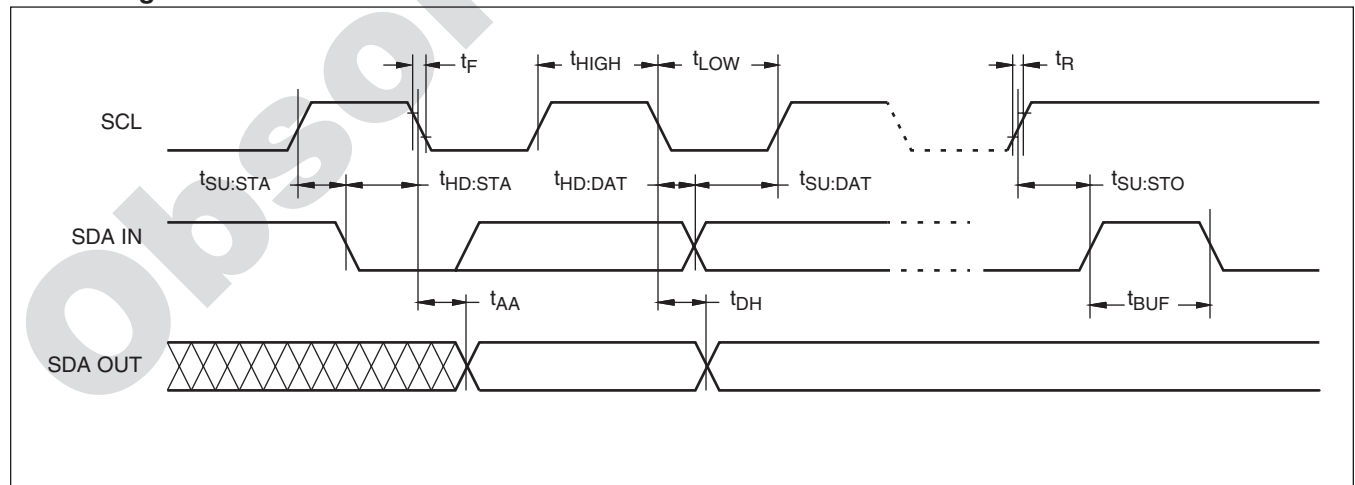### Read & Write Cycle Limits

Symbol	Parameter	Min.	Max.	Units
f_{SCL}	SCL clock frequency	0	100	KHz
T_I	Noise suppression time constant at SCL, SDA inputs		100	ns
t_{AA}	SCL low to SDA data out valid	0.3	3.5	µs
t_{BUF}	Time the bus must be free before a new transmission can start	4.7		µs
$t_{HD:STA}$	Start condition hold time	4.0		µs
t_{LOW}	Clock low period	4.7		µs
t_{HIGH}	Clock high period	4.0		µs
$t_{SU:STA}$	Start condition setup time	4.7		µs
$t_{HD:DAT}$	Data in hold time	0		µs
$t_{SU:DAT}$	Data in setup time	250		ns
t_R	SDA and SCL rise time		1	µs
t_F	SDA and SCL fall time		300	ns
$t_{SU:STO}$	Stop condition setup time	4.7		µs
t_{DH}	Data out hold time	300		ns

POWER-UP TIMING

Symbol	Parameter	Max.	Units
t_{PUR}[4]	Power-up to read operation	1	ms
t_{PUW}[4]	Power-up to write operation	5	ms

Bus Timing

Notes: (4) t_{PUR} and t_{PUW} are the delays required from the time V_{CC} is stable until the specified operation can be initiated. These parameters are periodically sampled and not 100% tested.

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WRITE CYCLE LIMITS

Symbol	Parameter	Min.	Typ.(5)	Max.	Units
t_{WR}[6]	Write Cycle Time		5	10	ms

The write cycle time is the time from a valid stop condition of a write sequence to the end of the internal erase/program cycle. During the write cycle, the X24C01 bus interface circuits are disabled, SDA is allowed to remain high, and the device does not respond to its word address.

Write Cycle Timing
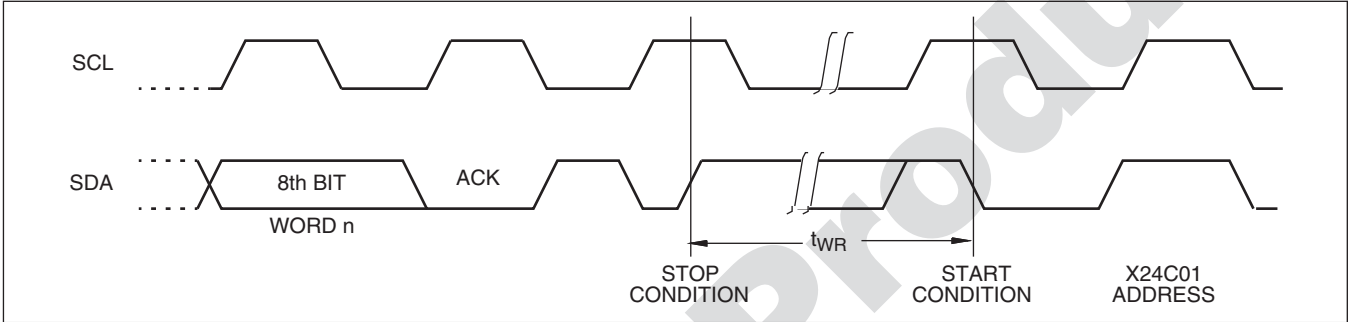
Notes: (5) Typical values are for $T_A = 25°C$ and nominal supply voltage (5V).

(6) t_{WR} is the minimum cycle time to be allowed from the system perspective unless polling techniques are used. It is the maximum time the device requires to automatically complete the internal write operation.

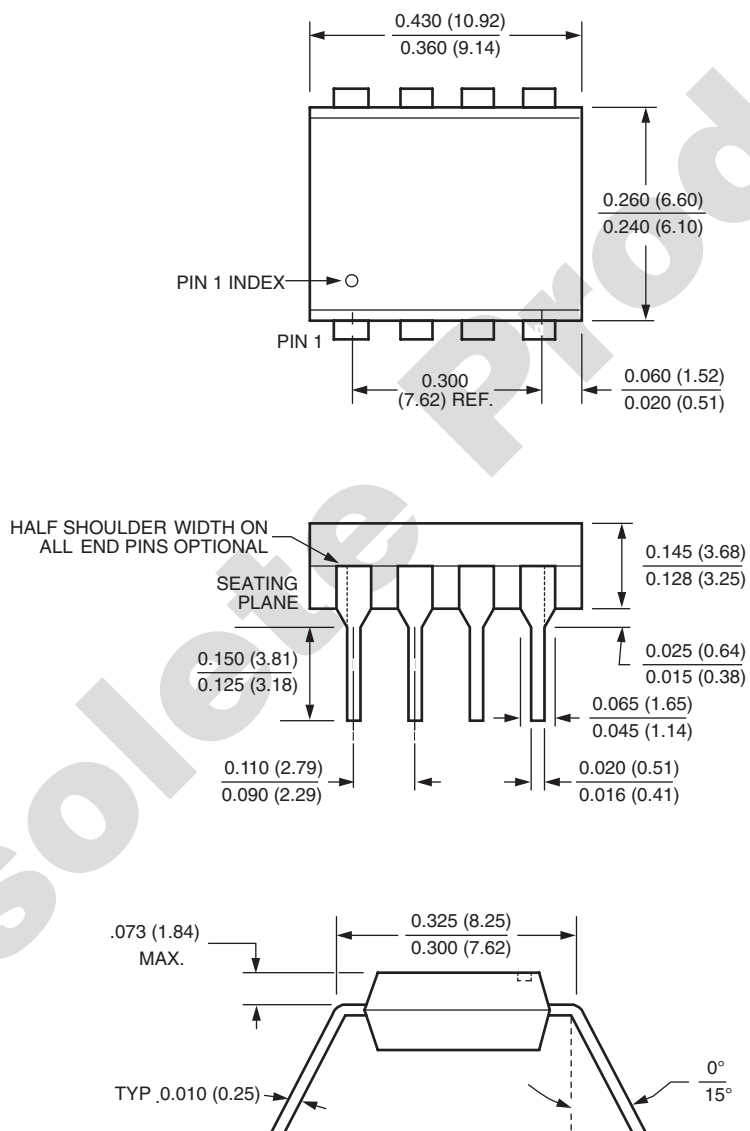### Guidelines for Calculating Typical Values of Bus Pull-Up Resistors

$$R_{MIN} = \frac{V_{CC} \, MAX}{I_{OL} \, MIN} = 2.6K$$

$$R_{MAX} = \frac{t_R}{C_{BUS}}$$
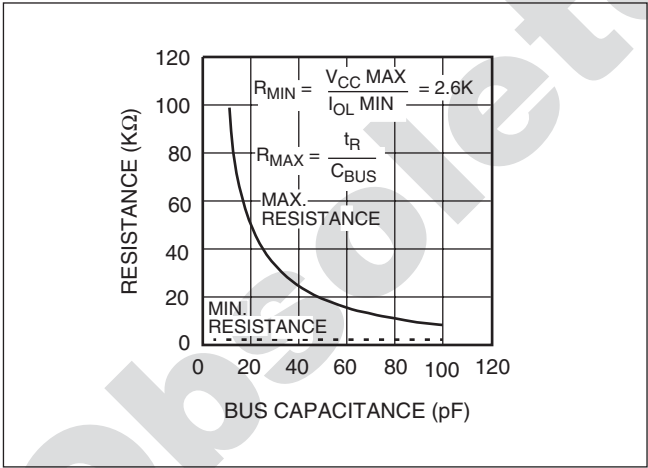
SYMBOL TABLE

WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from LOW to HIGH	Will change from LOW to HIGH
	May change from HIGH to LOW	Will change from HIGH to LOW
	Don't Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance

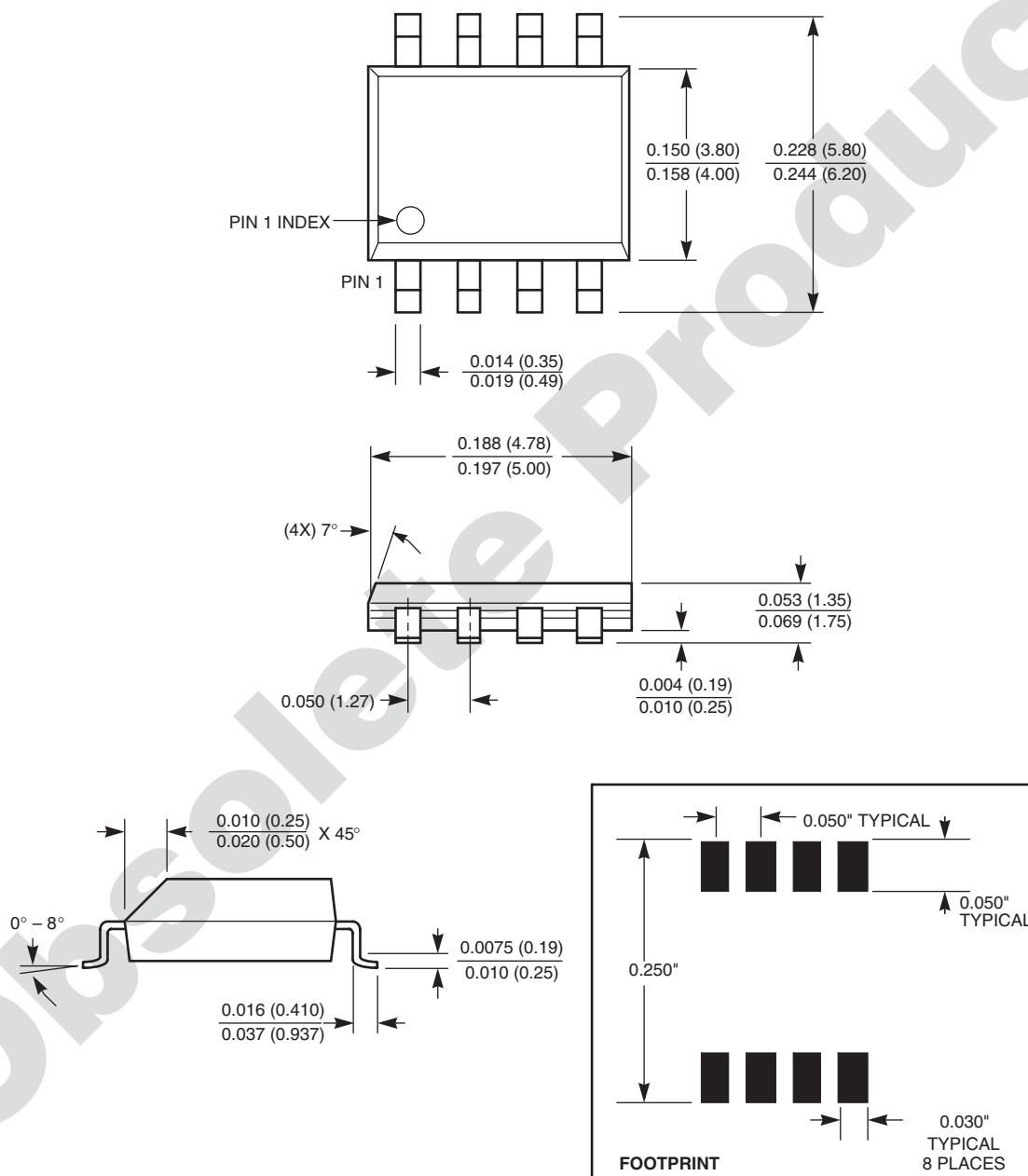## PACKAGING INFORMATION

8-Lead Plastic, PDIP, Package Code P8

0.430 (10.92)
0.360 (9.14)

0.260 (6.60)
0.240 (6.10)

PIN 1 INDEX

PIN 1

0.300
(7.62) REF.

0.060 (1.52)
0.020 (0.51)

HALF SHOULDER WIDTH ON
ALL END PINS OPTIONAL

SEATING
PLANE

0.145 (3.68)
0.128 (3.25)

0.025 (0.64)
0.015 (0.38)

0.150 (3.81)
0.125 (3.18)

0.065 (1.65)
0.045 (1.14)

0.110 (2.79)
0.090 (2.29)

0.020 (0.51)
0.016 (0.41)

.073 (1.84)
MAX.

0.325 (8.25)
0.300 (7.62)

TYP .010 (0.25)

0°
15°

NOTE:
1. ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)
2. PACKAGE DIMENSIONS EXCLUDE MOLDING FLASH

PACKAGING INFORMATION

8-Lead Plastic, SOIC, Package Code S8

PIN 1 INDEX

PIN 1

0.150 (3.80)
0.158 (4.00)

0.228 (5.80)
0.244 (6.20)

0.014 (0.35)
0.019 (0.49)

0.188 (4.78)
0.197 (5.00)

(4X) 7°

0.053 (1.35)
0.069 (1.75)

0.050 (1.27)

0.004 (0.19)
0.010 (0.25)

0.010 (0.25)
0.020 (0.50) X 45°

0° − 8°

0.0075 (0.19)
0.010 (0.25)

0.016 (0.410)
0.037 (0.937)

0.050" TYPICAL

0.050" TYPICAL

0.250"

0.030" TYPICAL
8 PLACES

FOOTPRINT

NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)

PACKAGING INFORMATION

8-Lead Plastic, MSOP, Package Code M8

0.118 ± 0.002
(3.00 ± 0.05)

0.012 + 0.006 / -0.002
(0.30 + 0.15 / -0.05)

0.0256 (0.65) TYP

R 0.014 (0.36)

0.118 ± 0.002
(3.00 ± 0.05)

0.030 (0.76)

0.0216 (0.55)

0.036 (0.91)
0.032 (0.81)

7° TYP

0.040 ± 0.002
(1.02 ± 0.05)

0.008 (0.20)
0.004 (0.10)

0.007 (0.18)
0.005 (0.13)

0.150 (3.81)
REF.

0.193 (4.90)
REF.

0.0256"TYPICAL

0.025"
TYPICAL

0.220"

0.020"
TYPICAL
8 PLACES

FOOTPRINT

NOTE:
1. ALL DIMENSIONS IN INCHES AND (MILLIMETERS)
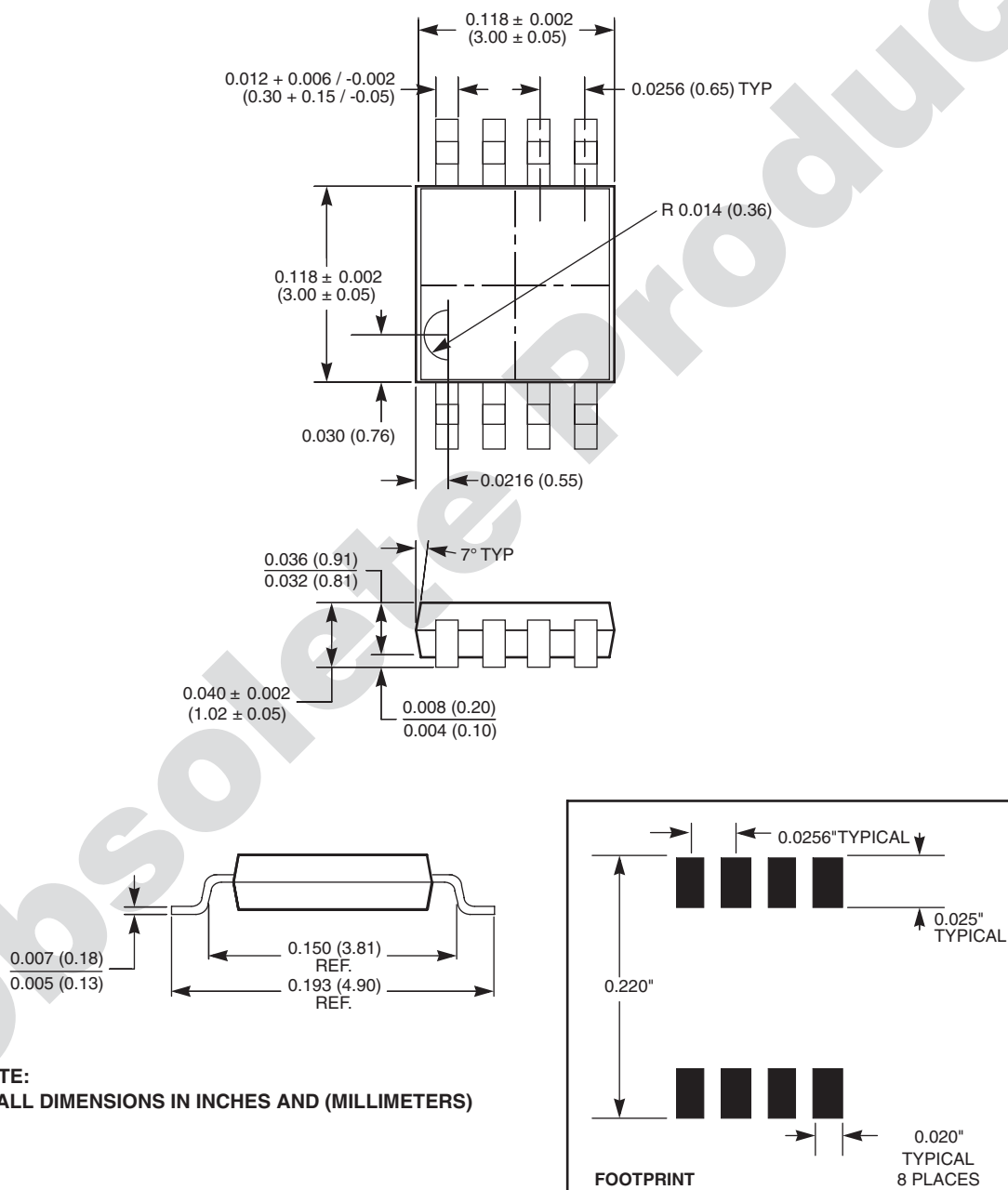
X24C01

ORDERING INFORMATION

X24C01 X X -X

Device

V_{CC} Limits
Blank = 4.5V to 5.5V
3.5 = 3.5V to 5.5V
3 = 3.0V to 5.5V
2.7 = 2.7V to 5.5V

Temperature Range
Blank = Commercial = 0°C to +70°C
I = Industrial = –40°C to +85°C
M = Military = –55°C to +125°C

Package
P = 8-Lead plastic DIP
S = 8-Lead SOIC
M = 8-Lead MSOP

Part Mark Convention

X24C01 X

Blank = 8-Lead SOIC
P = 8-Lead Plastic DIP
M = 8-Lead MSOP

X

Blank = 4.5V to 5.5V, 0°C to +70°C
F = 2.7V to 5.5V, 0°C to +70°C
G = 2.7V to 5.5V, –40°C to +85°C
I = 4.5V to 5.5V, –40°C to +85°C
B = 3.5V to 5.5V, 0°C to +70°C
C = 3.5V to 5.5V, –40°C to +85°C
D = 3.0V to 5.5V, 0°C to +70°C
E = 3.0V to 5.5V, –40°C to +85°C
M = 4.5V to 5.5V, –55°C to +125°C