TOSHIBA

TC55257DPL/DFL/DFTL-55L/70L/85L

PRELIMINARY

SILICON GATE CMOS

32,768 WORD x 8 BIT STATIC RAM

Description

The TC55257DPL is a 262,144 bit static random access memory organized as 32,768 words by 8 bits using CMOS technology, and operated from a single 5V power supply. Advanced circuit techniques provide both high speed and low power features with an operating current of 5mA/MHz (typ.) and a minimum cycle time of 55ns.

When $\overline{CE}$ is a logical high, the device is placed in a low power standby mode in which the standby current is 0.3μA typically. The TC55257DPL has two control inputs. Chip Enable ($\overline{CE}$) allows for device selection and data retention control, while an Output Enable input ($\overline{OE}$) provides fast memory access. Thus the TC55257DPL is suitable for use in microprocessor application systems where high speed, low power, and battery backup are required.

The TC55257DPL is offered in a standard dual-in-line 28-pin plastic package (0.6 inch width), a small outline plastic package, and a thin small outline plastic package (forward type).

Features

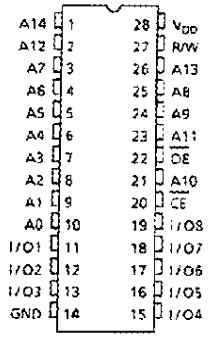
- Low power dissipation: 27.5mW/MHz (typ.)
- Standby current: 2μA (max.) at Ta = 25°C
- 5V single power supply
- Access time (max.)

	TC55257DPL/DFL/DFTL		
	-55L	-70L	-85L
Access Time	55ns	70ns	85ns
$\overline{CE}$ Access Time	55ns	70ns	85ns
$\overline{OE}$ Access Time	30ns	35ns	45ns

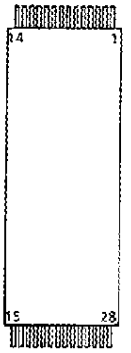
- Power down feature: $\overline{CE}$
- Data retention supply voltage: 2.0 ~ 5.5V
- Inputs and outputs directly TTL compatible
- Package TC55257DPL : DIP28-P-600
  TC55257DFL : SOP28-P-450
  TC55257DFTL : TSOP28-P

Pin Connection (Top View)

○ 28 PIN DIP & SOP



○ 28 PIN TSOP (forward type)



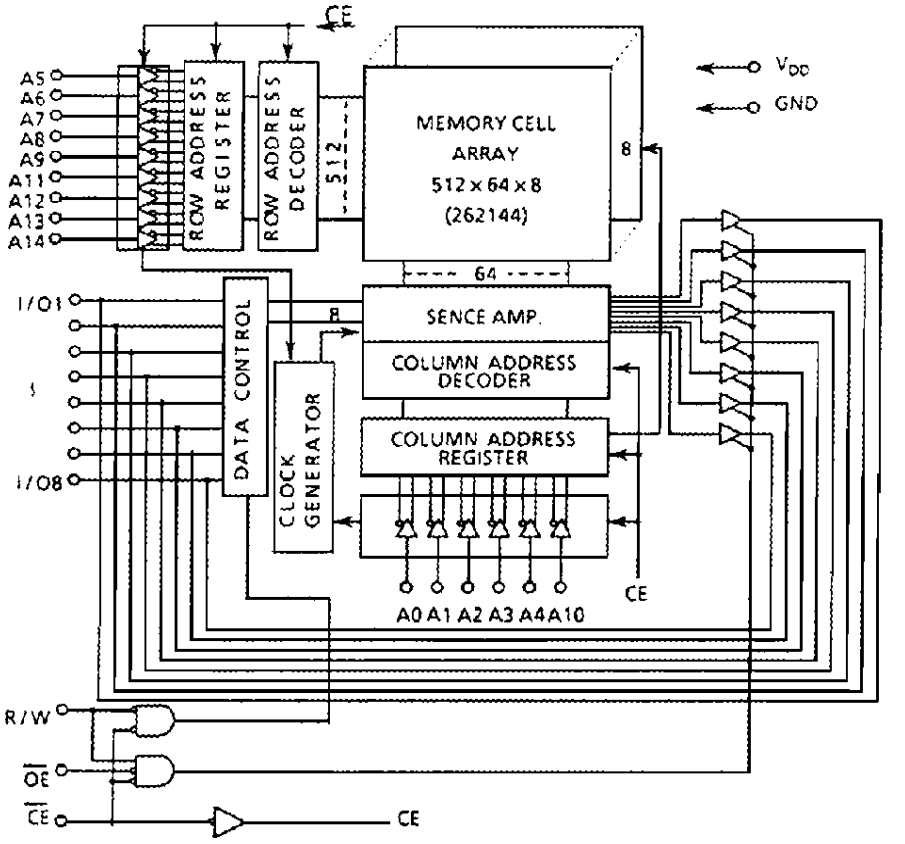
Pin Names

A0 ~ A14	Address Inputs
R/W	Read/Write Control Input
$\overline{OE}$	Output Enable Input
$\overline{CE}$	Chip Enable Input
I/O1 ~ I/O8	Data Input/Output
V_{DD}	Power (+5V)
GND	Ground

TSOP Pinout

PIN NO.	1	2	3	4	5	6	7	8	9	10	11	12	13	14
PIN NAME	$\overline{OE}$	A_{11}	A_9	A_8	A_{13}	R/W	V_{DD}	A_{14}	A_{12}	A_7	A_6	A_5	A_4	A_3
PIN NO.	15	16	17	18	19	20	21	22	23	24	25	26	27	28
PIN NAME	A_2	A_1	A_0	I/O1	I/O2	I/O3	GND	I/O4	I/O5	I/O6	I/O7	I/O8	$\overline{CE}$	A_{10}

Block Diagram



Operating Mode

OPERATION MODE	$\overline{CE}$	$\overline{OE}$	R/W	I/O1 ~ I/O8	POWER
Read	L	L	H	D_{OUT}	I_{DDO}
Write	L	*	L	D_{IN}	I_{DDO}
Output Deselect	L	H	H	High-Z	I_{DDO}
Standby	H	*	*	High-Z	I_{DDS}

* H or L

Maximum Ratings

SYMBOL	ITEM	RATING	UNIT
V_{DD}	Power Supply Voltage	-0.3 ~ 7.0	V
V_{IN}	Input Voltage	-0.3* ~ 7.0	V
$V_{I/O}$	Input and Output Voltage	-0.5* ~ V_{DD} + 0.5	V
P_D	Power Dissipation	1.0/0.6**	W
T_{SOLDER}	Soldering Temperature (10 s)	260	°C
T_{STRG}	Storage Temperature	-55 ~ 150	°C
T_{OPR}	Operating Temperature	0 ~ 70	°C

* -3.0V at pulse width 50ns
** SOP

DC Recommended Operating Conditions

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.2	–	V_{DD} + 0.3	
V_{IL}	Input Low Voltage	-0.3*	–	0.8	
V_{DH}	Data Retention Supply Voltage	2.0	–	5.5	

* -3.0V at pulse width 50ns

DC and Operating Characteristics (Ta = 0 ~ 70°C, V_{DD} = 5V±10%)

SYMBOL	PARAMETER	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Leakage Current	V_{IN} = 0 ~ V_{DD}		–	–	±1.0	µA
I_{LO}	Output Leakage Current	$\overline{CE}$ = V_{IH} or R/W = V_{IL} or $\overline{OE}$ = V_{IH} V_{OUT} = 0 ~ V_{DD}		–	–	±1.0	µA
I_{OH}	Output High Current	V_{OH} = 2.4V		-1.0	–	–	mA
I_{OL}	Output Low Current	V_{OL} = 0.4V		4.0	–	–	mA
I_{DDO1}	Operating Current	$\overline{CE}$ = V_{IL} R/W = V_{IH} Other Input = V_{IH}/V_{IL} I_{OUT} = 0mA	t_{cycle} = 1µs	–	10	–	mA
			t_{cycle} = Min. cycle	–	–	70	
I_{DDO2}		$\overline{CE}$ = 0.2V R/W = V_{DD} - 0.2V Other Input = V_{DD} - 0.2V/0.2V I_{OUT} = 0mA	t_{cycle} = 1µs	–	5	–	
			t_{cycle} = Min. cycle	–	–	60	
I_{DDS1}	Standby Current	$\overline{CE}$ = V_{IH}		–	–	3	mA
I_{DDS2}		$\overline{CE}$ = V_{DD} - 0.2V V_{DD} = 2.0V ~ 5.5V	Ta = 0 ~ 70°C	–	–	20	µA
			Ta = 25°C	–	0.3	2	

Capacitance* (Ta = 25°C, f = 1MHz)

SYMBOL	PARAMETER	TEST CONDITION	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = GND	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = GND	10	

Note: This parameter is periodically sampled and is not 100% tested.

AC Characteristics (Ta = 0 ~ 70°C, V_{DD} = 5V±10%)

Read Cycle

SYMBOL	PARAMETER	TC55257DPL/DFL/DFTL						UNIT
		-55L		-70L		-85L		
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{RC}	Read Cycle Time	55	–	70	–	85	–	ns
t_{ACC}	Address Access Time	–	55	–	70	–	85	
t_{CO}	$\overline{CE}$ Access Time	–	55	–	70	–	85	
t_{OE}	Output Enable to Output in Valid	–	30	–	35	–	45	
t_{COE}	Chip Enable ($\overline{CE}$) to Output in Low-Z	10	–	10	–	10	–	
t_{OEE}	Output Enable to Output in Low-Z	5	–	5	–	5	–	
t_{OD}	Chip Enable ($\overline{CE}$) to Output in High-Z	–	20	–	25	–	30	
t_{ODO}	Output Enable to Output in High-Z	–	20	–	25	–	30	
t_{OH}	Output Data Hold Time	10	–	10	–	10	–	

Write Cycle

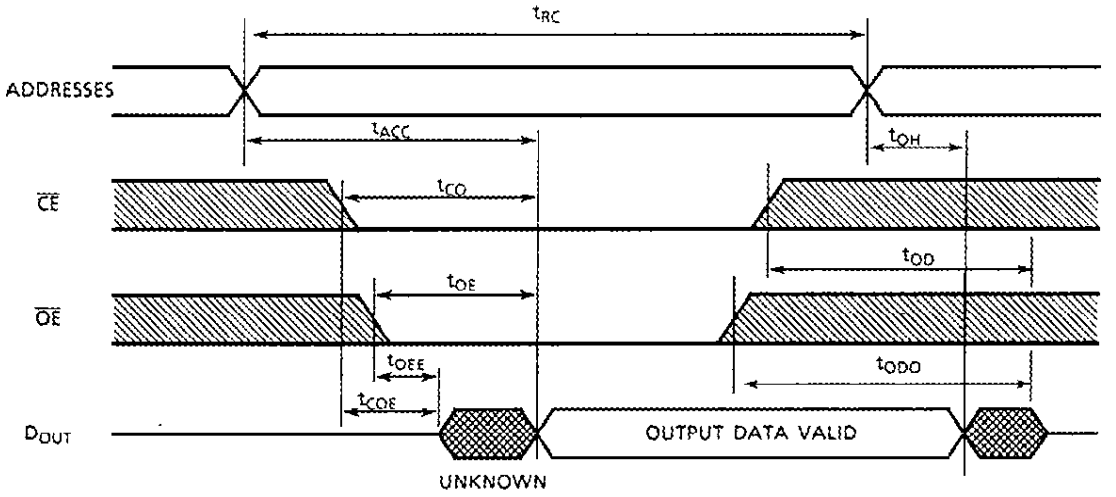
SYMBOL	PARAMETER	TC55257DPL/DFL/DFTL						UNIT
		-55L		-70L		-85L		
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{WC}	Write Cycle Time	55	–	70	–	85	–	ns
t_{WP}	Write Pulse Width	45	–	50	–	60	–	
t_{CW}	Chip Selection to End of Write	50	–	60	–	65	–	
t_{AS}	Address Setup Time	0	–	0	–	0	–	
t_{WR}	Write Recovery Time	0	–	0	–	0	–	
t_{ODW}	R/W to Output in High-Z	–	20	–	25	–	30	
t_{OEW}	R/W to Output in Low-Z	5	–	5	–	5	–	
t_{DS}	Data Setup Time	25	–	30	–	40	–	
t_{DH}	Data Hold Time	0	–	0	–	0	–	

AC Test Conditions

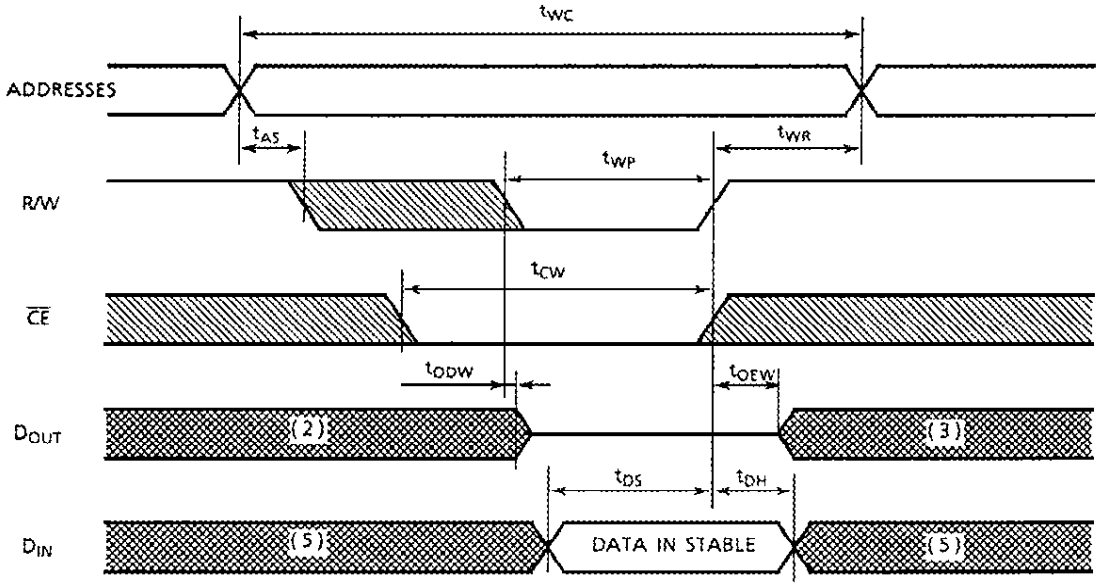
Input Pulse Levels	2.4V/0.6V
Input Pulse Rise and Fall Time	5ns
Input Timing Measurement Reference Level	1.5V
Output Timing Measurement Reference Level	1.5V
Output Load	1 TTL Gate and C_L = 30pF (-55L) 1 TTL Gate and C_L = 100pF (-70L, -85L)

Timing Waveforms

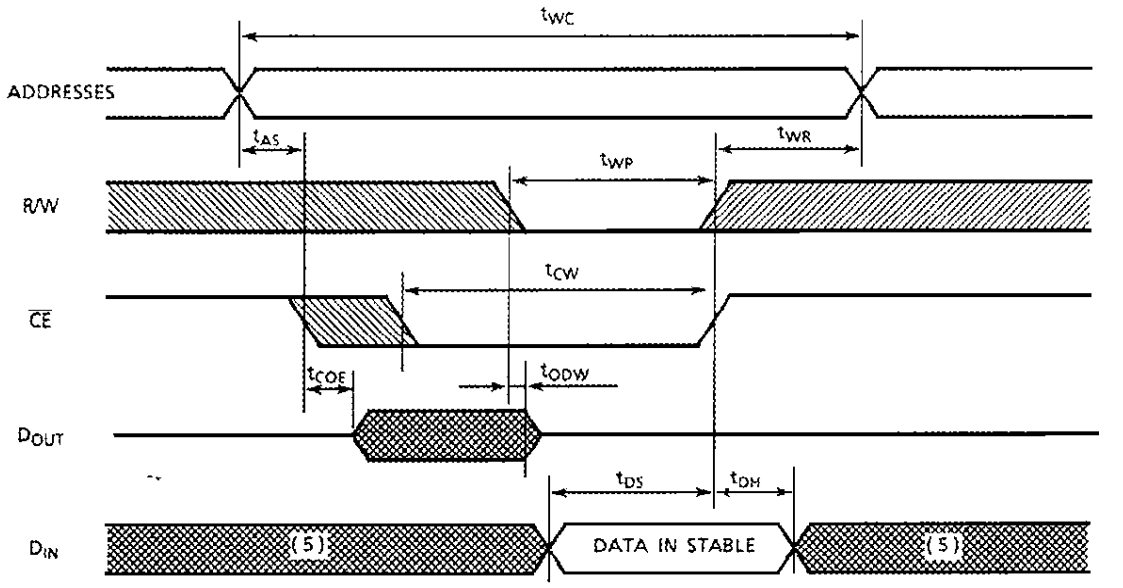
Read Cycle (1)



Write Cycle 1 (4) (R/W Controlled Write)



Write Cycle 2 [4] ($\overline{CE}$ Controlled Write)



Notes:

1. R/W is High for read cycle.
2. Assuming that $\overline{CE}$ Low transition occurs coincident with or after the R/W Low transition, Outputs remain in a high impedance state.
3. Assuming that $\overline{CE}$ High transition occurs coincident with or prior to the R/W High transition, Outputs remain in a high impedance state.
4. Assuming that $\overline{OE}$ is High for a write cycle, the Outputs are in a high impedance state during this period.
5. The I/O may be in the output state during this time; input signals of opposite phase must not be applied.

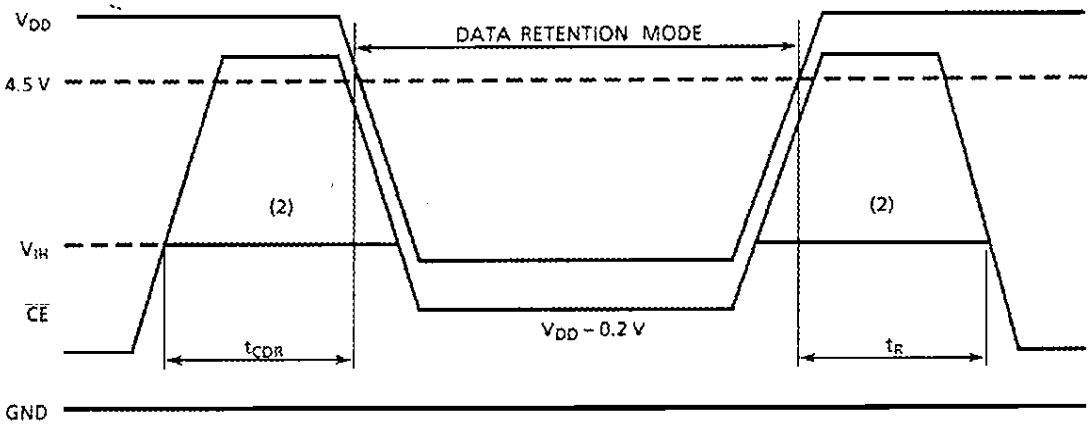
Data Retention Characteristics (Ta = 0 ~ 70°C)

SYMBOL	PARAMETER		MIN.	TYP.	MAX.	UNIT
V_{DH}	Data Retention Supply Voltage		2.0	–	5.5	V
I_{DDS2}	Standby Current	V_{DH} = 3.0V	–	–	10*	µA
		V_{DH} = 5.5V	–	–	20	
t_{CDR}	Chip Deselect to Data Retention Mode		0	–	–	ns
t_R	Recovery Time		$t_{RC(1)}$	–	–	

*: 2µA (Max.) Ta = 0 ~ 40°C

Note (1): Read Cycle Time

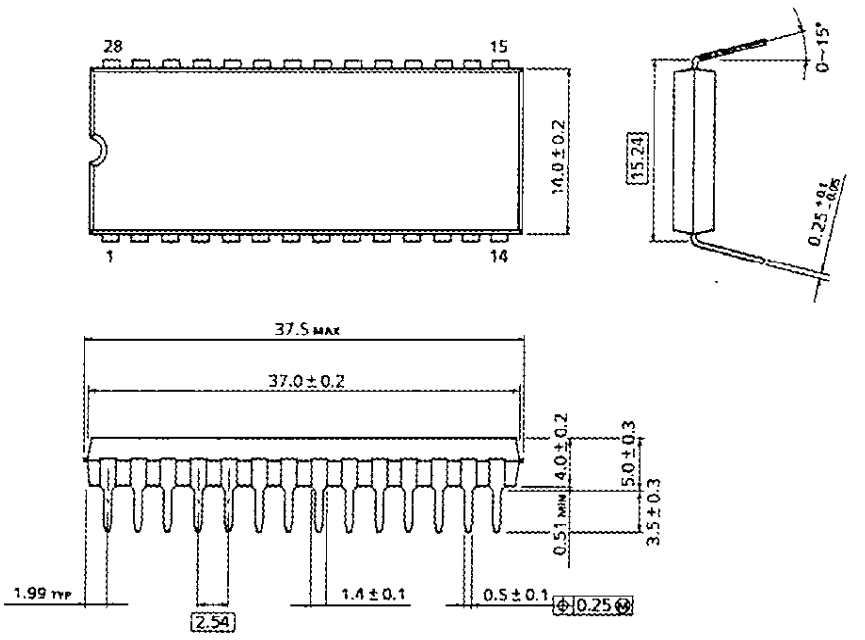
$\overline{CE}$ Controlled Data Retention Mode



Note (2): If the V_{IH} of $\overline{CE}$ is 2.2V in operation, I_{DDS1} current flows during the period that the V_{DD} voltage is going down from 4.5V to 2.4V.

Outline Drawing

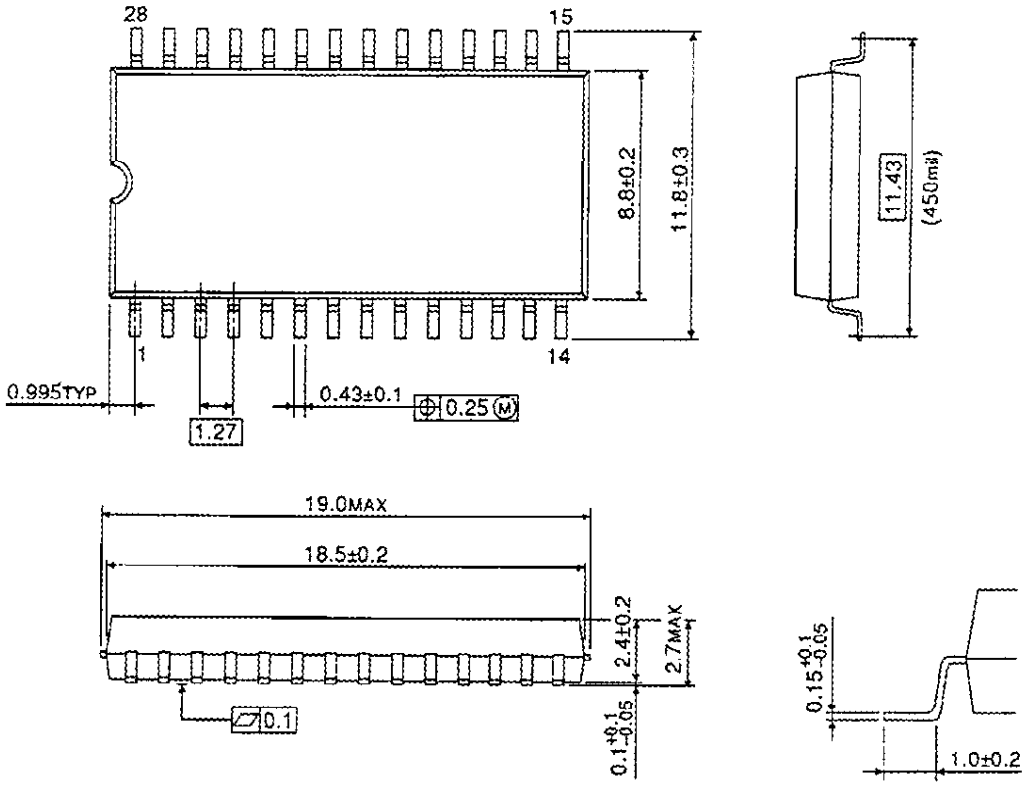
DIP28-P-600 Unit in mm



Weight : 4.42g (Typ.)

Outline Drawing

SOP28-P-450 Unit in mm

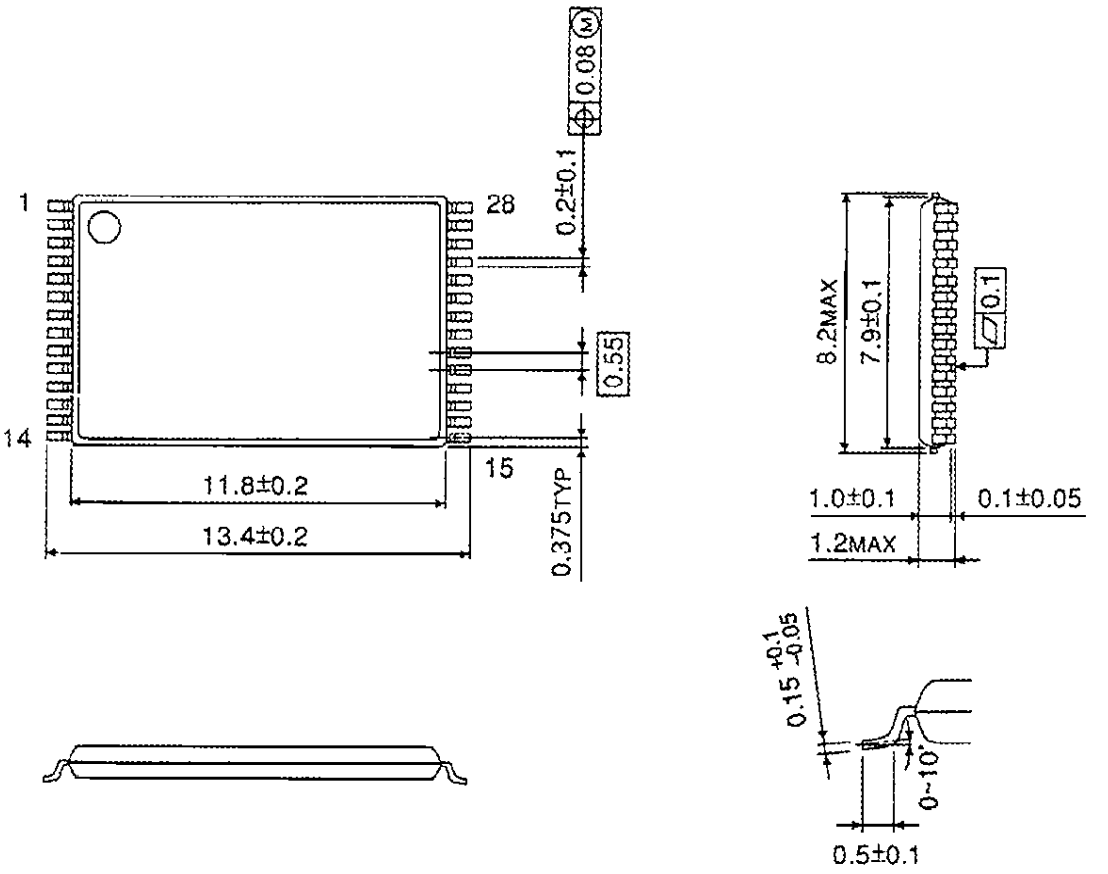


Weight : 0.79g (Typ.)

Outline Drawing

TSOP29-P

Unit in mm



Weight : 0.22g (Typ.)

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