National Semiconductor

PRELIMINARY

LMX2411
Baseband Processor for Radio Communications

General Description

The LMX2411 is a monolithic, integrated baseband processor suitable for use in Digital European Cordless Telecommunications (DECT) systems as well as other mobile telephony and wireless communications applications. It is fabricated using National's ABiC IV BiCMOS process (f_T = 15 GHz).

The LMX2411 contains both transmit and receive functions. The transmitter utilizes a low power, high speed digital-to-analog converter (DAC) and a mask programmable Read Only Memory (ROM) to generate a Gaussian filter pulse shape. The receiver includes a high speed, low power voltage comparator for making hard decisions on incoming data and a CMOS switch coupled with a sample and hold circuit for DC compensation. Supply voltage can range from 2.85V to 3.6V. The LMX2411 features very low current consumption of 2.5 mA transmit and 5 mA receive (steady state). It also has separate power down pins for transmit and receive functions to further reduce power consumption.

The LMX2411 can be used with the LMX2216B LNA/Mixer, the LMX2240 IF Receiver, and the LMX2320 Phase-Locked Loop to form a complete RF front end solution. These chips form the major blocks of an RF front end solution for DECT.

The LMX2411 is available in a 16-pin JEDEC surface mount plastic package.

Features

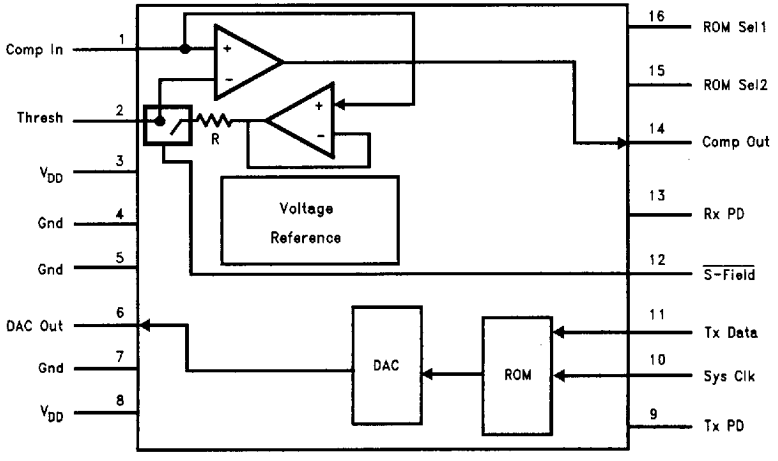
- High speed voltage comparator (40 ns settling time)
- Generates Gaussian filtered modulating signal for a direct VCO modulator
- Bit rates to 1.152 Mb/s (DECT)
- Supports 10.368, 13.824, and 18.432 MHz system clocks through pin selection
- On-chip DC compensation circuit
- Average current consumption 0.6 mA for DECT handset (burst mode operation)
- Power down mode for extended battery life
- Compatible with Sierra SC14400 and Philips PCD5040 DECT Burst Mode Controllers

Applications

- Digital European Cordless Telecommunications (DECT)
- Portable wireless communications (PCS/PCN, cordless)
- Wireless local area networks (WLANs)
- Other wireless communications systems

This data sheet contains the design specifications for product development. Specifications may change in any manner without notice.

Functional Block Diagram



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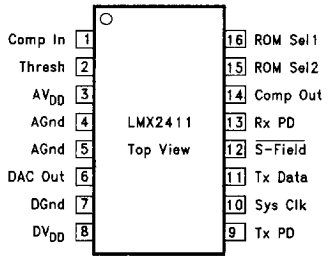
LMX2411 Connection Diagram

Small Outline Package—(SOP)



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Top View

Order Number LMX2411M
See NS Package Number M16A

Pin Description

Pin No.	Pin Name	I/O	Description
1	Comp In	I	Positive input to the threshold comparator
2	Thresh	I/O	Negative input to the threshold comparator. This pin should be connected to a DC voltage only if the internal DC compensation circuit is not used. When the DC compensation loop is used, this pin should have a capacitor to ground on it.
3	V_{DD}		Supply voltage
4	GND		Ground
5	GND		Ground
6	DAC Out	O	Output of the Gaussian filter for modulating a VCO
7	GND		Ground
8	V_{DD}		Supply voltage
9	Tx PD	I	Transmitter power down. DAC is set to 128 (HEX 80) (Mid-range) when this is HIGH.
10	Sys Clk	I	Oversampling input clock from the system (9x, 12x, or 16x the bit rate). If 12x or 16x is used, the effective sampling rate for the ROM filter is 6x or 8x, respectively.
11	Tx Data	I	Transmit data input
12	$\overline{\text{S-Field}}$	I	DC compensation circuit enable. While LOW, the DC compensation circuit is enabled, and the threshold is updated through the DC compensation loop. While HIGH, the switch is opened, and the comparator threshold is held by the external capacitor.
13	Rx PD	I	Receiver power down pin; should be grounded if power down is not used.
14	Comp Out	O	Comparator output
15	ROM Sel2	I	ROM selection pin 2. Selects the oversampling clock to be used for the ROM filter.
16	ROM Sel1	I	ROM selection pin 1. Selects the oversampling clock to be used for the ROM filter.

Gaussian ROM Selection Table

ROM Sel2	ROM Sel1	Function
0	0	10.368 MHz System Clk ROM is selected
0	1	13.824 MHz System Clk ROM is selected
1	0	18.432 MHz System Clk ROM is selected
1	1	Reserved

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Power Supply Voltage (V_{CC}) 6.5V

Storage Temperature Range (T_S) −65°C to +150°C

Lead Temperature (T_l) (Soldering, 10 Seconds) +260°C

Recommended Operating Conditions

Supply Range (V_{CC}) 2.85V to 3.6V

Operating Temperature (T_A) −10°C to +70°C

DC Electrical Characteristics

The following specifications are guaranteed over the recommended operating conditions.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
DIGITAL INTERFACE SECTION (Note 1)						
V_{OH}	High Level Output Voltage	$I_{OH} = -1.0$ mA	$V_{CC} - 0.4$			V
V_{OL}	Low Level Output Voltage	$I_{OL} = 1.0$ mA			0.4	V
V_{IH}	High Level Input Voltage		$V_{CC} - 0.8$			V
V_{IL}	Low Level Input Voltage				0.8	V
I_{IN}	Input Current	GND < V_{IN} < V_{CC}	−1.0		1.0	μA

Note 1: DC Electrical Characteristics for the digital section apply to all digital input and output pins. This includes Tx Data, Tx PD, Rx PD, Comp Out, ROM Sel1, ROM Sel2, and $\overline{\text{S-Field}}$.

Electrical Characteristics

The following specifications are guaranteed over recommended operating conditions, and oscillator (Sys Clk) frequency of 10.368 MHz unless otherwise specified.

Symbol	Parameter	Condition	Min	Typ	Max	Unit
I_{Rx}	Rx Mode Current Consumption (Note 1)	Tx Mode Off		6	7	mA
I_{Tx}	Tx Mode Current Consumption (Note 2)	Rx Mode Off		3.5	5	mA
I_{PD}	Standby Current (Power Down)	Tx and Rx Mode Off		50	100	μA
SYSTEM CLK INPUT						
V_{OSC}	Oscillator Sensitivity	Sys Clk Input	0.5			V_{PP}
f_{OSC}	Maximum Oscillator Frequency	40% < Duty Cycle < 60%	19			MHz
V_{OFF}	Oscillator DC Offset			1.5		V
I_{OSC}	Oscillator Input Current	GND < V_{IN} < V_{CC}		±30	±50	μA
TRANSMIT ROM FILTER						
t_S	DAC Voltage Settling Time to within ½ LSB	C_{LOAD} = 3 pF All 0's to all 1's		100		ns
R_{OUT}	Output Impedance (Pin 6)		2.9		4.1	kΩ
V_{OUT}	Output Voltage Swing (Pin 6) (Note 3)	Measured from 0V	0.95		1.05	V
	DAC Midband Voltage	DAC Code = 10000000	479		529	mV
	Gaussian Filter Pulse Response Accuracy (Note 4)				±0.5	%
	ISI from Gaussian Filter (Note 5)	$B_b T = 0.5$ Filter		11		%
DC COMPENSATION SAMPLE AND HOLD CIRCUIT						
V_{OS}	Input Offset Voltage				3	mV
$V_{I/O}$	Input/Output Voltage Swing	Centered at 1.5V		1		V_{PP}
R_{SH}	Sample and Hold Resistor		2240		3360	Ω
D_V	Threshold Input Voltage Droop	C_{HOLD} = 2700 pF (Pin 2)		1	10	mV/ms

Electrical Characteristics The following specifications are guaranteed over recommended operating conditions, and oscillator (Sys Clk) frequency of 10.368 MHz unless otherwise specified. (Continued)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
COMPARATOR						
t_{SET}	Settling Time	100 mV step with 5 mV Overdrive; 20 pF load		40		ns
V_{IN}	Input Voltage Range	Centered at 1.5V	1.1		2	V
I_{BIAS}	Comp In Bias Current (Pin 1)				4	μA
I_t	Threshold Input Bias Current			2.7	27	nA
V_{IOS}	Input Offset Voltage				3	mV

Note 1: Average current consumption for an 8% power up duty cycle is 8% × 6 mA = 0.48 mA; average current consumption for a 40% power up duty cycle is 40% × 6 mA = 2.4 mA.

Note 2: Average current consumption for a 5% power up duty cycle is 5% × 3.5 mA = 0.175 mA.

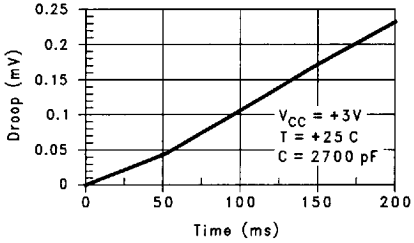
Note 3: Output range = 0 to (V_{REF} * 0.8). V_{REF} is an internal bandgap reference which produces a voltage of nominally 1.25V ±50 mV.

Note 4: Pulse response accuracy is measured as a percentage of the measured output pulse response vs. the calculated ideal Gaussian pulse response.

Note 5: ISI is Inter-symbol Interference, and is defined as the smallest peak-to-peak voltage obtained by an alternating bit pattern divided by the largest peak-to-peak voltage obtained by alternating four 1's and four 0's.

Typical Performance Characteristics

Sample and Hold Droop vs Time



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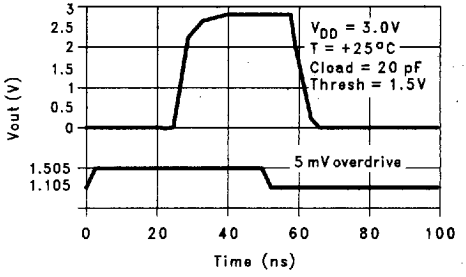
Comparator Output vs Time



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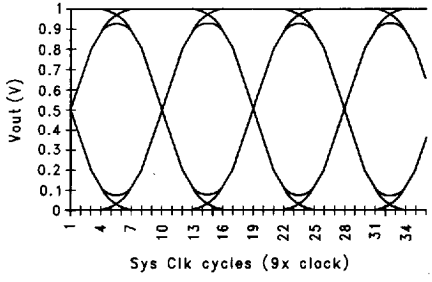
Gaussian $B_b T$ = 0.5 Output Eye Diagram



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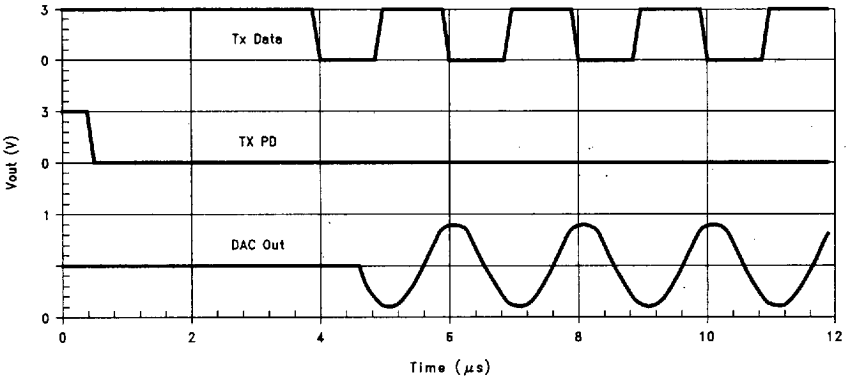
Typical Performance Characteristics (Continued)

DAC Output at Start of Transmit Burst vs Time



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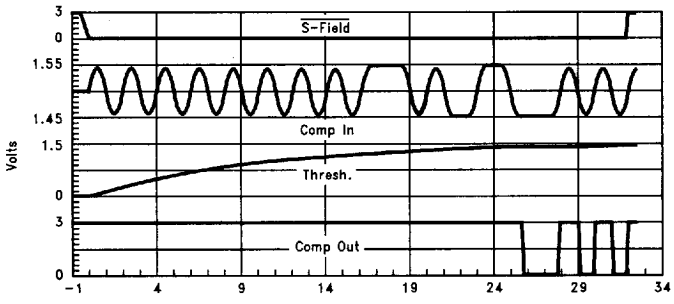
DC Comp. Circuit Response vs Time
(from Full Discharge of Hold Capacitor)
(See Application Circuit)



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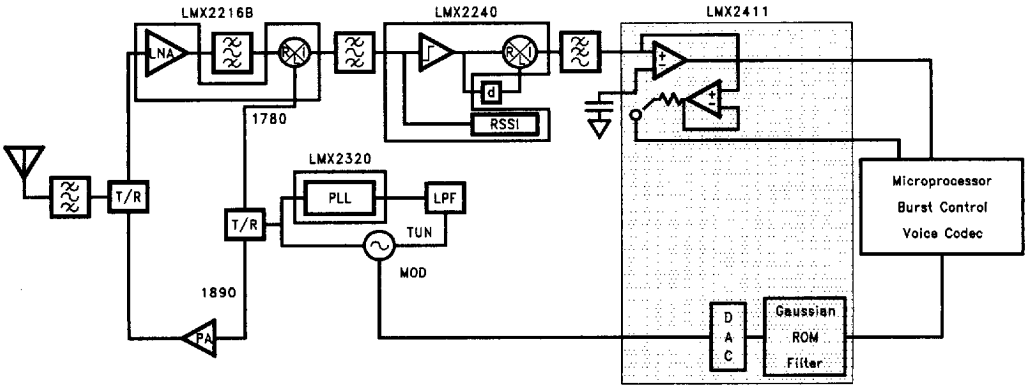
Typical Application Block Diagram



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Functional Description

OVERVIEW

The LMX2411 is a 3V integrated circuit designed to be capable of regenerating received GMSK data and generating GMSK transmitter drive signals to meet the specifications of the Digital European Cordless Telecommunications (DECT) standard.

The transmit portion of the LMX2411 functions as a pulse shaper for incoming serial data, delivering a filtered data stream capable of modulating a VCO. The ROM and supporting logic is designed to create Gaussian filter pulse responses. The output of the LPF ROM and DAC is the modulating baseband drive signal that is fed to a VCO.

The receiver section of the LMX2411 processes the filtered data stream produced by a demodulator (e.g., the LMX2240). The data stream is compared against a threshold voltage determined by the DC compensation circuit. This DC compensation circuit allows control over DC drift due to temperature, frequency drift, component tolerance, and aging.

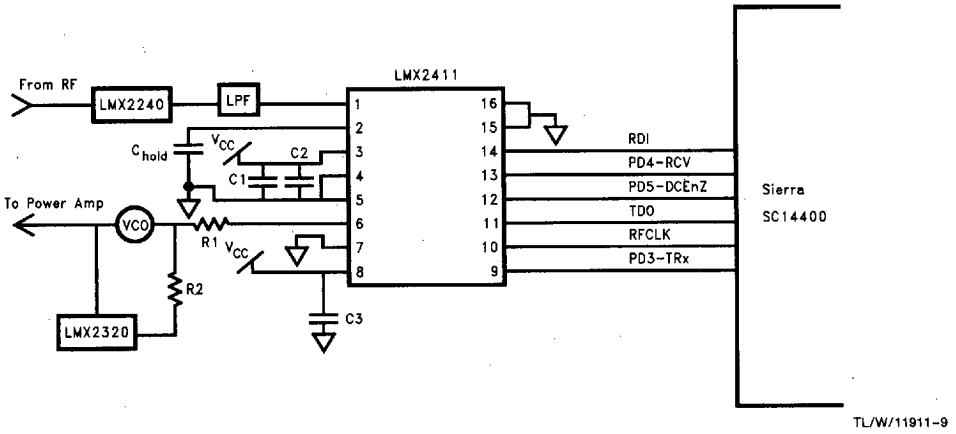
THE TRANSMIT ROM FILTER

The LMX2411 uses a mask-programmable Read-Only Memory (ROM) look-up table to construct pulse responses of a Gaussian filter shape. For DECT, this filter is half the bandwidth of the bit rate (B_b T = 0.5). The output of the ROM addresses a (voltage mode output) digital-to-analog converter (DAC). The LMX2411 ROM Filter supports three different system clocks selected by two external pins. These pins (ROM Sel1 and ROM Sel2) choose the proper oversampling clock. When the 12x or 16x clock is chosen, a divide by 2 flip flop is enabled to give the ROM a 6x or 8x clock from which to operate. However, when the 9x oversampling clock (10.368 MHz) is chosen, the divide by 2 circuit is not enabled. The Tx Data is synchronized with the Sys Clk in the following manner: When Tx PD is taken LOW, the first edge (rising or falling) of Tx Data initializes an internal counter, so that the data bits are sampled near their center. The power up state of the three bit memory in the ROM filter depends on the state of Tx Data during power down. If Tx Data is LOW when the Tx PD pin is HIGH, the ROM filter register will be set to 010. If Tx Data is HIGH when the Tx PD pin is HIGH, the ROM filter register will be set to 101. This allows the filter to be set for either base station or handset operation.

THE COMPARATOR AND ANALOG DC COMPENSATION CIRCUIT

The high speed comparator's threshold can be set either by an external voltage or by using the internal DC compensation circuit. When using the internal DC compensation loop, the received, demodulated signal is input both to the comparator "+" input and to the sample-and-hold (S&H) buffer amplifier. The S&H buffer allows a single RC filter to average the DC value of the received signal without distorting it. This DC value is connected to the "−" input of the comparator. When the signal $\overline{\text{S-Field}}$ is used (named after the synchronization field in DECT), this circuit can acquire the DC voltage during the preamble and then hold it (with the external capacitor) for the duration of the burst. This solution avoids the problem of long strings of 1's and 0's that conventional continuous averaging circuits have while still reacting quickly to acquire the proper DC average at the beginning of a burst.

Typical Application Examples



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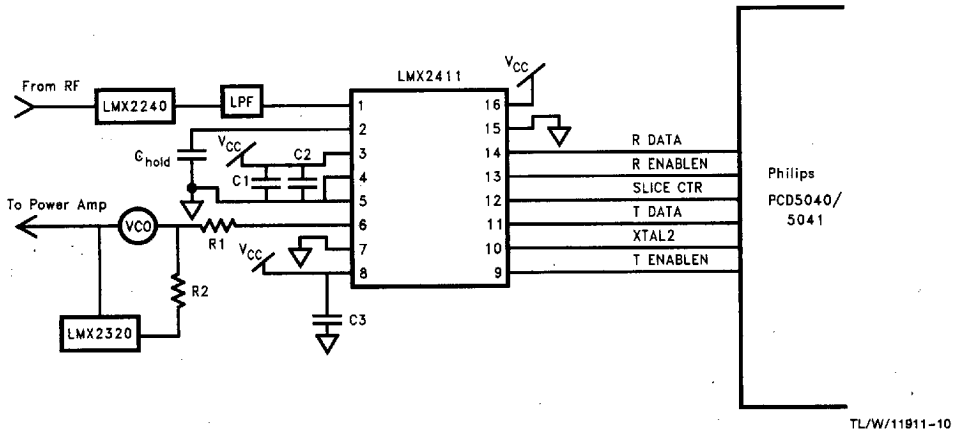
(a)



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(b)

C1 = 1 μF ±10% Tantalum (polarized) C2 = 0.01 μF ±10% NPO Ceramic
C3 = 0.01 μF ±10% NPO Ceramic C_{HOLD} = 2700 pF ±10% NPO Ceramic
R1 and R2 are 5% ¼W Thin Film Carbon (values calculated from equation (1))
LPF = 1 MHz low pass filter (Toko H354LAI-2484DDD)

Application Information

THE TRANSMIT DAC

The transmit DAC uses a voltage mode output. By nature, the output impedance of voltage mode DACs is relatively high. To conserve current, the output impedance of the LMX2411 was designed at 3 kΩ. This results in very low current consumption in the resistor strings, but also results in low drive capability. The user should be aware that in order to achieve the minimum settling time, the maximum capacitive load for the DACs should be no more than 3 pF. To achieve a settling time suitable for DECT bit rates, the maximum capacitive load the transmit DAC should see is about 15 pF.

VCO modulation of a TDD and/or TDMA radio requires some compromise to the VCO phase-locked loop circuitry. A common practice is to use a very narrow PLL loop bandwidth to avoid distorting the modulating signal. However, this is not an effective technique when fast switching is required. Rapid switching times demand a wide loop bandwidth. A typical loop bandwidth of 20 kHz will distort the lower frequency components of the DECT modulating signal.

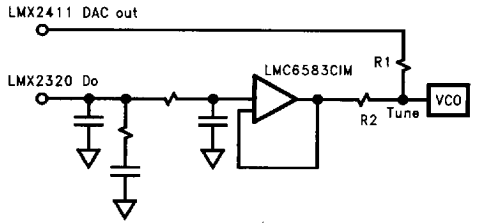

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FIGURE 1. Illustration of a Circuit That Could Be Used to Modulate an Open Loop VCO.

An alternate modulation technique is to open the loop by powering down the PLL, which in the LMX2320 results in a TRI-STATE® at the charge pump output. For short bursts, the loop filter will not lose the charge, and the center frequency will not drift. *Figure 1* shows a sample circuit for modulating on an open loop. Note that the VCO requires only one tuning port for both locking and modulation. R1 and R2 will vary depending on which wideband VCO is used. The proper equation to be used in determining R1 and R2 is below:

$$V_{DAC} * \frac{R2}{R1 + R2} * K_V = 576\ kHz \qquad (1)$$

In this case, K_V is the VCO sensitivity, expressed in MHz/V, and V_{DAC} is nominally 1V. Generally, R1 will be on the order of 50 kΩ to 250 kΩ, and the ratio of R1 to R2 will vary from 30:1 to 50:1 for wideband VCOs, and will be smaller for narrowband VCOs. Also, the 576 kHz is the peak to peak frequency deviation for DECT, which means the peak is half of that, or 288 kHz.

The Gaussian filter ROM DAC uses a three bit memory to represent the filter's pulse response. The result is an effective 3 bit time delay from input of the first bit to when that bit is actually output from the filter. When using the LMX2411 transmit section, the bits must be sent two bit times before they must be seen at the antenna to account for this small delay in the ROM DAC. There is also a half bit sample delay to allow the 2411 to sample the data near the center of the bit. Also, the end of the information data stream must be padded by 3 bits to push the last data bit through the filter. Finally, it should be noted that after the Tx PD pin goes low, the ROM filter output will be at the mid-band voltage until the first edge of Tx Data, which is used for synchronizing the internal clock with the transmitted data.

The three bit address of the ROM filter is preset to an alternating pattern when Tx PD is HIGH. The value of the alternating pattern depends on the polarity of Tx Data when Tx PD is HIGH. If Tx Data is HIGH (handset), the three bit memory is set to 101, and if Tx Data is LOW (base station), the three bit memory is set to 010. This allows for either the base station or handset preamble.

When beginning the burst for open loop modulation, the Tx Data line should be held constant at the polarity opposite to the first bit to be transmitted. For handsets, this means Tx Data should be HIGH; for base stations, this means Tx Data should be LOW. When Tx PD goes LOW, the output of the ROM filter will stay at mid-band (DAC code "10000000") until the first edge on Tx Data. This allows the DAC average output voltage to be added to the PLL loop voltage while the center frequency is being acquired, thus avoiding a frequency offset problem.

THE DC COMPENSATION LOOP

The analog DC compensation loop is designed to provide a simple yet accurate way to track and correct the effects of DC drift due to center frequency drift. This loop will provide accurate representations of the center voltage of the received signal. However, on initial startup (i.e., full Hold capacitor discharge), the average DC value will not be recovered until the end of the DECT synchronization word for the first burst. The second and subsequent bursts should have the DC value recovered within the first few bits of the synchronization field. This means that in normal situations, the receiver will miss the first burst due to lack of synchronization (i.e., too many errors in the CRC).

It should be noted, however, that because the droop in the sample and hold circuit is small, a normal DECT conversation can take place without degradation. The Typical Performance Characteristics plots should be consulted for expected droop values and DC compensation loop performance.

Some burst mode controllers support a digital DC compensation method (i.e., Sierra SC14400). In this method, the duty cycle of the incoming signal is monitored by a counter, and an update value is sent to a DAC that sets the threshold value for the comparator. In this case, the LMX2411 should have the pin for $\overline{\text{S-Field}}$ pulled HIGH, and the output of the BMC's DAC should be input directly to the comparator's threshold input (pin 2).