

SANYO

No. 1339D

**LA4145, 4146**

Monolithic Linear IC

0.6 to 0.9W AF POWER AMPLIFIER

Features

- The LA4145 is especially suited for use in cassette tape recorder, radio-cassette recorder, stereo cassette player applications; the LA4146 is especially suited for use in mini musical instrument applications.
 - 0.6 W typ/ $V_{CC} = 6.0$ V, $R_L = 8 \Omega$, THD = 10 %
 - 0.9 W typ/ $V_{CC} = 6.0$ V, $R_L = 4 \Omega$, THD = 10 %
 - Minimum number of external parts required
 - Soft clip
 - Small pop noise at V_{CC} ON/OFF mode
 - Voltage gain fixed at 50 dB
- An external resistor can be connected to reduce this value.

Maximum Ratings/ $T_a = 25^\circ\text{C}$

Maximum supply voltage	V_{CC} max	Quiescent mode	9	V
		Operating mode $R_L = 8\Omega$	8	V
Maximum output current	I_o peak		500	mA
Allowable power dissipation	P_d max	50 x 50 mm ² PCB	0.9	W
Operating temperature	T_{opg}		-20 ~ +70	$^\circ\text{C}$
Storage temperature	T_{stg}		-40 ~ +150	$^\circ\text{C}$

Operating Conditions/ $T_a = 25^\circ\text{C}$

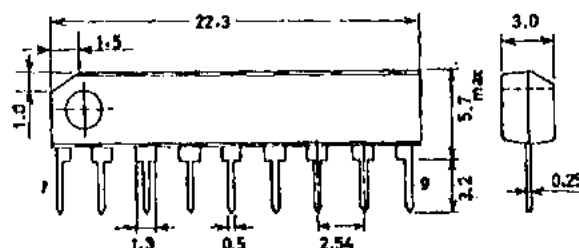
Recommended supply voltage	V_{CC}	6	V
Recommended load resistance	R_L	4 to 3	Ω
Operating voltage range	V_{CC}	3.6 to 8	V

Operating Characteristics/ $T_a = 25^\circ\text{C}$, $V_{CC} = 6.0$ V, $R_L = 8 \Omega$, $R_g = 600 \Omega$, $f = 1$ kHz

		min	typ	max	unit
Quiescent current	I_{CCQ}		10	20	mA
			5	10	mA
Voltage gain	V_G	48	50	52	dB
Output power	P_o		0.9		W
			0.6		W
Total harmonic distortion	THD		0.2	1.0	%
Input resistance	r_i		30		k Ω
Output noise voltage	V_{NO}		0.6	1.2	mV
Ripple rejection	SVRR		-40		dB

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Case Outline 3017B-S91C
(unit: mm)



SANYO: SEP9

Specifications and information herein are subject to change without notice.

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Proper care in changing voltage gain

An external resistor can be connected in series with the feedback capacitor at pin 2 to reduce the voltage gain. (See R_{NF} -VG characteristic.)

Proper cares in using IC**1. Maximum ratings**

If the IC is used in the vicinity of the maximum ratings, even a slight variation in conditions may cause the maximum ratings to be exceeded, thereby leading to breakdown. Allow an ample margin of variation for supply voltage, etc. and use the IC in the range where the maximum ratings are not exceeded.

2. Pin-to-pin short

If power is applied when the space between pins is shorted, breakdown or deterioration may occur. When mounting the IC on the board or applying power, make sure that the space between pins is not shorted with solder, etc.

3. Radio applications

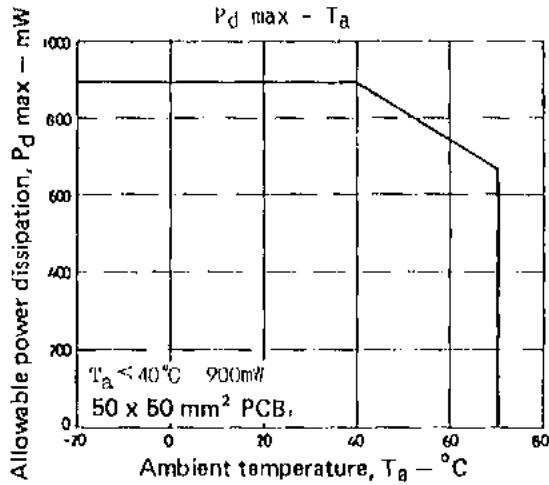
For use in radio applications, keep a good distance between IC and bar antenna.

4. Printed circuit pattern

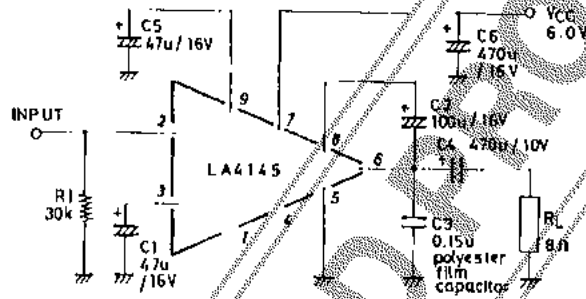
When designing the printed circuit pattern, make the power supply, output, and ground lines thicker and shorter and determine the pattern and parts placement so that no feedback loop is formed between input and output. Place power capacitor C_6 , oscillation blocking capacitor C_3 as close to the IC pin as possible to prevent oscillation from occurring. (See the sample printed circuit pattern.)

Description of external parts

- C_1 (47 μ) : Feedback capacitor (NF capacitor)
Low cutoff frequency f_L depends on this capacitor. $f_L = 90$ Hz for $C_L = 47$ μ F. Decreasing the capacitor value makes the starting time earlier.
- C_2 (100 μ) : Bootstrap capacitor
- C_3 (0.15 μ) : Oscillation blocking capacitor
It is recommended to use a polyester film capacitor being good in temperature characteristic, high frequency characteristic.
- C_4 (470 μ) : Output capacitor
- C_5 (47 μ) : Decoupling capacitor
Serves to reject ripple. The starting time depends on this capacitor. Increasing the capacitor value makes the starting time later.
- C_6 (470 μ) : Power capacitor
Place as close to the power pin of the IC as possible.
- R_1 (30 k Ω) : Input bias resistor
Serves to apply input bias. The input impedance almost entirely depends on this resistor value. If a variable resistor also serves for this purpose, this resistor can be omitted. In this case, it is recommended to use a resistor of 30 k Ω .



■ Sample Application Circuit: AF power amp



Sample Printed Circuit Pattern (Cu-foiled area)

