T-52-33-15

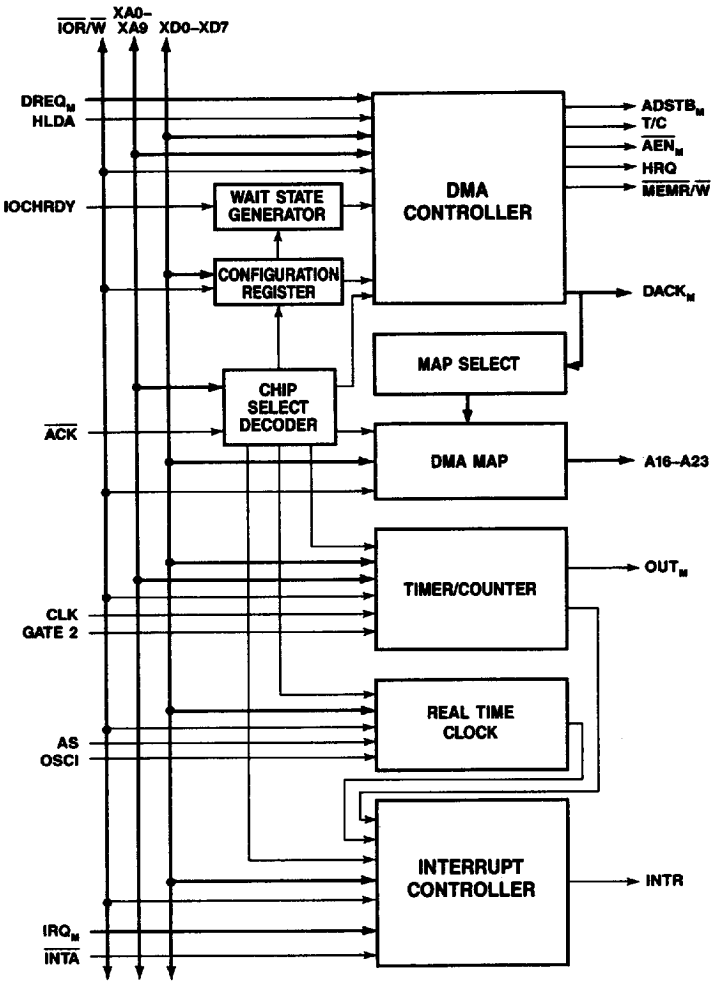
IMP82C206

IMP82C206 — Integrated Peripherals Controller

The IMP82C206 Integrated Peripheral Controller is a peripheral interface circuit. It contains two 8237 Direct Memory Access (DMA) Controllers, two 8259 Interrupt Controllers, one 8254 Timer/Counter, one MC146818 Real Time Clock, and a 74LS612 memory chip as well as several other TTL/SSI interface logic chips. In fact, all of the peripherals attached to the peripheral bus (X Bus) of the AT architecture are available in this one chip. External devices transfer information directly from the system memory to improve system performance. This chip also offers improved speed performance and additional enhanced features such as an additional 64 bytes of user RAM for the Real Time Clock and reduced recovery specifications for the DMA Controller, Timer/Counter, and Interrupt Controllers.

Features

- Compatible with IBM PC/AT
- Provides the fully-compatible equivalent of Intel's 8237 DMA Controller, 8259 Interrupt Controller, 8254 Timer/Counter, and Motorola's 146818 Real Time Clock
- Variable wait state for DMA cycles
- Programmable delays for CPU access to internal registers
- Option to select 4 or 8 MHz clock
- All CMOS implementation
- 16-bit to 8-bit transfers in bus conversion logic
- Detection logic checking and parity generation
- Accelerated recovery time of 120 ns



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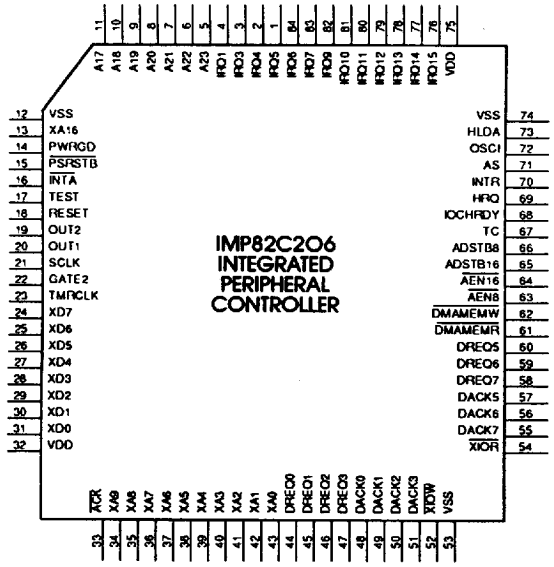

Pin Descriptions

Name	Pin Number	Pin Type	Description
XD7-XD0	24-31	I/O	**DATA BUS.** The Data Bus lines are tri-state bidirectional lines connected to the system data bus (XD bus in a PC/AT design). During DMA cycles, the first eight bits of the address are output onto the data bus to be strobed into an external latch by the Address Strobe (ADSTB8 or ADSTB16). During DMA transfers, data enters the DMA Controller on the data bus (read from memory or peripheral) or leaves the DMA Controller on the data bus (write to memory or peripheral). During I/O operations, the data bus is used as an input (writing) or output (reading) to the following: 1. DMA Controller registers — Address register — Status register — Temporary register — Word Count register 2. Three Interrupt Controller registers — Interrupt Request register — In Service register — Interrupt Mask register 3. Timer/Counters registers — contents or states of the counters 4. Real Time Clock internal registers and RAM 5. Page registers of memory mapper During the interrupt sequence, the interrupt controllers output the interrupt vector byte on the data bus.
XAB-XAO XA9	35-43 34	I/O I	**ADDRESS BUS.** The system address bus is used to address various registers of the IMP82C206. During a non-DMA cycle, A9-A0 are used to address configuration registers and the internal registers of the DMA Controller, Interrupt Controller, Timer/Counter, RTC, RAM, and Memory Mapper. In the active DMA cycle, A7-A0 are outputs and carry address information for DMA channels 0-3. Correspondingly, A8-A1 are address outputs for 16-bit DMA channels 5-7. They are tied to the external address bus (XA bus) in the PC/AT environment.
$\overline{XIOR}$	54	I/O	**I/O READ.** As an active low input, this signal is used to access the internal registers of the IMP82C206. During a DMA transfer from a peripheral, the signal becomes an output generated by the DMA Controller.
$\overline{XIOW}$	52	I/O	**I/O WRITE.** This active low input is used to write the internal registers of the IMP82C206. During a DMA transfer to a peripheral, the signal becomes an output generated by the DMA Controller.
IOCHRDY	68	I/O	**I/O CHANNEL READY.** When used as an input, a low on IOCHRDY causes the internal DMA ready signal to go low asynchronously (not ready). When IOCHRDY goes high, internal DMA Ready goes high one DMA clock cycle later. This signal is used as an input to the wait state generation logic to extend memory read and write pulses during DMA transfers. To ensure reliability, IOCHRDY must satisfy set-up and hold times of DMACLK.

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Name	Pin Number	Pin Type	Description
			As an output, this pin is an open drain output and provides an active low output whenever any register is accessed. This output will remain low for a programmed number of SCLK cycles and then go high, if pulled up by an external register. IOCHRDY provides a means of introducing a programmed number of wait-states (determined by bits 7-6 of Configuration Register 0 and bit 2 of Configuration Register 1) for I/O cycles to the IMP82C206. In the PC/AT's environment, this pin should be wire-ored to the PC/ATs IOCHRDY signal.
$\overline{ACK}$ (MSE)	33	I	**MODULE SELECT ENABLE.** The Module Select Enable signal, when high, enables the select function on one of the modules (DMA Controller, interrupt Controller CTC, RTC, DMA Page register, or the Configuration registers) for I/O reads and writes. When low, the IMP82C206 is essentially disconnected from the system bus; read and write signals are ignored. The IMP82C206, at this time, could be performing an active DMA or an interrupt cycle. In the PC/AT environment, this pin is tied to the $\overline{ACK}$ signal.
AS	71	I	**ADDRESS STROBE.** Active high Address Strobe is used to strobe an address pointer into an internal latch. The positive pulse falling edge latches the address from the XD bus.
OSCI	72	I	**OSCILLATOR INPUT.** The Oscillator Input is the time base for the clock/calendar. This frequency is determined in Register A of the RTC. External square waves of 32.768 KHz may be connected to this input.
RESET	18	I	**RESET.** Active high RESET performs initialization of the various sections of the IMP82C206.
$\overline{PSRSTB}$	15	I	**POWER SENSE.** The Power Sense pin establishes the condition of the control registers when power is applied to the device. When $\overline{PSRSTB}$ and TEST are low, the following occurs: — Periodic Interrupt Enable (PIE) bit is cleared to zero. — Periodic Interrupt Flag (PF) bit is cleared to zero. — Alarm interrupt Enable (AIE) bit is cleared to zero. — Alarm Interrupt Flag (AF) bit is cleared to zero. — Update ended Interrupt Enable (UIE) bit is cleared to zero. — Update ended Interrupt Flag (UF) bit is cleared to zero. — Interrupt Request status Flag (IRQF) is cleared to zero. — VRT bit in Register D is cleared to zero. In the PC/AT environment, this pin should be tied to the battery back-up circuit.
PWRGD	14	I	**POWER GOOD.** The Power Good pin must be high for bus cycles in which the CPU accesses the IMP82C206. When PWRGD is low, all input and output pins are disconnected from the processor. OSCI remains connected to provide battery-backed timekeeping.
TEST	17	I	**TEST.** Active high Test is an input used for test purposes only. It is tied low for normal operation.
$\overline{INTA}$	16	I	**INTERRUPT ACKNOWLEDGE.** The active low Interrupt Acknowledge is issued by the CPU. The interrupt acknolwedge sequence enables the Interrupt Controller to place its vector on the data bus.
IRQ15-IRQ9 IRQ7, IRQ6 IRQ5-IRQ3 IRQ1	76-82 83, 84 1-3 4	I	**INTERRUPT REQUESTS.** Asynchronous Interrupt Request lines. May be programmed to be edge (low to high) or level (high) sensitive.
INTR	70	O	**INTERRUPT.** Active high INTERRUPT line indicates to the CPU that an interrupt request is pending

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Name	Pin Number	Pin Type	Description
TMRCLK	23	I	**TIMER CLOCK.** The Clock input for the three counters in the CTC.
GATE2	22	I	**GATE 2.** Gate 2 is the input for Counter 2. In the PC/AT environment, it is used for speaker tone generation and is controlled by bit 0 of I/O port 061H.
OUT1	20	O	**OUT 1.** Out 1 is the output of Timer 1. In the PC/AT environment, Timer 1 is programmed as a rate generator, which produces a 15 μsec period signal that is used to request a memory refresh cycle.
OUT2	19	O	**OUT 2.** Out 2 is the output of Timer 2. In the PC/AT environment, OUT 2 drives the speaker.
SCLK	21	I	**CLOCK INPUT.** The Clock Input is used to generate the timing signals which control internal operations and DMA operations. This input may be driven from DC to 10 MHz and may be stopped in either state for standby operation. The internal clock to be used in the DMA Controller is set by bit 0 of Configuration Register 0. It can be SCLK or SCLK/2.
HLDA	73	I	**HOLD ACKNOWLEDGE.** The active high Hold Acknowledge is a signal from the CPU indicating that control of the system buses has been relinquished.
HRQ	69	O	**HOLD REQUEST.** The Hold Request output is a signal requesting control of the system buses. A HRQ is issued by the DMA Controller when a DREQ occurs and the corresponding mask bit is clear. It is also issued for a software DMA request.

Name	Pin Number	Pin Type	Description
DREQ0-DREQ3 DREQ5-DREQ7	44-47 60-58	I	**DMA REQUEST.** The DMA Requests are individual asynchronous channel request inputs used by peripherals to obtain DMA service. A request is generated by activating the DREQ line of a channel. Polarity of DREQ is programmable. DACK will acknowledge the recognition of the DREQ signal. DREQ must be maintained until the corresponding DACK goes active. In Fixed Priority, DREQ0 has the highest priority and DREQ7 has the lowest priority. Reset initializes these lines to active high. DREQ is not recognized while the clock is stopped. Unused DREQ inputs should be pulled to their inactive state and the corresponding mask bit set. DREQ0-DREQ3 support 8-bit transfers between 8-bit I/O and 8-bit or 16-bit system memory. DREQ5-DREQ7 support 16-bit data transfers between 16-bit I/O and 16-bit system memory. DREQ4 is not available for transfers as it is used to cascade DREQ0-DREQ3.
DACK0-DACK3 DACK5-DACK7	48-51 57-55	O	**DMA ACKNOWLEDGE.** The DMA Acknowledge signal notifies the requesting peripheral when a DMA cycle is granted. The active polarity of these lines is programmable. These signals are used internally for cascading the DMA channels and for DMA page register selection. Due to their use within the System, these signals must be programmed to be active low. Reset initializes the DACK signals to active low.
TC	67	O	**TERMINAL COUNT.** The active high Terminal Count (TC) output signal contains information concerning the completion of DMA services. When TC is reached, except for Channel 0 in memory-to-memory mode, a pulse is generated by the DMA Controller. The TC pulse is output when TC for channel 1 occurs during memory-to-memory transfers.

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Name	Pin Number	Pin Type	Description
			At a TC pulse occurrence, the DMA Controller terminates the service and resets the request. If an automatic initialize is set, the base registers are written to the current registers of that channel. If automatic initialize is not enabled for the channel, the mask bit and TC bit in the status word is set for the currently active channel. If automatic initialize is enabled, the mask bit remains clear.
$\overline{\text{DMAMEMR}}$	61	O	**DMA MEMORY READ.** The active low DMA Memory Read is a tri-state output. This output is used to access data from the selected memory location during DMA read or memory-to-memory transfers. In the PC/AT environment, this signal is connected to $\overline{\text{XMEMR}}$.
$\overline{\text{DMAMEMW}}$	62	O	**DMA MEMORY WRITE.** The active low DMA Memory Write is a tri-state output. This output is used to write to the selected memory location during DMA write or memory-to-memory transfers. In the PC/AT environment, this signal is connected to $\overline{\text{XMEMW}}$.
ADSTB8	66	O	**ADDRESS STROBE** for **8-BIT DMA TRANSFERS** (channels 0-3). The Address Strobe is an active high signal. It is used to latch the upper address byte (A8-A15) for 8-bit peripherals by driving the strobe input of external transparent octal latches. During block operations, this signal is only issued when the upper address byte must be altered. This eliminates S1 states and provides higher system performance.
ADSTB16	65	O	**ADDRESS STROBE** for **16-BIT DMA TRANSFERS** (channels 5-7). The Address Strobe is an active high signal. It is used to latch the upper address byte (A9-A16) for 16-bit peripherals by driving the strobe input of external transparent octal latches. During block operations, this signal is only issued when the upper address byte must be altered. This eliminates S1 states and provides higher system performance.
$\overline{\text{AEN8}}$	63	O	**ADDRESS ENABLE** for **8-BIT DMA TRANSFERS.** The Address Enable is an active low signal which enables an 8-bit latch. This latch contains the upper eight address bits (A8-A15). When the DMA does not control the system bus, this signal is inactive.
$\overline{\text{AEN16}}$	64	O	**ADDRESS ENABLE** for **16-BIT DMA TRANSFERS.** The Address Enable is an active low signal which enables an 8-bit latch. This latch contains the upper eight address bits (A9-A16). When the DMA does not control the system bus, this signal is inactive.
XA16 A23-A17	13 11-5	O O	**DMA PAGE REGISTER ADDRESS.** The DMA Page Register Addresses, XA16 and A17-A23, are tri-state output pins. A17-A23 are the upper seven bits of the DMA page register. XA16 is used for DMA transfers for 8-bit peripherals only (Channel 0-3). It is the least significant bit of the DMA page register. XA16 is not used for DMA transfers to 16-bit peripherals (Channel 5-7) as XA9-XA16 are provided by demultiplexing the data bus.
Vcc	32,75	—	**POWER SUPPLY.** DC Power supply connection. (See 'Absolute Maximum Ratings' and 'Operating Conditions' tables.)
Vss	12,53,74	—	**GROUND.** Ground connection.

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IMP82C206 — Integrated Peripherals Controller

The IMP82C206 contains the equivalent of two 8237A DMA Controllers, a 74LS612 Memory Mapper, two 8259A Interrupt Controllers, an 8254 Counter/Timer, and a MC146818 Real Time Clock with RAM. It is an implementation containing the standard peripherals required to implement an IBM PC/AT system board except the keyboard interface controller.

Two Direct Memory Access (DMA) Controllers are provided. They provide improved system performance as external devices transfer information directly from the system memory.

The controllers are connected to provide the user with a total of seven DMA channels.

DMA1 — 4 channels for 8-bit transfers
DMA2 — 3 channels for 16-bit transfers
Note: The first 16-bit DMA channel is used for cascading).

Also included in the DMA subsystem is the DMA Page Register. This device provides the A17-A23 addresses during 16-bit DMA transfers.

Sixteen interrupt channels, partitioned into two cascaded controllers (INTC1, INTC2) with eight inputs each, are provided in the IMP82C206. Three of these channels are connected internally to various devices.

Channel 0 — Counter/Timer Counter 0 Interrupt
Channel 2 — Cascade to Slave Interrupt Controller (INTC2)
Channel 8 — Real Time Clock Interrupt

The thirteen interrupt channels, not connected internally, may be user defined and utilized to meet specific system requirements.

A general purpose Counter/Timer (CTC) subsystem provides the ability to generate accurate time delays under system control. The CTC contains three independent counters. A counter may be individually programmed as a timer or as a counter.

Counter 0 is connected to Interrupt 0 of INTC1. It is intended to be used as a multi-level interrupt to the system for such tasks as timekeeping and task switching.

Counter 1 may be programmed to generate pulses or square waves for use by external devices.

Counter 2 is a full function Counter/Timer which has a gate input for controlling the internal counter. This channel can be used as an interval counter, a timer, or as a gated rate/pulse generator.

All three counters are driven from the same clock input pin. This pin is independent from the other clock inputs to the IMP82C206.

A Real Time Clock (RTC) is included in the IMP82C206. The RTC contains a time-of-day clock with alarm, calendar (one hundred year), programmable periodic interrupt, choice of BCD or binary timekeeping, time-of-day interrupts, 12 hour or 24 hour format for timekeeping, daylight savings time, automatic end-of-month detection, automatic leap year detection, and 114 bytes of low power static RAM with battery backup. This provides protection for RAM and the RTC if subjected to a loss of power.

The Top Level Decode is a multilevel decode scheme which interconnects and controls all of the major subsystems. It performs the generation of enables to the subsystems and the direction of the data bus buffers. It is also used to maintain I/O decode compatibility with the IBM PC/AT.

The Clock and Wait State Control subsystem controls the generation of DMA wait states. If programmed, it handles the negation of IOCHRDY during CPU access. This subsystem performs the generation of enables to the subsystems. Also, the control and direction of the data bus buffers are managed.

Top Level Decode

The IMP82C206 Top Level Decode provides eight separate enables to various subsystems of the device. Also, the decoder determines the control and enabling of the XD0-XD7 output buffers. These buffers are enabled whenever the internal subsystem generates an enable and the $\overline{XIOR}$ signal is asserted.

The decoder is enabled by three signals. These three signals are $\overline{ACK}$ and XA9-XA8. To enable any internal device, $\overline{ACK}$ must be one and both XA9 and XA8 must be zero. Table 1.1 contains the Top Level Decode Scheme.

SELECTED DEVICE	ADDRESS RANGE (Hex)	$\overline{ACK}$	XA9	XA8	XA7	XA6	XA5	XA4	XA3	XA2	XA1	XA0
DMA1	000-000F	1	0	0	0	0	0	0	X	X	X	X
INTC1	020-021	1	0	0	0	0	1	0	0	0	0	X
CONFIG	022-023	1	0	0	0	0	1	0	0	0	1	X
CTC	040-043	1	0	0	0	1	0	0	0	0	X	X
RTC	071	1	0	0	0	1	1	1	0	0	0	1
DMAPAGE	080-08F	1	0	0	1	0	0	0	X	X	X	X
INTC2	0A0-0A1	1	0	0	1	0	1	0	0	0	0	X
DMA2	0C0-0DF	1	0	0	1	1	0	X	X	X	X	X
DISABLED	DISABLED	0	X	X	X	X	X	X	X	X	X	X
DISABLED	DISABLED	X	1	X	X	X	X	X	X	X	X	X
DISABLED	DISABLED	X	X	1	X	X	X	X	X	X	X	X

Table 1.1 Internal Decode Scheme

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Selects to the individual subsystems are more fully decoded and designed to comply with the IBM PC/AT requirements. As the IMP82C206 will not respond to unused address spaces established by the Top Level Decoder, the user can take advantage of these areas by inserting additional peripherals in the I/O map. As output buffers are not enabled, unless an internal subsystem is enabled, extra peripherals may be tied directly to the XD0-XD7 data lines.

Clock and Wait State Control

Four functions are performed by the Clock and Wait State Control subsystem. These are:

1. Control of the DMA command width
2. Control of the CPU read cycle length
3. Control of the CPU write cycle length
4. Selection of the DMA clock rate

All of these functions may be selected by writing to the Configuration Registers located at address 023H. A read or write is accomplished by first writing an index to location 022H. This selects one of the IMP82C206 Configuration Registers. Then a read or write may be performed to address 023H.

Register Configurations

Register 0 (023H) (Index 01H)

MSB LSB

B7	B6	B5	B4	B3	B2	B1	B0
RW1	RW0	16W1	16W0	8W1	8W0	EMR	CLK

(Read/Write Register)

RW1-RW0— When higher speed CPU's are accessing the System, the cycle can be extended. By programming up to four wait states into the Configuration Register, a not ready condition on IOCHRDY (low) is asserted whenever a valid decode from the Top Level Decoder is detected and either $\overline{XIOR}$ or $\overline{XIOW}$ is asserted. IOCHRDY remains low for the number of wait states specified.

Read/Write Cycle Wait States	RW1	RW0
1	0	0
2	0	1
3	1	0
4	1	1

Wait states are in increments of one SCLK cycle and are not affected by the DMA Clock Divider.

16W1-16W0— Wait states can be independently controlled for both 8-bit and 16-bit DMA cycles. This allows the user to modify the DMA cycle to more closely fit the application.

16-Bit DMA Wait States	16W1	16W0
1	0	0
2	0	1
3	1	0
4	1	1

8W1-8W0— These bits provide the ability to program the register for wait states to be inserted in 8-bit DMA cycles.

8-Bit DMA Wait States	8W1	8W0
1	0	0
2	0	1
3	1	0
4	1	1

Note: During DMA, the IOCHRDY pin is used as an input to the wait state generation logic. This input is driven low (0) by the peripheral to extend the cycle. When the cycle is completed, IOCHRDY is released allowing it to return high (1).

EMR —This bit enables the extended $\overline{DMAMEMR}$ function. In the IBM PC/AT environment, assertion of $\overline{DMAMEMR}$ is delayed one clock cycle later than $\overline{XIOR}$.

0: $\overline{DMAMEMR}$ delayed one DMA clock cycle later than $\overline{XIOR}$
1: $\overline{DMAMEMR}$ and $\overline{XIOR}$ are enabled simultaneously

CLK —This bit allows the user to insert a divider between the DMA Controller subsystems and the SCLK input pin, or connect the two directly.

0: SCLK input is divided by two and is used to drive both the 8-bit and 16-bit DMA subsystems
1: Divider is bypassed and the SCLK input used directly

The Internal synchronizer controls the actual switching of the clock when the state of this bit changes. This prevents a short clock pulse from creating a DMA malfunction when the state changes.

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The Configuration Register 0 contents are preloaded by RESET to an initial value of 0C0H. This value establishes a default which is IBM PC/AT compatible and corresponds to:

Read/Write cycles —4 wait states
16-bit DMA transfers —1 wait state
8-bit DMA transfers —1 wait state
$\overline{\text{DMAMEMR}}$ delayed 1 DMA clock cycle later than $\overline{\text{XIOR}}$
DMA clock is equal to SCLK/2

Register 1 (023H) (Index 02H)

MSB LSB

B7	B6	B5	B4	B3	B2	B1	B0
R	R	R	R	R	NRWS	N16WS	N8WS

(Read/Write Register)

B7-B3 —Reserved bits.

NRWS —The high performance of the IMP82C206 allows CPUs, up to 20 MHz, to access the IMP82C206 with zero wait states. Setting this bit to a one allows zero wait state accesses. Setting this bit to zero allows Configuration Register 0, bits RW1-RW0, to control the number of wait states used during an IMP82C206 access. The default setting is a zero after RESET.

0: Configuration Register 0 controls number of wait states used during an access (default)
1: Zero wait state access

N16WS —To allow 16-bit DMA transfers to occur with zero wait states, this bit must be set to a one. Setting the bit to a zero allows Configuration Register 0, bits 16W1-16W0, to govern the wait states for a 16-bit DMA transfer. The default setting is zero after RESET.

0: Configuration Register 0 governs wait states (default)
1: Zero wait state access

N8WS —Setting this bit to a one will allow 8-bit DMA transfers to occur with zero wait states. Setting the bit to a zero allows Configuration Register 0, bits 8W1-8W0, to govern the wait states for an 8-bit DMA transfer. The default setting is one after RESET.

0: Configuration Register 0 governs the wait states (default)
1: Zero wait state access

Note: Setting any of these bits to one requires the system timing to be capable of supporting zero wait state accesses. None of these bits need be changed from their default settings for operations in the PC/AT environment.

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IMP82C206 — DMA Controllers

Functional Description

Two DMA controllers are implemented in the IMP82C206. These devices generate the memory addresses and control signals to transfer information directly between a peripheral device and memory with little CPU intervention.

Through the internal cascade ability, system expansion is implemented. The controllers provide multiple channels for direct memory transfers. The DMA2 Channel 0 is the cascade interconnection for the two DMA devices necessary to maintain IBM PC/AT compatibility. Four channels for transfers to 8-bit peripherals (DMA1) are provided; three channels for transfers to 16-bit peripherals (DMA2).

Cycle length can be controlled by inserting wait states or extending the command strobes. These controls are accessible through the programmable registers.

Each DMA controller has 16 internal registers for programmability and control. These registers include: Base Address, Base Word Count, Current Address, Current Word Count, Command Register, Mode Register, and Status Register. See "Register Description" for a complete list of registers and their functions.

DMA Operation

During normal operation of the IMP82C206, the DMA subsystem will be in one of the following conditions: Idle, Program, or Active.

Idle State (SI) is the default condition. In the SI condition, the DMA controller will be executing cycles consisting of only one state. As the default, this condition is applicable until the device is initialized and a DMA request is active.

When a DMA request becomes active, the device enters the Active condition and a Hold Request (HRQ) is issued to the System. Once Hold Acknowledge (HLDA) becomes active, the IMP82C206 generates the necessary memory addresses and command signals to accomplish transfers. Memory-to-I/O and I/O-to-Memory transfers occur in one cycle; Memory-to-Memory transfers require two cycles. During transfers between memory and I/O, data is presented on the system bus by either memory or the requesting device and completed in one cycle. Memory-to-Memory transfers, however, require the DMA to store data from the read operation in an internal register. The contents of this register is then written to memory on the subsequent cycle.

Idle Condition

The DMA is in an Idle condition when there is no service request pending for a device. While in SI, the DREQ input pins are sampled each clock cycle. Also, to determine if the CPU is attempting to access the internal registers, the internal select and HLDA are also sampled every clock cycle. (Since a CPU cycle is already in effect, the Program condition has priority over the Active condition.) The DMA exits the Idle condition when the status changes.

Program Condition

The Program condition can be entered whenever HLDA is inactive and an internal register is being accessed. The two DMA controllers use different addresses to select the internal registers. For DMA1, address lines XA0-XA3 are used and for DMA2, address lines XA1-XA4 are used. Table 2.1 lists the register address assignments.

Whenever HLDA has been inactive for one DMA clock cycle, the IMP82C206 will enable the Programming condition. It is the responsibility of the System to ensure that programming and HLDA are mutually exclusive. To prevent an attempt to service a device with a partially programmed channel, the channel should be masked or the DMA disabled. If a request for service occurs on an unmasked channel, which is being programmed, erratic operation of the IMP82C206 may occur.

An internal Byte Pointer flip-flop is used to supplement the addressing of the word count and address registers. With the flip-flop cleared, a read or write of a word count or address register will access that register's high byte. The Byte Pointer Flip-Flop will be toggled for any read/write of a word count or address register and will be cleared by a hardware RESET or Master Clear command. Commands are also provided to directly set or reset the flip-flop.

The DMA subsystem supports special commands to control the device while in the Program condition. They are derived from a set of addresses and the read or write strobes ($\overline{XIOW}$ or $\overline{XIOR}$). These commands are:

- —Master Clear
- —Clear Mask Register
- —Clear Mode Register Counter
- —Set Byte Pointer Flip-Flop
- —Clear Byte Pointer Flip-Flop

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Address Operation					
Register Function	**DMA1**	**DMA2**	**$\overline{XIOR}$**	**$\overline{XIOW}$**	**Flip-Flop**
Read Channel 0 Current Address Low Byte	000H	0C0H	0	1	0
Read Channel 0 Current Address High Byte			0	1	1
Write Channel 0 Base and Current Address Low Byte			1	0	0
Write Channel 0 Base and Current Address High Byte			1	0	1
Read Channel 0 Current Word Count Low Byte	001H	0C2H	0	1	0
Read Channel 0 Current Word Count High Byte			0	1	1
Write Channel 0 Base and Current Word Count Low Byte			1	0	0
Write Channel 0 Base and Current Word Count High Byte			1	0	1
Read Channel 1 Current Address Low Byte	002H	0C4H	0	1	0
Read Channel 1 Current Address High Byte			0	1	1
Write Channel 1 Base and Current Address Low Byte			1	0	0
Write Channel 1 Base and Current Address High Byte			1	0	1
Read Channel 1 Current Word Count Low Byte	003H	0C6H	0	1	0
Read Channel 1 Current Word Count High Byte			0	1	1
Write Channel 1 Base and Current Word Count Low Byte			1	0	0
Write Channel 1 Base and Current Word Count High Byte			1	0	1
Read Channel 2 Current Address Low Byte	004H	0C8H	0	1	0
Read Channel 2 Current Address High Byte			0	1	1
Write Channel 2 Base and Current Address Low Byte			1	0	0
Write Channel 2 Base and Current Address High Byte			1	0	1
Read Channel 2 Current Word Count Low Byte	005H	0CAH	0	1	0
Read Channel 2 Current Word Count High Byte			0	1	1
Write Channel 2 Base and Current Word Count Low Byte			1	0	0
Write Channel 2 Base and Current Word Count High Byte			1	0	1
Read Channel 3 Current Address Low Byte	006H	0CCH	0	1	0
Read Channel 3 Current Address High Byte			0	1	1
Write Channel 3 Base and Current Address Low Byte			1	0	0
Write Channel 3 Base and Current Address High Byte			1	0	1
Read Channel 3 Current Word Count Low Byte	007H	0CEH	0	1	0
Read Channel 3 Current Word Count High Byte			0	1	1
Write Channel 3 Base and Current Word Count Low Byte			1	0	0
Write Channel 3 Base and Current Word Count High Byte			1	0	1
Read Status Register	008H	0D0H	0	1	X
Write Command Register			1	0	X
Read DMA Request Register	009H	0D2H	0	1	X
Write DMA Request Register			1	0	X
Read Command Register	00AH	0D4H	0	1	X
Write Single Bit DMA Request Mask Register			1	0	X
Read Mode Register	00BH	0D6H	0	1	X
Write Mode Register			1	0	X
Set Byte Pointer Flip-Flop	00CH	0D8H	0	1	X
Clear Byte Pointer Flip-Flop			1	0	X
Read Temporary Register	00DH	0DAH	0	1	X
Master Clear			1	0	X
Clear Mode Register Counter	00EH	0DCH	0	1	X
Clear all DMA Request Mask Register Bits			1	0	X
Clear all DMA Request Mask Register Bits	00FH	0DEH	0	1	X
Write all DMA Request Mask Register Bits			1	0	X

Table 2.1 DMA Register Address Assignment

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IMP82C206 DMA

Active Condition

The IMP82C206 DMA subsystem enters the Active condition when one of the following conditions occur:

— Software request
— DMA request on an unmasked channel; device NOT in Program condition

The IMP82C206 will then begin a DMA transfer cycle.

A hold request is issued to the System after a DREQ request is received. When a Hold Acknowledge is returned, the DMA exits the Idle State and enters the Active Condition. In the Active Condition, memory address and command signals are generated to effect a Memory-to-I/O, I/O-to-Memory, or Memory-to-Memory transfer.

During transfers between memory and I/O, two commands are activated during the same cycle. In Memory-to-I/O transfers, $\overline{\text{DMAMEMR}}$ and $\overline{\text{XIOW}}$ are both asserted during the same cycle to transfer data directly from memory to the requesting device. (Note that IMP82C206 does not latch data from, nor drive data out, on this type of cycle.)

The number of clock cycles necessary to transfer data is varied. Control of the number of clock cycles required to transfer a word of data is dependent upon the peripheral device requirements and/or the DMA programming. During an Active cycle, the DMA will step through a series of states of one DMA clock cycle in length. The number of states in a cycle is dependent upon the type of cycle being performed and, again, how the DMA is programmed.

Memory and I/O data transfers require one cycle. Data is presented on the system bus by either the requesting device or memory. Memory-to-Memory transfers require two cycles as the data is stored from the read operation in an internal register. The contents of this register is then written to memory on the subsequent cycle.

An example of the series of steps necessary in an IMP82C206 read cycle are:

1. Receives a DREQ
2. Issues a HRQ
3. Waits for HLDA (remains in Idle condition)
4. DMA exits Idle condition at next clock cycle
5. Enters state S0
   a) Device resolves priority
   b) Issues DACK on the highest priority channel requesting service
6. Proceeds to state S1 where the multiplexed addresses are output and latched
7. State S2 is entered; $\overline{\text{DMAMEMR}}$ is asserted.
8. State S3 is entered; $\overline{\text{XIOW}}$ command is asserted. The IMP82C206 DMA remains in S3 until the Wait State Counter has decremented to zero and IOCHRDY is true. Note: At least one additional S3 will occur unless Compressed Timing is selected.
9. Ready condition is detected. The DMA enters S4 where both commands are deasserted.

Note: In Block and Demand Mode, subsequent cycles will begin in S2 unless the intermediate addresses require updating. In these subsequent cycles, the lower addresses are changed in S2.

The DMA can be programmed on a channel-by-channel basis to operate in one of four modes.

Cascade Mode

The Cascade mode is used for system expansion by cascading the DMA controllers. This mode determines the priority of the additional device. The master DMA controller does not generate address or control signals. The DREQ and DACK signals are used to interface the HRQ and HLDA signals of the slave DMA devices. This method preserves the priority chain and the new device must wait for a HLDA. After receiving the DREQ from a slave controller and the HLDA from the CPU, the master controller ignores all inputs, except HLDA and DREQ, on the active channel. This prevents conflicts between the DMA devices.

The Cascade mode is not limited to two levels of DMA controllers. Additional devices can be cascaded to the available channels in either DMA1 or DMA2. The Cascade mode interconnection for two levels of DMA devices is depicted in Figure 2.1.

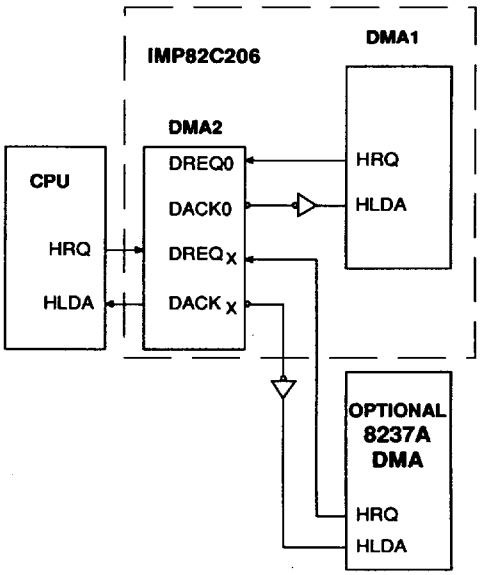

Figure 2.1 Cascade Mode Interconnect

To program cascaded controllers, the slave devices must be programmed first. Each successive device is then programmed. RESET sets the DACK outputs to become active low. The outputs are then placed in the active state. As there is an inversion between DACK0 of DMA2 and HLDA of DMA1, the DACK active low state should not be modified. Unwanted hold requests during the initialization process, generated by second level devices, are prevented by the first level device DMA request mask bit.

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Block Transfer Mode

In the Block Transfer mode, a DREQ or a software request is needed to begin the DMA transfer. The transfer continues until the terminal count (FFFFh) is attained. (DREQ is held active until DACK is asserted.) When the terminal count (T/C) is reached, the T/C is pulsed and the status register terminal count bit is set. If the automatic initialization option has been enabled, the channel will re-initialize itself. If automatic initialize is not enabled, the DMA will set the DMA request bit mask and suspend transferring on that channel.

Demand Transfer Mode

The Demand Transfer mode allows peripherals with limited buffering ability to control DMA transfers. The peripheral device will assert DREQ to begin a DMA transfer. When the peripheral's buffer is depleted, it will deassert DREQ and pass bus control back to the CPU. Later, when it's buffer has been filled again, it can reassert DREQ to start another transfer cycle.

In the Demand Transfer mode, transfers are initiated in response to the assertion of DREQ and continue until either T/C is reached or DREQ becomes inactive. Once DREQ has been deasserted, higher priority channels are allowed to intervene. A T/C pulse is generated, the terminal count bit in the status registers is reset, and auto-initialization, if enabled, is initiated upon reaching terminal count.

During idle periods between transfers, the CPU is released to operate and can monitor the operation by reading intermediate values from the address and Word Count Registers.

Single Transfer Mode

In Single Transfer mode, the DMA executes only one transfer cycle at a time. The DREQ is held active until the request is acknowledged (DACK goes active). Once the transfer is complete, HRQ is deasserted and the bus is released. After HLDA has gone inactive, the HRQ is asserted if another cycle is requested. If another cycle, on the same channel is requested, it is executed unless a request from a higher priority channel has been received. This insures that the CPU can execute at least one bus cycle between transfers.

After each transfer, the word count is decremented and the address is incremented or decremented. The terminal count bit in the status register is set and a T/C pulse is generated when the word count decrements from 0000h to FFFFh. If automatic initialization is not enabled, the DMA request bit mask is set and transfers on that channel are suspended; if enabled, the channel is re-initialized.

DMA Transfers

Multiple transfer types are provided in the IMP82C206 DMA subsystem. They are:

Memory-to-Memory Transfer

A block of memory may be moved from one location in memory to another location using the Memory-to-Memory transfer. By setting a bit in the Command Register, DMA Channel 0 and Channel 1 may be programmed to operate as Memory-to-Memory channels. If Channel 0 is programmed to maintain the same source address on every cycle, the CPU can initialize large blocks of memory with the same value. The DMA will continue performing transfer cycles until Channel 1 reaches terminal count.

After programming the DMA channels to operate as Memory-to-Memory channels, a transfer is initiated by generating a software or an external request to Channel 0. After the transfer is initiated, Channel 0 provides the address for the source block during the memory read portion of the cycle; Channel 1 generates the address for the memory write cycle. During the read cycle, a byte of data is latched in the internal Temporary Register. The contents of this register are then output on the XD0-XD7 data lines during the write portion of the cycle and, subsequently, written to memory. When Channel 1 reaches terminal count, transfer cycles are suspended.

Verify Transfer

The DMA operates as though a Read or Write Transfer is being performed. The HRQ, addresses, and DACK are generated but a command signal is not asserted. No actual transfer is performed; thus IOCHRDY is ignored in this cycle. Verify Transfer is a tool which is useful in diagnostics.

Read Transfer

Data is copied to an I/O device from memory. The memory address is generated and DMAMEMR and XIOW are asserted during the same cycle.

Write Transfer

Data is copied to memory from an I/O device. The memory address is generated and DMAMEMR and XIOR are asserted during the same cycle.

Auto-initialization

The auto-initialization process reloads the Base Address and Base Word Count Registers into the Current Address and Current Word Count Registers. The base registers may be altered by the CPU only. Thus, in active cycles, these registers remain unchanged.

Each of the four DMA channel Mode Registers contain a bit which enables auto-initialization on the channel after reaching terminal count. When automatic initialization has been programmed for a channel, the request mask bit is not set upon reaching terminal count. This feature provides the DMA with the ability to continue operation without CPU intervention.

To support full auto-initialization in Memory-to-Memory transfers, the Word Count Registers of Channel 0 and Channel 1 must be programmed with the same starting value. If Channel 0 reaches terminal count before Channel 1, Channel 0 reloads the starting address and word count and continues transferring data from the beginning of the source block. If Channel 1 reaches terminal count first, it reloads the current registers and Channel 0 will not be re-initialized.

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DREQ Priority

The IMP82C206 supports two methods of establishing DREQ priority. These are Fixed and Rotating priority.

Fixed priority is assigned priority based on channel position.

Rotating priority is based on the rotation assignment of the channels. The ordering of priority from Channel 0 to Channel 3 is maintained but the actual assignment of priority changes. The channel with the most recent DREQ performed is rotated and assigned the lowest priority; as the order of priority is fixed, the remaining three channels rotate accordingly. The rotating priority method is illustrated in Table 2.2.

In instances where multiple requests occur, the IMP82C206 will issue a HRQ but will not freeze the priority logic until HLDA is returned. Once HLDA becomes active, the priority is frozen. DACK is asserted on the highest priority requesting channel. Priority, for the next HRQ, is assigned when HLDA is released.

Address Generation

The number of pins required by the DMA subsystem are reduced by multiplexing eight intermediate bits of the address with the XD0-XD7 data bus. During state S1, the XD bus is used to output the eight bits of the memory address. For an 8-bit cycle, addresses A8-A15 are output; a 16-bit cycle addresses A9-A16 are output. An external TTL device must be provided with latch and enable signals for the external device.

During DMA1 cycles, the address bits are output as follows:

Lower 8-bits of address — XA0-XA7
Intermediate addresses A8-A15 - XD0-XD7
High 8-bits of address — XA16, A17-A23

ADSTB8 is asserted for one DMA clock cycle and the falling edge is used to latch the intermediate addresses A8-A15. AEN8 controls the output drivers of the external latch. The DMA Page Register generates A16-A23.

During DMA2 cycles, the address bits are output as follows:

Lower 8-bits of address — XA1-XA8
Intermediate addresses A9-A16 - XD0-XD7
High address — A17-A23

ADSTB16 and $\overline{\text{AEN16}}$ signals provide control for a separate latch. The DMA Page Register generates A17-A23. During 16-bit DMA transfers, XA0 and XA16 remain inactive.

The high order addresses are generated by the DMA Page Register during DMA cycles. The DMA Page Register consists of a set of 16 8-bit registers. Eight of the registers are used but sixteen are provided to maintain IBM PC/AT compatibility. Each DMA channel, excepting Channel 0 of DMA2, has a register with which it is associated. Channel 0 of DMA2 is used for internal cascading to DMA1. The assignment and address of each of these registers is shown in Table 2.3.

Multiple sequential transfers are generated during Demand and Block Transfers. Normally, the external address latches do not need to be relatched as the information is unchanged. When a carry or borrow from the lower 8-bits of the Address Counter occurs, the system updates the latch contents. As S1 cycles are executed only when necessary, the overall through-put performance is improved.

Register Function	Address
Unused	080H
8-bit DMA Channel 2 (DACK2)	081H
8-bit DMA Channel 3 (DACK3)	082H
8-bit DMA Channel 1 (DACK1)	083H
Unused	084H
Unused	085H
Unused	086H
8-bit DMA Channel 0 (DACK0)	087H
Unused	088H
16-bit DMA Channel 2 (DACK6)	089H
16-bit DMA Channel 3 (DACK7)	08AH
16-bit DMA Channel 1 (DACK5)	08BH
Unused	08CH
Unused	08DH
Unused	08EH
Refresh Cycle	08FH

Table 2.3 DMA Address Extension Register Map

First Arbitration	Second Arbitration	Third Arbitration	Priority
Channel 0	CHANNEL 2 - Cycle Grant	CHANNEL 3 - Cycle Grant	Highest
CHANNEL 1 - Cycle Grant	CHANNEL 3	Channel 0	
Channel 2	Channel 0	Channel 1	
Channel 3	Channel 1	Channel 2	Lowest
	CHANNEL X = Requested Channel		

Table 2.2 Rotating Priority Method

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Compressed Timing

The DMA subsystem can be programmed to compress the time to transfer a word in three clock cycles instead of four. A normal cycle consists of three states: S2, S3, and S4, State 3 is executed twice due to the one wait state insertion. To achieve greater through-put, the IMP82C206 may be programmed to assert both commands in S2, omitting one of the S3 cycles. Only one S3 cycle is executed, instead of two S3 cycles, and the transfer terminates in S4. The T/C is output in S1 in compressed timing. (Compressed timing is not valid for Memory-to-Memory transfers.) S1 cycles are executed to update the address latch, as needed.

Register Description

Current Address Register

Each DMA channel has a 16-bit Current Address Register. The address value used during transfers is held in this register. The channel can be programmed to increment or decrement this register when a transfer is completed. This register is read or written by the CPU in consecutive 8-bit bytes. Upon reaching terminal count in the Current Word Count Register, this register is reloaded from the Base Address Register if auto-initialization is selected. Channel 0 will not be incremented or decremented if the Address Hold Bit in the Command Register is set.

Current Word Count Register

The number of transfers to be performed is determined by the Current Word Count Register of each channel. After each transfer, the register is decremented until it goes from zero to FFFFh. When the register goes to FFFFh, the System generates a terminal count. At that time, the channel either auto-initializes or operation is suspended, and the appropriate Request Mask Bit is set. The number of transfers performed is one greater than the value programmed into the register.

Base Address Register

The Base Address Register stores the initial value of the Current Address Register for auto-initialization. It is a write only register and is loaded by the CPU when writing to the Current Address Register. When terminal count is reached and the auto-initialize bit is set, the contents of this register are loaded into the Current Address Register.

Base Word Count Register

The initial value of the Current Word Count Register is stored in the Base Word Count Register. It is a write only register and is loaded by the CPU when writing to the Current Word Count Register. During auto-initialization, this register is loaded into the Current Word Count Register.

Command Register

The Command Register controls the overall operation of the DMA subsystem. This register is programmed by the microprocessor in the Program Condition. It is cleared by RESET or the Master Clear command.

MSB LSB

B7	B6	B5	B4	B3	B2	B1	B0
DAK	DRQ	EW	RP	CT	CD	AH	M-M

DAK —DMA Acknowledge (DACK) active level is determined by bit 7.

0: Active low signal.
1: Active high signal.

DRQ —DMA Request for Service (DREQ) active level is determined by bit 6.

0: Active high signal.
1: Active low signal.

EW —Extended Write sets the write commands to be asserted one DMA cycle earlier during a transfer. When enabled, the read and write commands both begin in state S2.

0: Late write
1: Extended write
X: Bit 3 = 1 (Compressed Timing set active)

RP —Rotating Priority scheme for honoring DMA registers is determined by bit 4. The default condition is fixed priority.

0: Fixed priority (default)
1: Rotating priority

CT —Compressed Timing is determined by bit 3 of this register.

0: Normal timing (default)
1: Compressed timing
X: Bit 0 = 1 (Memory-to-Memory enabled)

CD —Controller Disable is the master disable for the DMA controller. This function disables the DMA subsystem (DMA1 or DMA2) when the CPU needs to reprogram one of the channels to prevent DMA cycles from occurring.

0: Controller enable
1: Controller disable

AH —The Address Hold feature is enabled for performing Memory-to-Memory transfers.

0: Address Hold enable
1: Address Hold disable
X: Bit 0 = 0 (Memory-to-Memory disabled)

M-M —Memory-to-Memory transfers enables Channel 0 and Channel 1 to be used.

0: Memory-to-Memory disabled
1: Memory-to-Memory enabled

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Mode Register

Each DMA channel has a Mode Register associated with it. Each of these registers reside at the same I/O address. The Write Mode Register command determines which channel's mode register is to be written and the mode of the selected channel. The mode register for each channel can be read by sequentially reading the Mode Register address. The CPU can restart the mode read process, at a known point, by using the Clear Mode Register Counter command. During write operations, bits 0 and 1 determine the channel mode register to be written. During mode read operations, bits 0 and 1 will both be 1.

MSB LSB

B7	B6	B5	B4	B3	B2	B1	B0
M1	M0	DEC	AI	TT1	TT0	CS1	CS0

(Write Operation)

M1-M0 —Mode selection for each channel is accomplished by bits 6 and 7.

00: Demand Mode select
01: Single Cycle Mode select
10: Block Mode select
11: Cascade Mode select

DEC —The direction of the address counter is determined by bit 5.

0: Increment address select
1: Decrement address select

AI —The Auto-initialization function is set by bit 4.

0: Auto-initialization disabled
1: Auto-initialization enabled

TT1-TT0 —The Type of Transfer to be performed is controlled by bits 2 and 3.

00: Verify Transfer
01: Write Transfer
10: Read Transfer
11: Illegal
XX: Bits 6 and 7 = 11 (Cascade mode selected)

CS1-CS0 —Channel Select bits 1 and 0 determine which channel's Mode Register will be written. Read back of a mode register will result in bit 1 and bit 0 both being 1.

00: Channel 0 Select
01: Channel 1 Select
10: Channel 2 Select
11: Channel 3 Select

Request Register

The Request Register is used to generate software requests. DMA service can be requested by DREQ or under software control. The request bits are non-maskable and subject to prioritization by the Priority Encoder network. Request Register bits can be set or reset independently by the CPU. All four bits are read in one operation and appear in the lower four bits of the byte. Bits 4 through 7 are read as ones. All four request bits are cleared to zero by RESET.

MSB LSB

B7	B6	B5	B4	B3	B2	B1	B0
X	X	X	X	X	RB	RS1	RS0

(Write Operation)

RB —The Request Bit indicates a software request.

0: Request Bit reset
1: Request Bit set

RS1-RS0 —Channel Select 0 and 1 determine which channel's Mode Register will be written. Read back of a mode register will result in bit 0 and bit 1 both being 1.

00: Channel 0 Select
01: Channel 1 Select
10: Channel 2 Select
11: Channel 3 Select

Format for the Request Register read operation is shown below.

MSB LSB

B7	B6	B5	B4	B3	B2	B1	B0
1	1	1	1	RC3	RC2	RC1	RC0

(Read Operation)

RC3-RC0 —During a Request Register read, the state of the request bit associated with each channel is returned in bit 0 through bit 3 of the byte. The bit position corresponds to the channel number.

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IMP82C206 DMA

Request Mask Register

The Request Mask register is a set of four bits. These bits are used to program the register to disable external DMA requests from generating transfer cycles.

This register can be programmed in two ways: Write Single Mask Bit or Write/Read All Mask Bits.

Each channel can be independently masked by writing to the Write Single Mask Bit location. The data format for this operation follows.

MSB LSB

B7	B6	B5	B4	B3	B2	B1	B0
X	X	X	X	X	MB	MS1	MS0

(Set/Reset Operation)

MB —The request Mask Bit determines if the channel is available for external requests. If the channel is unavailable, external requests are inhibited.

0: Clear Mask Bit
1: Set Mask Bit

MS1-MS0 —These two bits select the Specific Mask bit which is to be set or reset by the Mask Bit.

00: Channel 0 Select
01: Channel 1 Select
10: Channel 2 Select
11: Channel 3 Select

By writing to the Write All Mask Bits address, all four mask bits can be programmed in one operation.

The data format for the Write All and the Read All Mask Bits function follows.

MSB LSB

B7	B6	B5	B4	B3	B2	B1	B0
X	X	X	X	MB3	MB2	MB1	MB0

(Read/Write Operation)

MB3-MB0 —Each bit position in the field represents the Mask Bit of a channel. The Mask Bit number corresponds to the channel number associated with the mask bit.

All mask bits are set following a RESET or a Master Clear command. The Request Mask Register can be cleared, enabling all four channels, by performing a Clear Mask Register operation. If auto-initialize is disabled, individual channel mask bits are set as a result of terminal count being reached.

Status Register

MSB LSB

B7	B6	B5	B4	B3	B2	B1	B0
DREQ3	DREQ2	DREQ1	DREQ0	TC3	TC2	TC1	TC0

(Read Operation)

By reading the Status Register, the status of all four channels can be checked to determine if a channel has reached terminal count and whether an external service request is pending. The channel number corresponds to the bit position. Each time a T/C is reached by a channel, bits 0-3 are set. Bits 4-7 are not affected by the state of the Mask Register Bits. Bits 0-3 are cleared by RESET, Master Clear, or when a Status Read occurs.

Temporary Register

The Temporary Register is loaded from XD0-XD7 during the first cycle of a Memory-to-Memory transfer. During the second cycle of the transfer, the data is output to the XD0-XD7 pins. Data from the last Memory-to-Memory transfer remains until a RESET or Master Clear command occurs.

Special Commands

Special commands are provided to simplify programming the device. These commands are activated as a result of a specific address and assertion of either a XIOR or XIOW. Information on the data lines is ignored by the IMP82C206 for special commands.

Clear Byte Pointer Flip-Flop

This command initializes the flip-flop to point to the low byte of the register allowing the CPU to read or write the register bytes in correct sequence. This command is normally executed prior to reading or writing to the address or word count registers.

Set Byte Pointer Flip-Flop

This command allows the CPU to adjust the pointer to the high byte of an address or word count register.

Master Clear

This command clears the Command Register, Status Register, Request Register, Temporary Register, Mode Register Counter, and Byte Pointer Flip-Flop; the Request Mask Register is set. This command has the same effect as a hardware RESET. The Master Clear or RESET command resets the DMA to the Idle Condition.

Clear Request Mask Register

This command clears the mask bits in the register for all DMA channels enabling the channels to accept requests.

Clear Mode Register Counter

To allow access to four Mode Registers while only using one address, an additional counter is used. After clearing the counter, this command allows all four of the Mode Registers to be read by doing successive reads to the Read Mode Register address. The order in which the registers will be read is Channel 0 first, Channel 3 last.

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IMP82C206 INTERRUPT

IMP82C206 — Interrupt Controller

Functional Description

The IMP82C206 includes two Intel 8259A compatible interrupt controllers which may be cascaded to provide 16 interrupt levels. They function as a system interrupt manager with the following functions:

- — Issue CPU interrupt requests
- — Provide a vector, which the CPU uses as an index, to determine which interrupt service routine to execute
- — Priority resolution on pending interrupts and in service interrupts
- — Accept requests from peripherals

The interrupt subsystem can be restructured, based on the system environment, during system operation. Priority assignment modes, which can be reconfigured at any time, provide this capability.

Table 3.1 shows the interrupt level assignments for these two controllers, referred to as INTC1 and INTC2. The CS1 and CS2 signals are chip selects generated by the top level logic within the IMP82C206. Address bit XA0 is used, in combination with these chip selects, to access INTC1 at I/O ports 20H and 21H or INTC2 at ports A0H and A1H.

Controller	Channel	Interrupt Source
INTC1	IR0	OUT0 from counter/timer
INTC1	IR1	IRQ1 input pin
INTC1	IR2	INTR output from INTC2
INTC1	IR3	IRQ3 input pin
INTC1	IR4	IRQ4 input pin
INTC1	IR5	IRQ5 input pin
INTC1	IR6	IRQ6 input pin
INTC1	IR7	IRQ7 input pin
INTC2	IR0	IRQ from real time clock
INTC2	IR1	IRQ9 input pin
INTC2	IR2	IRQ10 input pin
INTC2	IR3	IRQ11 input pin
INTC2	IR4	IRQ12 input pin
INTC2	IR5	IRQ13 input pin
INTC2	IR6	IRQ14 input pin
INTC2	IR7	IRQ15 input pin

Table 3.1 IMP82C206 Interrupt Level Assignmens for Controllers

Note that the INTR output from INTC2 is connected to the IR2 input of the INTC1 to cascade the two controllers. The controllers are identical in function, although INTC1 must be programmed as the master and INTC2 as the slave. Figure 3.1 shows the interconnections between INTC1 and INTC2 within the IMP82C206.

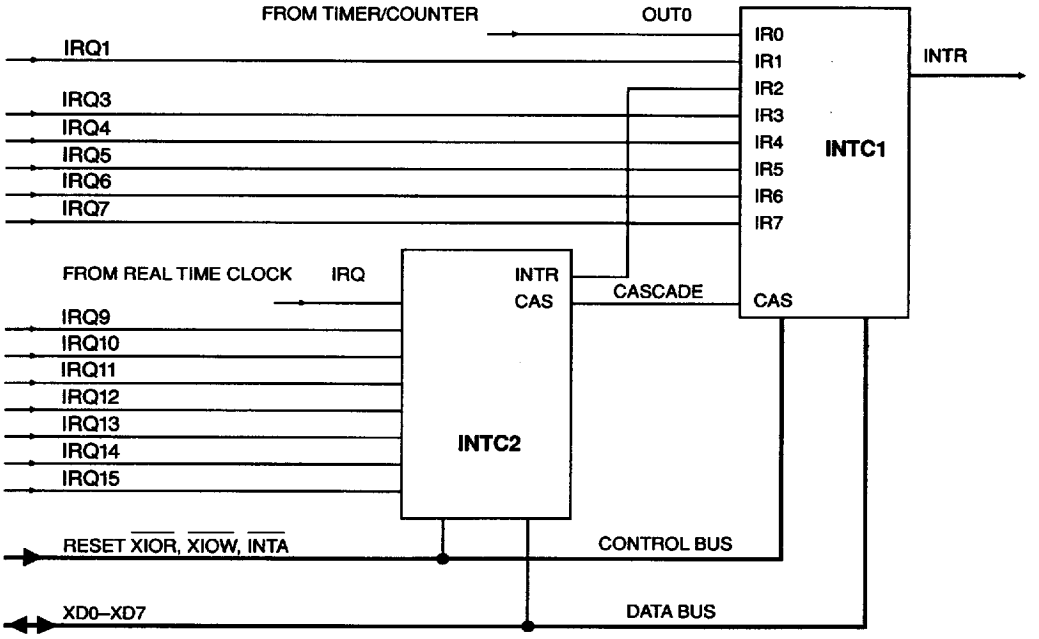

Figure 3.1 Internal Cascade Interconnect

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IMP82C206 INTERRUPT

The following sections provide a detailed description of the interrupt controller. Since the two controllers are functionally identical, information is provided for only one controller. The I/O ports are specified for INTC1 with the corresponding INTC2 ports specified in parenthesis. Example: 20H (A0H)

Operation

Interrupt Sequence

The purpose of the interrupt controller is to accept interrupt requests from peripheral devices, resolve priority, and supply an interrupt flag to the CPU. The CPU responds with two interrupt acknowledge cycles, during which the interrupt controller will supply a vector enabling the CPU to jump to the appropriate service routine.

The major elements within the interrupt controller and their functions are:

Interrupt Register (IR) — holds the state of each interrupt request line.

In-Service Register (IS) — contains the value of all interrupt channels that are currently being serviced.

Mask Register — contains the value of interrupt channels that are currently disabled.

Priority Resolver — evaluates active interrupt channels to determine if an interrupt request should be issued to the CPU. This section is also used to set the appropriate bit in the IS register during the interrupt acknowledge sequence.

Control Logic Section — includes a state machine controlling access to initialization and operation control registers.

The following section describes the events that occur during an interrupt sequence.

1. One or more interrupt request lines go active, setting the corresponding IR bits in the INTERRUPT REGISTER (IR).
2. Priority is resolved based on programmed priority information combined with the state of the INTERRUPT, IN-SERVICE (IS), and MASK registers. If a valid interrupt is determined, the INTR output is asserted.
3. The CPU responds to INTR with the first of two interrupt acknowledge cycles. The leading edge of the first $\overline{\text{INTA}}$ pulse will freeze the state of the IR register, and the priority resolver will determine the interrupt level to be serviced. The trailing edge of the $\overline{\text{INTA}}$ pulse will cause the appropriate IS bit to be set, and the corresponding IR bit to be reset. The current state of all other IR bits will remain frozen until the trailing edge of the second $\overline{\text{INTA}}$ pulse. If the controller is programmed as a master, and the current interrupt is from the slave, the CASCADE output goes active.
4. The second $\overline{\text{INTA}}$ pulse causes the appropriate interrupt vector (V7-V0) to be enabled onto the data bus (XD7-XD0). Bits V7-V3 of the vector are programmed using Initialization Command Word 2 (ICW2), bits V2-V0 correspond to the interrupt level being acknowledged. If the CASCADE signal is active, the slave controller will provide the vector; otherwise, the master will provide the vector. If no interrupt is active, a level 7 interrupt will be indicated by bits V2-V0 of the vector, indicating that a spurious interrupt has occurred.
5. If automatic end-of-interrupt (AEOI) is enabled, the IS bit will be reset at the trailing edge of the $\overline{\text{INTA}}$ pulse; otherwise, the IS bit will remain set until reset by writing Operation Command Word 2 (OCW2).

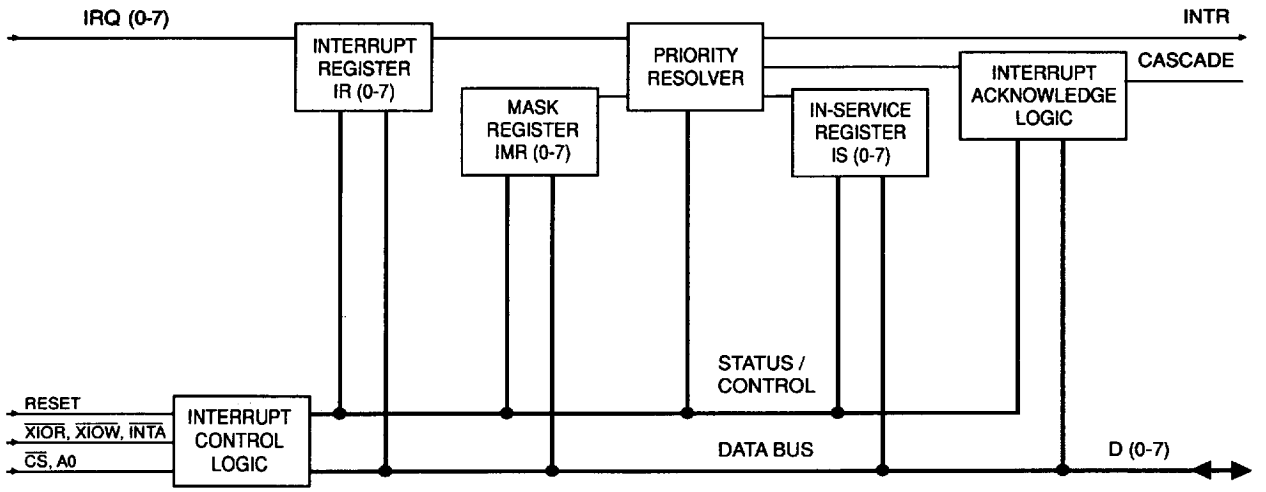

Figure 3.2 Interrupt Controller Block Diagram

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IMP82C206 INTERRUPT

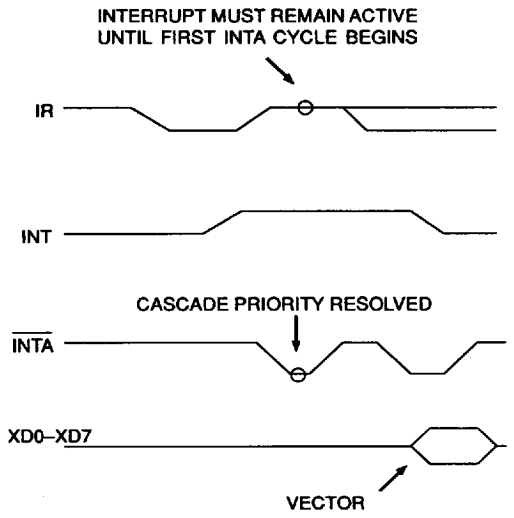

Figure 3.3 Interrupt Sequence

End-of-Interrupt

Resetting a bit in the In-Service Register is designated by an end-of-interrupt (EOI). The interrupt controller supports the following types of EOI:

1. Specific EOI
   A specific IS bit may be reset by writing the appropriate value to Operation Command Word 2 (OCW2). The IS bit to be reset is specified using bits L2-L0 of OCW2. The specific EOI command is selected using bits Specific Level (SL) and EOI of OCW2.
2. Non-specific EOI
   If a non-specific EOI is selected using bits SL and EOI of OCW2, the interrupt controller will reset the IS bit of the highest priority interrupt currently in-service. An IS bit that is masked during Special Mask Mode will not be reset.
3. Automatic EOI (AEOI)
   Automatic EOI mode is enabled by the AEOI bit of Initialization Command Word 4 (OCW4). If enabled, the IS bit will be reset automatically at the trailing edge of the second $\overline{INTA}$ pulse during the interrupt acknowledge sequence.

Priority Assignment

The interrupt controller supports fully nested interrupts with automatic and software controlled priority assignments. Following reset, the priority assignments are as shown below:

	Lowest Priority \							/ Highest Priority
Interrupt level:	7	6	5	4	3	2	1	0

These assignments may be modified by writing the appropriate value to Operation Command Word 2 (OCW2). The options available are:

1. Specific Rotation
2. Rotate on EOI
3. Rotate on AEOI

Specific Rotation

For Specific Rotation, a value is written to OCW2 to indicate the new lowest priority interrupt. Table 3.2 shows the priority assignments produced by executing a specific rotate command with the lowest priority interrupt defined by bits L2-L0 of OCW2.

Value			Priority Assignments							
L2	L1	L0	Low	/	/	/	/	/	/	High
0	0	0	0	7	6	5	4	3	2	1
0	0	1	1	0	7	6	5	4	3	2
0	1	0	2	1	0	7	6	5	4	3
0	1	1	3	2	1	0	7	6	5	4
1	0	0	4	3	2	1	0	7	6	5
1	0	1	5	4	3	2	1	0	7	6
1	1	0	6	5	4	3	2	1	0	7
1	1	1	7	6	5	4	3	2	1	0

Table 3.2 IMP82C206 Interrupt Level Assignments

Rotate on EOI

Rotate on end-of-interrupt is used in applications that require arbitration between a number of equal priority peripherals. In this mode, after an interrupt is serviced, it is assigned lowest priority. This method guarantees that all peripherals will be serviced at least once within eight interrupt requests to the CPU. Rotation on EOI is accomplished by writing the appropriate value to OCW2. Refer to the Software Description Section for detailed bit definitions. The following example illustrates the effect of the rotate on EOI command.

	Lowest Priority \							/ Highest Priority
Before Rotation:	5	4	3	2	1	0	7	6
After Rotation:	6	5	4	3	2	1	0	7

Rotate on AEOI

Rotate on AEOI performs the same function as rotation EOI, except that the rotation is triggered by an automatic end-of-interrupt and does not require a OCW2 write for each rotation. This mode may be set or reset by writing to OCW2.

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The Interrupt Controller contains a state machine to control the initialization sequence. The sequence is started by writing a one to bit 4 or Initialization Command Word 1 (ICW1) at I/O port 20H (AOH). This command starts the initialization process. The following is the sequence of events that occur during initialization:

1. Initialization Command Word Counter is set to zero
2. ICW1 is latched into the controller
3. Highest priority is set to level 0
4. Special mask mode is disabled
5. Slave mode address is set to 7
6. Interrupt register is enabled for status reads
7. Mask register is reset
8. Multiple interrupts are enabled
9. Automatic rotation is disabled

After these events occur, the remainder of the initialization sequence consists of multiple writes to port 21H (A1H) to initialize registers ICW2-ICW4. Figure 3.4 is a diagram showing the initialization sequence as controlled by the internal state machine. This sequence may be aborted by writing a zero to bit 4 of ICW1.

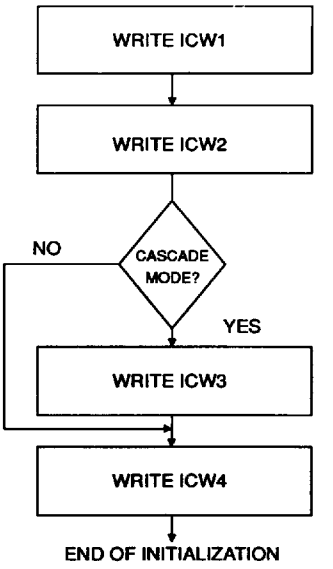

Figure 3.4 Initialization Sequence

Software Description

Configuration Register Summary

WR ONLY = Write Only Register
RD ONLY = Read Only Register
RD/WR = Read/Write Register
* = Don't Care

REGISTER NAME	TYPE	I/O PORT	BIT DEFINITIONS 7	6	5	4	3	2	1	0
ICW1	WR ONLY	20H (A0H)	*	*	*	SI	LTM	*	SM	*
ICW2	WR ONLY	21H (A1H)	V7	V6	V5	V4	V3	*	*	*
ICW3	WR ONLY	21H	S7	S6	S5	S4	S3	S2	S1	S0
		A1H	0	0	0	0	0	ID2	ID1	ID0
ICW4	WR ONLY	21H (A1H)	*	*	*	EMI	*	*	AEOI	*
OCW1	RD/WR	21H (A1H)	M7	M6	M5	M4	M3	M2	M1	M0
OCW2	WR ONLY	20H (A0H)	R	SL	EOI	SI	2/3	L2	L1	L0
OCW3	WR ONLY	20H (A0H)	0	ESSM	SMM	SI	2/3	PM	RR	RIS
IR	RD ONLY	20H (A0H)	IR7	IR6	IR5	IR4	IR3	IR2	IR1	IR0
IS	RD ONLY	20H (A0H)	IS7	IS6	IS5	IS4	IS3	IS2	IS1	IS0

TABLE 3.3 Functions of IMP82C206 Configuration Registers

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Detailed Configuration Register Definitions:

ICW1 : I/O Port 20H (A0H)

SI : Initialization select
- 0 : OCW2/3 selected
- 1 : ICW1 selected

LTM : Level trigger enable
- 0 : Edge triggered interrupts enabled (Default)
- 1 : Level triggered interrupts enabled

SM : Single Mode
- 0 : Cascade mode enabled (Default)
- 1 : Single mode enabled. NOTE: This mode NOT recommended for IMP82C206 operation

ICW2 : I/O Port 21H (A1H)

V7-V3 : Interrupt Vector bits 7-3

ICW3 : I/O Port 21H (INTC1)

S7-S0 : Selects which IR input of INTC1 is sourced by the INTR output of INTC2 for cascade mode. For proper initialization, this register should be initialized with the value 04H, indicating that the slave is present at IR level 2.

I/O Port A1H (INTC2)

ID2-0 : Slave identification for INTC2. For proper initialization, this register should be initialized with the value 02H, indicating the slave is present at IR level 2.

ICW4 : I/O Port 21H (A1H)

EMI :
- 0 : Disable multiple interrupts (Default)
- 1 : Enable multiple interrupts
  This mode allows INTC2 to fully nest interrupts in cascade mode. Since INTC2 is a slave connected to channel 2 of INTC1, IS bit 2 of INTC1 will be set whenever an INTC2 interrupt is being serviced. By enabling multiple interrupts, INTC1 will ignore the state of IS bit 2, and allow additional level 2 interrupts from the INTC2.

AEOI :
- 0 : Automatic end of interrupt disabled (Default)
- 1 : Automatic end of interrupt enabled

OCW1 : I/O Port 21H (A1H)

M7-M0 : Interrupt mask bits 7-0
- 0 : Corresponding IR input not masked (Default)
- 1 : Corresponding IR input masked

OCW2 : I/O Port 20H (A0H)

R : Rotate enable
SL : Specific level
EOI : End of interrupt enable

R	SL	EOI	Function
0	0	0	Disable rotate on AEOI (Default)
0	0	1	Non-specific EOI
0	1	0	No operation
0	1	1	Specific EOI
1	0	0	Enable rotate on AEOI
1	0	1	Rotate on non-specific EOI
1	1	0	Specific rotate
1	1	1	Rotate on specific EOI

SI : Initialization select
- 0 : OCW2/3 selected
- 1 : ICW1 selected

2/3 : Operation Command word 2/3 select
- 0 : OCW2 selected
- 1 : OCW3 selected

L2-L0 : Interrupt level select for specific rotate and EOI commands

OCW3 : I/O Port 20H (A0H)

ESMM : Enable special mask set/reset

SMM : Special mask mode
This mode is used to enable processing of interrupts while a higher priority interrupt is in-service. After an interrupt is acknowledged, lower level interrupts may be enabled by setting the bit in the mask register corresponding to the interrupt in-service. For example, IR0 is acknowledged causing IS0 to be set. If IR1 is of lower priority, it would normally be blocked by IS0. If SMM is enabled, mask bit 0 may be set, thus allowing IR1 to generate an INTR and be acknowledged.

ESSM	SMM	Operation
0	0	No operation (Default)
0	1	No operation
1	0	Special mask mode disabled
1	1	Special mask mode enabled

SI : Initialization select
- 0 : OCW2/3 selected
- 1 : ICW1 selected

2/3 : Operation Command word 2/3 select
- 0 : OCW2 selected
- 1 : OCW3 selected

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PM : Poll mode enable
0 : No operation (Default)
1 : Poll mode enabled
The poll sequence is initiated by writing a one to the PM bit. This will perform the equivalent of the first $\overline{INTA}$ pulse of an interrupt acknowledge cycle. The state of the IR register will be frozen, and the priority resolver will determine if an interrupt is pending. The next read from address 20H (A0H) is designated a poll read and performs the equivalent of the second $\overline{INTA}$ pulse. The interrupt controller will place the following byte onto the data bus.

D7	D6	D5	D4	D3	D2	D1	D0
IP	*	*	*	*	V2	V1	V0

IP : A one indicates that an interrupt is pending

V2-V0 : If IP is a one, then V2-V0 will correspond to the interrupt that is pending. If an IP is a one, the appropriate IS bit will be set and the corresponding IR bit reset. At the completion of the poll read, the IR register will be unfrozen.

RR : Register read enable
Enables status read from IS or IR registers, as selected by RIS. This bit is reset if PM is enabled.

RIS : In-Service register read enable
0 : Select IR status read (Default)
1 : Select IS status read

IMP82C206 TIMING DIAGRAMS

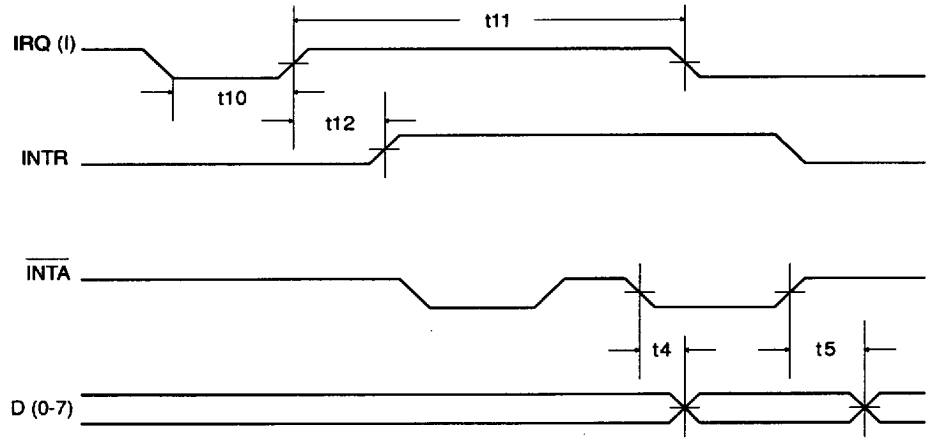

Figure 3.5 Interrupt Acknowledge Cycle

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IMP82C206 Real Time Clock

Functional Description

The Real Time Clock (RTC) of the IMP82C206 provides a source of time and date information to the system including a time-of-day clock with alarm, one hundred year calendar, and a programmable periodic interrupt. Through the use of battery backup for the clock and static RAM, this information is protected in the event of power off situations. 128 bytes of RAM are provided in the RTC: 14 bytes are used for clock and control functions; 114 bytes are used for general purpose storage e.g. system configuration information. The RTC can also be used as an additional source of periodic interrupts to the CPU.

The Real Time Clock (RTC) circuit consists of four functional blocks. They are:

1. Address decode
2. Control/status registers, the Time/date registers, and the general purpose RAM
3. Clock divider circuit and the Periodic interrupt selector
4. Update logic and miscellaneous glue logic

Address Decode

The first block contains the address decode which enables the system to read and write the internal registers and RAM of the RTC. Addressing the contents of the RTC is a two step process. First, a pointer value (00-7F) is placed on the lower seven bits of the data bus and then latched internally with the falling edge of the AS signal. In the PC/AT environment, the AS signal is generated by an I/O write to address 070H. The second step of the process, an I/O read or write to address 071H, uses the previously latched pointer value to access the desired storage location. The address map for the RTC is shown in Table 4.1.

FUNCTION	INDEX
Seconds	00
Seconds Alarm	01
Minutes	02
Minutes Alarm	03
Hours	04
Hours Alarm	05
Day of Week	06
Date of Month	07
Month	08
Year	09
Register A	0A
Register B	0B
Register C	0C
Register D	0D
User RAM	0E
User RAM	0F
.	
.	
.	
User RAM	7E
User RAM	7F

Table 4.1 Address Map for Real Time Clock

Control/Status Registers

The control/status registers, the time/date registers, and the general purpose RAM can be read by the CPU; however, some of the registers can not be written, and some are inaccessible to the CPU during certain periods of time. These restrictions will be identified on a register by register basis in the "Register Configuration" section.

Clock Divider Circuit and the Periodic Interrupt Selector

The third block of the RTC consists of the clock divider circuit and the periodic interrupt selector. The RTC can use one of three input frequencies to generate the 1 Hz internal clock. These include 4.194304 MHz, 1.048576 MHz, or 32.768 KHz; however, to prolong battery life, it is suggested that the slower, 32.768 KHz frequency be used. The DV2-DV0 bits of Register A are programmed to match the selection of input frequency thereby enabling the appropriate number of stages in the divide chain to yield the desired 1 Hz output. All along the chain, taps are made available to the periodic interrupt selector. The RS3-RS0 bits can be programmed to select 1 of the 15 possible taps.

Update Logic and Miscellaneous Glue Logic

The fourth block contains the update logic and miscellaneous glue logic. An update cycle occurs once a second and is responsible for updating the time and calendar information. The alarm registers are compared to the time registers during the update and, if a match occurs, the AF bit is set and an interrupt may be generated. At the end of the update cycle, the UF bit is set and an interrupt may be generated. The duration of the update cycle varies depending on the input frequency used. If 4.194304 MHz or 1.048576 MHz is used, the cycle lasts 248 μs, but, if 32.768 KHz is used, the cycle lasts 1948 μs. In all cases, the UIP bit will go high 244 μs prior to the start of the update cycle and return low at the end of the cycle. The UIP bit is most often used to avoid contention between the CPU and RTC updates. One method is to read the UIP bit and, if it is zero, perform the read or write operation to one of the ten time/date registers. At least 244 μs is available to complete the read or write. If UIP is one, the update is about to begin or is already in progress and the read or write should be postponed until UIP is zero.

Another way to avoid the update cycle is to use the update ended interrupt or poll the UF bit. When the UF bit goes high at the end of an update, the CPU has until the start of the next update to complete a read or write. If UIE is high, the update ended interrupt will occur when UF goes high. This frees the CPU from polling UF, but still allows, until the start of the next update, a read or write to be performed.

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Register Configurations

Time and Date Registers

The IMP82C206 has a total of 10 time/date registers. They hold the following information: seconds, seconds alarm, minutes, minutes alarm, hours, hours alarm, day, date, month, and year. The addresses of these registers range from 0H-9H respectively. All of these registers are read/write with one exception: The MSB of the seconds register is read only and is always zero. During the update cycle, the registers are switched off the data bus. If the software attempts to write a register during this time, the contents will not be altered. If a read is attempted, the results will be undefined.

The seconds and minutes registers can be loaded with values ranging from 00-59 (BCD) or 00H-3BH (binary). The hours register can contain values of 01-12 and 81-92 (BCD) or 01H-0CH and 81H-8CH (binary) when 12 hour mode is selected. The AM/PM designation is made by the presence (PM) or absence (AM) of the MSB in the hours register. In 24 hour mode, the values can range from 0-23 (BCD) or 00H-17H (binary).

The Alarm registers for seconds, minutes, and hours contain the same range of values as their non-alarm counterparts. In addition to providing an interrupt at a specific time, the alarm registers can be programmed to provide a periodic interrupt. If the two upper bits in an alarm register are set high, the register becomes a 'don't care' in the comparisons. As an example, if the hours and minutes alarm registers both contained 'don't care' values (C0H-FFH), then an alarm interrupt would occur every minute.

Registers for the day, date, month, and year are also provided. The days register contains the day of the week information. Values may range from 01-07 in BCD or binary where one is Sunday. The date register contains values that range from 01-31 (BCD) or 01H-1FH (binary). Automatic end of month recognition is provided. Values representing the month of the year are stored in the months register. They fall in the range of 01-12 (BCD) or 01H-0CH (binary). The years register contains values that range from 00-99 (BCD) or 00H-63H (binary). Automatic leap year detection is provided.

Register Function	Index Register Address	BCD Range	Binary Range
Seconds	0	00-59	00H-3BH
Seconds Alarm	1	00-59	00H-3BH
Minutes	2	00-59	00H-3BH
Minutes Alarm	3	00-59	00H-3BH
Hours (12 hour mode) Hours (24 hour mode)	4	01-12 (AM) 81-92 (PM) 00-23	01H-0CH 81H-8CH 00H-17H
Hours Alarm (12 hour mode) Hours Alarm (24 hour mode)	5	01-12 (AM) 81-92 (PM) 00-23	01H-0CH 81H-8CH 00H-17H
Day of Week	6	01-07	01H-07H
Day of Month	7	01-31	01H-1FH
Month	8	01-12	01H-0CH
Year	9	00-99	00H-63H

Table 4.2 Time, Calendar, and Alarm Data Format

Control and Status Registers

The status of the Real Time Clock is monitored and operations controlled by four registers. These registers are accessible by the CPU at all times. Their Index Address is 0AH-0DH.

Register A (0AH)

Register A is read/write with the exception of bit 7, the update in progress (UIP) bit, which is read only.

MSB LSB

B7	B6	B5	B4	B3	B2	B1	B0
UIP	DV2	DV1	DV0	RS3	RS2	RS1	RS0

(Read/Write Register except UIP)

UIP —The Update In Progress flag is a status bit the CPU monitors which indicates if an update cycle is in progress. If it is high, an update cycle is in progress or about to start. UIP goes active 244 μs prior to the start of the update cycle and remains active for the duration of the update. If the bit is low, an update cycle is not in progress and will not be for at least 244 μs. The bit is not altered by RESET; however, when the SET bit in Register B goes high, UIP goes low.

0: Update not in progress
1: Update in progress

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DV2-DV0 — The Divider Control bits are programmed to select the proper divider for the time base used to provide a 1 Hz output. They can also be programmed to reset the divider chain. When reset is removed from the divider chain, the first update cycle will begin 1/2 second later. This facilitates more accurate setting of the time. Bit combinations not shown are reserved for test purposes. These bits are not altered by RESET.

000: 4.194304 MHz
001: 1.048576 MHz
010: 32.768 KHz
11X: Reset

RS3-RS0 — These four bits control the selection of a particular frequency of Periodic Interrupt. The Periodic Interrupt is derived from the Divider chain and is separate from the Alarm Interrupt. It provides rates greater than the one second rate supplied by the Alarm Interrupt. Both the alarm and periodic interrupts do, however, use the same interrupt channel in the Interrupt Controller. Table 4.3 shows the rates that may be selected. These bits are not altered by RESET.

RS3	RS2	RS1	RS0	4.194304 or 1.048576 MHz	32.768 KHz
0	0	0	0	None	None
0	0	0	1	30.517 µs	3.90625 ms
0	0	1	0	61.053 µs	7.8125 ms
0	0	1	1	122.070 µs	122.070 µs
0	1	0	0	244.141 µs	244.141 µs
0	1	0	1	488.281 µs	488.281 µs
0	1	1	0	976.562 µs	976.562 µs
0	1	1	1	1.953125 ms	1.953125 ms
1	0	0	0	3.90625 ms	3.90625 ms
1	0	0	1	7.8125 ms	7.8125 ms
1	0	1	0	15.625 ms	15.625 ms
1	0	1	1	31.25 ms	31.25 ms
1	1	0	0	62.5 ms	62.5 ms
1	1	0	1	125 ms	125 ms
1	1	1	0	250 ms	250 ms
1	1	1	1	500 ms	500 ms

Table 4.3 Periodic Interrupt Rate

Register B (0BH)

Register B is a read/write register.

MSB LSB

B7	B6	B5	B4	B3	B2	B1	B0
SET	PIE	AIE	UIE	0	TDF	24/12	DSE

(Read/Write Register)

SET — The SET bit enables or disables update cycles. When high, it aborts current update cycles and inhibits future update cycles. When it is low, updates function normally. This bit allows the time and date to be set without update cycle interference. It is not altered by RESET.

0: Update cycle enabled
1: Update cycle disabled

PIE — The Periodic Interrupt is enabled when this bit is high. When it is low, the interrupt will not be seen on the INTR line; however, it will continue to occur at the rate that is determined by the RS3-RS0 bits in Register A. The Periodic Interrupt Flag (PF) bit in Register C is not affected by the state of the PIE bit. PIE goes low when $\overline{\text{PSRSTB}}$ is asserted.

0: Periodic interrupt disabled
1: Periodic interrupt enabled

AIE — The Alarm Interrupt is enabled when this bit is high. When it is low, the alarm interrupt will not be seen on the INTR line; however, the Alarm Flag (AF) bit in Register C will continue to be set when a match between the time bytes and the alarm bytes is detected. AIE goes low when $\overline{\text{PSRSTB}}$ is asserted.

0: Periodic interrupt disabled
1: Periodic interrupt enabled

UIE — The Update Ended Interrupt is enabled when this bit is high. This interrupt occurs at the end of each update cycle and can be used to avoid the update cycle when reading or writing the time bytes. If UIE is low, the update interrupt will not be seen on the INTR line; however, the Update Ended Interrupt Flag (UF) bit in Register C will continue to be set at the completion of an update. UIE goes low when $\overline{\text{PSRSTB}}$ is asserted.

0: Periodic interrupt disabled
1: Periodic interrupt enabled

Bit 3 is unused in the IMP82C206.

TDF — The Time/Date Format bit is programmed by the user to select binary or Binary Coded Decimal (BCD) representations of the time/date information. If the TDF bit is high, binary is selected. If it's low, BCD is selected. If this bit is changed, the time and date information may need to be changed as well. TDF is unaffected by $\overline{\text{PSRSTB}}$ or RESET.

0: BCD representation enabled
1: Binary representation enabled

24/12 — The 24/12 bit is programmed by the user to select either 24 hour or 12 hour mode for the hour and hour alarm bytes. If the bit is high, then 24 hour mode is used. If it is low, then 12 hour mode is used. If the mode is changed, the hours and hours alarm bytes may need to be changed as well. The 24/12 bit is not altered by $\overline{\text{PSRSTB}}$ or RESET.

0: Twelve hour mode enabled
1: Twenty-four hour mode enabled

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DSE —The Daylight Savings Time bit is programmed by the user to enable or disable Daylight Savings Time. If the bit is high, two updates will be made: On the last Sunday in April, the time bytes will change from 1:59:59 AM to 3:00:00 AM; on the last Sunday in October, the time bytes will change from 1:59:59 AM to 1:00:00 AM. If DSE is low, then these special updates do not occur. DSE is not altered by PSRSTB or RESET.

0: Daylight Savings Time disabled
1: Daylight Savings Time enabled

Register C (0CH)

Register C is a read only register.

MSB LSB

B7	B6	B5	B4	B3	B2	B1	B0
IRQF	PF	AF	UF	0	0	0	0

(Read Only Register)

IRQF —The Interrupt Request Flag bit is a flag which indicates the occurrence of any RTC interrupt. It will be high when one or more of the following is true: PF = PIE = 1, AF = AIE = 1, and/or UF = UIE = 1. When IRQF goes high, it causes the INTR line to go high. IRQF goes low after Register C is read. It also goes low when PSRSTB is asserted. It is not altered by RESET.

0: No Interrupt
1: RTC Interrupt occurrence

PF —The Periodic Interrupt Flag is a flag which indicates the occurrence of a periodic interrupt. It goes high upon the occurrence of a periodic interrupt from the divider chain, regardless of the state of the PIE bit.It goes low after a read of Register C or when PSRSTB is asserted. It is not altered by RESET.

0: No Periodic interrupt
1: Periodic Interrupt occurrence

AF —The Alarm Register Flag is a bit which goes high when the current time matches the time set in the alarm registers. It does this regardless of the state of the AIE bit. It goes low after Register C is read or when PSRSTB is asserted. It is not altered by RESET.

0: No Alarm occurrence
1: Alarm occurrence

UF —The Update Cycle Flag bit goes high when the update cycle finishes, regardless of the state of the UIE bit. It goes low after a read of Register C or when PSRSTB is asserted. It is not altered by RESET.

0: Update Cycle not complete
1: Update Cycle complete

Bits 3-0 are unused in the IMP82C206 and, when read, will be low.

Register D (0DH)

Register D is a read only register.

MSB LSB

B7	B6	B5	B4	B3	B2	B1	B0
VRT	0	0	0	0	0	0	0

(Read Only Register)

VRT —The Valid RAM and Time bit is an indicator of valid RAM and time contents in the RTC. A read of Register D, showing VRT low, indicates that power has been lost to the IMP82C206 (PSRSTB went low), and that reinitialization is necessary. If VRT is high, and the data is intact. VRT will only be set high after a Register D read, if PSRSTB is high. It is not altered by RESET.

0: RTC RAM and Time to be initialized
1: Valid RAM and Time

Bits 6-0 are unused in the IMP82C206 and, when read, will be low.

Static RAM

There are 114 bytes of static RAM available in the RTC portion of the IMP82C206. This RAM may be addressed from 0EH-7FH. All of these bytes are read/write, unaffected by RTC functions, and available during the update cycle. Because the RAM is battery back-up, it is most often used for storing setup and configuration information.

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IMP82C206 — Counter/Timer

Functional Description

The Counter/Timer (CTC) is a programmable interval timer/counter. It is a general purpose, multi-timing element and can be treated as an array of I/O ports in the system software. It can be used to generate accurate time delays under software control by programming one of the counters for the desired delay. The CTC can also be programmed to interrupt the CPU after the set delay keeping software overhead minimal and allowing variable length delays.

The controls necessary to load, read, configure, and operate each counter are provided by the Control Logic. All three counters are driven from the common control logic. Six operating modes are available. These are:

Mode 0 Interrupt on terminal count
Mode 1 Hardware retriggerable one-shot
Mode 2 Rate generator
Mode 3 Square wave generator
Mode 4 Software triggered strobe
Mode 5 Hardware retriggerable strobe

All counters can be programmed and operated in any mode. Due to the absence of an external hardware trigger signal, Counter 0 and Counter 1 have limited capability in Mode 1 and Mode 5.

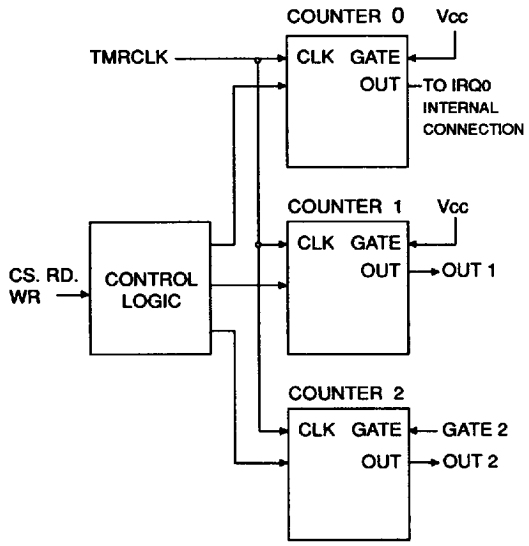

Figure 5.1 Counter/Timer Block Diagram

The use of each counter is as follows:

Counter 0 may be used as an interrupt to the system for timekeeping and task switching. Output (Out0) is connected to IRQ0 of Interrupt Controller 1. (For more information, see "Interrupt Controller Functional Description.")

Counter 1 may be programmed to generate pulse or square waves for use by external devices. In the PC/AT environment, this channel is used to generate memory refresh requests.

Counter 2 is a full function Counter/Timer. This channel can be used as an interval timer, a counter, or as a gated rate/pulse generator. In the PC/AT environment, this channel drives the speaker.

TMRCLK, a common clock input pin, is the driver for all three counters and operates independently from other clock inputs on the IMP82C206.

Counter Description

Each counter consists of a Control Register, a Status Register, a 16-bit Counting Element (CE), a pair of 8-bit Counter Input Latches (CIL, CIH), and a pair of 8-bit Counter Output Latches (COL, COH). Each counter has a clock input for loading and decrementing the CE, a mode defined GATE input for controlling the counter (only GATE2 is externally accessible), and an OUT signal (OUT0 is not externally accessible). The state and function of the OUT signal is controlled by the Counter Mode and condition of the CE (See "Counter Mode" definitions).

The Control Register, which controls the counter, is loaded by writing a byte to the Control Word address (043H). This control word command contains a pointer to the desired counter. The remaining bits in the command contain the mode, type of command, and count format information. This mode information is stored in the Control Register and used to control the counter.

The Status register provides the capability for the software to monitor counter conditions. It may also be used to read the contents of the Control Register e.g. programmed mode, current states of the OUT pins, and null count flag.

The Counting Element (CE), the actual counter, is a loadable 16-bit synchronous counter. The CE is loaded or decremented on the falling edge of TMRCLK. The maximum initial count for the CE is zero which is equivalent to 65536 in binary operation or 10000 in BCD. The CE is a descending counter. When the counter is decremented to zero, it wraps or is reloaded, depending upon the Mode. In Modes 2 and 3, the CE is reloaded; Modes 1, 4, and 5 wraps to FFFF in binary operation or 9999 in BCD.

The CE may be loaded or reloaded in one TMRCLK cycle using the Counter Input Latches. Depending on the counters read/write mode (MSB only, LSB only, or MSB and LSB), one or two bytes are written into the CI latches. These bytes are transferred to the counter as one 16-bit word whenever a load cycle is performed. If the counter read/write mode is MSB only or LSB only, the unused byte will be forced to zero.

Counter Output Latches are provided that allow the CE count to be captured and read later. This allows the current count to be read without affecting the counting in progress. The Latch Counter Command is used to perform this latching function on one or more counters. (See "Latch Counter Command.")

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Programming the CTC

Each counter must be programmed before it can be used. The Control Word Register, Status Register, Counting Element, and Output Latches of each counter are undefined until programmed. The counters are programmed by writing a Control Word followed by an initial count.

Address	Function
040H	Counter 0 Read/Write
041H	Counter 1 Read/Write
042H	Counter 2 Read/Write
043H	Control Register Write Only

Table 5.1 Counter/Timer Address Map

Register Configurations

Control Word (043H)

The Control Word address is used to program the operating mode of all three counters. The Control Word format selects the three types of control word commands: Mode Configuration, Read-Back, and Latch Counter. The Control Word is written to the Control Word Register associated with each counter. This register will be used by the counter to set the operating mode, counter read/write format, and counting format.

MSB LSB

B7	B6	B5	B4	B3	B2	B1	B0
F3	F2	F1	F0	M2	M1	M0	BCD

F3-F0: Bits 7-4 determine the counter and command to be performed.

SELECT COUNTER:

F3	F2	COMMAND
0	0	Select Counter 0
0	1	Select Counter 1
1	0	Select Counter 2
1	1	Read-Back Command (See "Read-Back Command" Section)

READ/WRITE OPERATIONS ONLY:

F1	F0	COMMAND
0	0	Counter Latch Command
0	1	Read/Write Least Significant Byte Only
1	0	Read/Write Most Significant Byte Only
1	1	Read/Write Least Significant Byte first, then Most Significant Byte

M2-M0: Bits 3-1 determine the counter's Mode during Counter Mode Configuration Commands.

M2	M1	M0	Function
0	0	0	Select Mode 0
0	0	1	Select Mode 1
X	1	0	Select Mode 2
X	1	1	Select Mode 3
1	1	0	Select Mode 4
1	1	1	Select Mode 5

BCD: Bit 0 selects the counting format to be used. Two formats are allowed: Binary or Binary Coded Decimal (BCD).

COUNTING FORMAT:

BCD	COMMAND
0	Binary Counter (16-bits)
1	BCD Counter (4 Decades)

Counter Mode Configuration Command

When writing to a counter, two conventions must be observed before the initial count is written: The counters Control Word must be entered and the Control Word format specified must be followed for the initial count i.e. Least Significant Byte (LSB) then Most Significant Byte (MSB).

The initial count may be changed at any time after programming. The Control Word need not be rewritten if the programmed format is used.

During Counter Mode Configuration Commands, M2-M0 are defined as follows:

MSB LSB

B7	B6	B5	B4	B3	B2	B1	B0
F3	F2	F1	F0	M2	M1	M0	BCD

M2-M0: Bits 3-1 determine the counter's Mode.

M2	M1	M0	Function
0	0	0	Select Mode 0
0	0	1	Select Mode 1
X	1	0	Select Mode 2
X	1	1	Select Mode 3
1	1	0	Select Mode 4
1	1	1	Select Mode 5

Latch Counter Command

When a Latch Counter Select Command is issued in the Control Word, the counter's output, COL and COH, latch the current state of the CE. COL and COH remain latched until read by the CPU, or the counter is reprogrammed. The output latches then return to a 'transparent' condition. In this condition, the latches are enabled and the content of the CE is read directly.

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MSB LSB

B7	B6	B5	B4	B3	B2	B1	B0
F3	F2	0	0	M2	M1	M0	BCD

F3-F2: Bits 7-6 determine the counter to be latched.

Command	F3	F2
Latch Counter 0	0	0
Latch Counter 1	0	1
Latch Counter 2	1	0
Read-Back Command	1	1

After the command is issued but before reading the first counter, Latch Counter Commands may be issued to multiple counters. However, if multiple commands are issued to the same counter, before reading the specified counter, only the first command will be accepted.

Read-Back Command

The Read-Back Command provides the ability to latch the count value or status of the selected counter(s). If the count was latched, the next one or two reads, depending on whether the counter is programmed to transfer one or two bytes, result in the count being returned. If the counter's status was latched, the next read from the counter will return the Counter Status. If both the count and status for a counter is latched, the status will be returned followed by the count.

MSB LSB

B7	B6	B5	B4	B3	B2	B1	B0
1	1	F1	F0	M2	M1	M0	BCD

F1 : Bit 5 selects the Latch Count. This enables the counter selected to latch the state of the CE in COL and COH.

0: Latch count enabled
1: Latch count disabled

F0 : Bit 4 selects the Latch Status. This enables the selected counter(s) to latch the current condition of it's Status Register. The next read of the Counter will result in the contents of the Status Register being read (see "Counter Status").

0: Latch Status enabled
1: Latch Status disabled

M2-M0: Bit 3 causes Counter 2 to latch one or both of the registers specified by Latch Count and Latch Status. The same is true for bit 2 and bit 1 except that they enable Counter 1 and Counter 0 respectively.

0: Latch registers specified by Latch Count and Latch Status
1: Latch disabled

Once a Read-Back Command has been performed, the counter's latched count value or status will remain until the counter is read or reprogrammed.

Table 5.2 lists examples of valid Read-Back commands.

Description/Results	B7	B6	B5	B4	B3	B2	B1	B0
Read back count and status of Counter 0. Result: Count and status latched for Counter 0.	1	1	0	0	0	0	1	0
Read back status of Counter 1. Result: Status latched for Counter 1.	1	1	1	0	0	1	0	0
Read back status of Counter 2 and Counter 1. Result: Status latched for Counter 2 but not Counter 1.	1	1	1	0	1	1	0	0
Read back count of Counter 2. Result: Count latched for Counter 2.	1	1	0	1	1	0	0	0
Read Back count and status of Counter 1. Result: Count latched for Counter 1 but not status.	1	1	0	0	0	1	0	0
Read back status of Counter 1. Result: Command ignored. status already latched for Counter 1.	1	1	1	0	0	0	1	0

Table 5.2 Example Read-Back Commands

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Counter Status

The Read-Back Command may be used to latch the Status Register of the selected counters.

MSB LSB

B7	B6	B5	B4	B3	B2	B1	B0
OUT	NC	F1	F0	M2	M1	M0	BCD

OUT : Bit 7 contains the state of the OUT signal of the counter.

NC : Bit 6 contains the condition of the Null Count Flag. This flag is used to indicate that the contents of the CE are valid.

0: Counter has been loaded from the CI registers
1: Counter has not been loaded from the CI registers

F1-F0 : Bits 5-4 contain the F1 and F0 Command bits which were written to the Command Register of the counter during initialization. This information is useful in determining whether the high byte, the low byte, or both must be transferred during counter read/write operations. (See "Control Word" Section.)

M2-M0: Bits 3-1 indicate the mode of the counter.

000: Mode 0 — Interrupt on terminal count
001: Mode 1 — Hardware retriggerable one-shot
X10: Mode 2 — Rate Generator
X11: Mode 3 — Square Wave generator
110: Mode 4 — Software triggered strobe
111: Mode 5 — Hardware triggered strobe

BCD : Bit 0 indicates the CE is operating in BCD format.

Counter Operation

All counters may be programmed in any of the six modes. However, due to the absence of an external hardware trigger, Counter 0 and Counter 1 have limited capability in Mode 1 and Mode 5.

The following modes are available.

Mode 0 — Interrupt on terminal count
Mode 1 — Hardware retriggerable one-shot
Mode 2 — Rate generator
Mode 3 — Square Wave generator
Mode 4 — Software triggered strobe
Mode 5 — Hardware triggered strobe

Mode 0 — Interrupt on Terminal Count

Mode 0 is typically used for event counting. When the Control Word is written, OUT2 goes low and remains low until the CE reaches zero. When zero is reached, OUT2 returns high and remains high until a new count or Control Word is written. Couting is enabled when GATE2 = 1. GATE2 has no effect on OUT2.

The CE is loaded with the first TMRCLK pulse (a rising edge followed by a falling edge of the IMP82C206 TRMCLK input) after the Control Word and initial count are loaded. If both CIL and CIH are written, the CE is loaded after CIH is written. This TMRCLK pulse does not decrement the count. For an initial count of N, OUT2 does not go high until N+1 TMRCLK pulses after initialization. Writing a new initial count to the counter reloads the CE on the next TMRCLK pulse and counting continues from the new count.

If an initial count is written with GATE2 = 0, it is loaded on the next TMRCLK pulse. Counting begins at GATE2 = 1. OUT2, therefore, goes high N TMRCLK pulses after GATE2 = 1.

Mode 1 — Hardware Retriggerable One-shot

Writing the Control Word causes OUT2 to go high initially. Once initialized, the counter is armed and a trigger, the rising edge of the GATE2 input, causes OUT2 to go low on the next TMRCLK pulse. OUT2 then remains low until the counter reaches zero. An initial count of N results in a one-shot pulse N TMRCLK cycles long.

Any subsequent triggers while OUT2 is low cause the CE to be reloaded, extending the length of the pulse until the new count expires. Writing a new count to CIL and CIH will not affect the current one-shot pulse N TMRCLK cycles long. GATE2 has no effect on OUT2.

Mode 2 — Rate Generator

Mode 2 is typically used to generate a Real Time Clock interrupt. It functions as a divide-by-N counter. Writing the Control Word during initialization sets OUT2 high.

When the initial count is decremented to 1, OUT2 goes low for one TMRCLK pulse. The following TMRCLK pulse returns OUT2 high, reloads the CE initial count, and the process is repeated. In Mode 2, the counter is periodic. The same counting sequence continues indefinitely and will generate an OUT2 pulse every N TMRCLK cycles. A count of one is invalid in Mode 2.

MODE	CONDITION		
	High	Rising	Low
0	Enables Counting	—	Disables Counting
1	—	a) Initiates Counting b) Reset Out Pin	—
2	Enables Counting	Initiates Counting	a) Disables Counting b) Forces Out Pin High
3	Enables Counting	Initiates Counting	a) Disables Counting b) Forces Out Pin High
4	Enables Counting	—	Disables Counting
5	—	Initiates Counting	—

Tables 5.3 GATE PIN FUNCTION

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GATE2 = 0 disables counting and forces OUT2 high immediately. A trigger reloads the CE with the initial count on the next TMRCLK pulse. Thus GATE2 can be used to synchronize the counter to external events.

Writing a new count, while counting, does not affect current operation unless a trigger is received. Otherwise, the new count will be loaded at the end of the current counting cycle.

Mode 3 — Square Wave Generator

Mode 3 is typically used for baud rate generation. It is similar to Mode 2 except for the duty cycle of OUT2. OUT2 is set high initially and remains high for the first half of the count. When the first half of the initial count expires, OUT2 goes low for the remainder of the count.

If the counter is loaded with an even count, the duty cycle of OUT2 will be 50% (high = low = N/2). For odd count values, OUT2 is high one TMRCLK cycle longer than it is low. Therefore, high = (N + 1)/2 and low = (N − 1)/2.

Mode 4 — Software Triggered Strobe

OUT2 goes high initially. Expiration of the initial count causes OUT2 to go low for one TMRCLK pulse. GATE2 = 0 disables counting but has no effect on OUT2. Also, a trigger will not reload the CE.

The counting sequence is started by writing the initial count. The CE is loaded on the TMRCLK pulse after initialization. The CE begins decrementing the count one TMRCLK pulse later. OUT2 will go low for one TMRCLK cycle, (N + 1) cycles after the initial count is written.

If a new initial count is written during a counting sequence, it is loaded into the CE on the next TMRCLK pulse and the sequence continues from the new count. This allows the sequence to be 'retriggered' by the software.

Mode 5 — Hardware Triggered Strobe

OUT2 goes high initially. Counting is started by a trigger. The expiration of the initial count causes OUT2 to go low for one TMRCLK cycle. GATE2 = 0 disables counting.

After writing the Control Word and initial count, the CE is loaded on the TMRCLK pulse after a trigger. Since loading the CE inhibits decrementing, OUT2 will go low for one TMRCLK cycle, (N + 1) TMRCLK cycles, after the trigger.

If a new count is written during a counting operation, the current counting sequence will not be affected unless a trigger occurs. A trigger causes the counter to be reloaded from CIL and CIH on the next TMRCLK pulse and counting continues from there.

Operation Common to All Modes

All Control Logic is reset when a Control Word is written to a Counter. OUT2 goes to a known initial state. TMRCLK pulses are not required.

GATE2	MODE
Level sensitive; sampled on rising edge of TMRCLK	0, 2, 3, 4
Rising-edge sensitive; rising edge sets an internal flip-flop whose output is sampled on the next rising edge of TMRCLK. The flip-flop resets immediately after being sampled.	1, 2, 3, 5
Gate input is edge and level sensitive.	2,3

Table 5.4 GATE2 Operation

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IMP82C206

IMP82C206 Absolute Maximum Ratings

PARAMETER	SYMBOL	MIN	MAX	UNITS
Supply Voltage	Vcc	–	7.0	V
Input Voltage	Vi	−0.5	5.5	V
Output Voltage	Vo	−0.5	5.5	V
Operating Temperature	Top	−25°	85°	C
Storage Temperature	Tstg	−40°	125°	C

Note: Permanent device damage may occur if Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions described under Operating Conditions.

IMP82C206 Operating Conditions

PARAMETER	SYMBOL	MIN	MAX	UNITS
Supply Voltage	Vcc	4.75	5.25	V
Ambient Temperature	Ta	0°	70°	C

IMP82C206 DC Characteristics

(Ta = 0°—70°C, Vcc = 5V + 5%)

PARAMETER	SYMBOL	MIN	MAX	UNITS	TEST CONDITIONS
Input Low Voltage	Vil	–0.4	0.4	V	—
Input High Voltage	Vih	3.6	Vcc + 0.5	V	—
Output Low Voltage	Vol	—	0.4	V	Iol = 2.0 mA
Output High Voltage	Voh	2.4	—	V	Iol = 2.0 mA
Input Current 0 < Vin < Vcc	Iol	–10	10	µA	Vin = Vcc to OV
Output Leakage Current	Iol	–10	10	µA	Vou = Vcc to 0.45
Vcc Supply Current	Icc	—	30	mA	CLK Freq = 8 MHz
Vcc Standby Supply Current	Iccsb	—	10	µA	CLK Freq = DC

IMP82C206 Capacitance

(Ta = 25°C, VCC = GND = OV)

PARAMETER	SYMBOL	MIN	MAX	UNITS	TEST CONDITIONS
Input Capacitance	Cin	—	10	pF	FC = 1 MHz
I/O Capacitance	Ci/o	—	20	pF	Unmeasured pins
Output Capacitance	Cout	—	20	pF	Returned to Vss

IMP82C206 AC Characteristics

(Ta = 0°C to 70°C, Vcc = 5V + 5%)

SYM	DESCRIPTION	6 MHz MIN	6 MHz MAX	8 MHz MIN	8 MHz MAX	UNITS
t1	Address setup to command active	25		25		nsec
t2	Command active period	250		200		nsec
t3	Address hold time from command inactive	0		0		nsec
t4	Data valid delay	200		160		nsec
t5	Data hold time from $\overline{XIOR}$ inactive	10		10		nsec
t6	XD0-XD7 active from $\overline{XIOR}$	5	40	5	40	nsec
t7	Data setup to $\overline{XIOW}$ inactive	200		160		nsec
t8	Data hold time from $\overline{XIOW}$ inactive	0		0		nsec
t9	Command recovery time	150		120		nsec
t10	Interrupt request width (low)	120		100		nsec
t11	Interrupt request width (high)	250		200		nsec
t12	INT output delay		400		300	nsec

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SYM	DESCRIPTION	6 MHz MIN	6 MHz MAX	8 MHz MIN	8 MHz MAX	UNITS
t15	Real time clock cycle time		500		500	nsec
t16	AS pulse width	200		160		nsec
t17	Data valid setup to AS inactive	200		160		nsec
t18	Data hold time from AS inactive	0		0		nsec
t19	OSCI period	500		500		nsec
t20	OSCI high time	200		200		nsec
t21	OSCI low time	200		200		nsec
t22	$\overline{\text{PSRSTB}}$ high delay from Vcc	5		5		µsec
t23	$\overline{\text{PSRSTB}}$ low pulse width	5		5		µsec
t24	VRT bit valid delay		2		2	µsec
t25	TMRCLK period	200	DC	125	DC	nsec
t26	TMRCLK low time	80		50		nsec
t27	TMRCLK high time	80		50		nsec
t28	GATE2 setup to TMRCLK	80		50		nsec
t29	GATE2 hold time from TMRCLK	80		50		nsec
t30	GATE2 low time	80		50		nsec
t31	GATE2 high time	80		50		nsec
t32	OUT2 delay from TMRCLK		200		120	nsec
t33	OUT2 delay from GATE2		200		120	nsec
t34	SCLK Period (1 × SCLK)	186		125		nsec
t34a	SCLK Period (2 × SCLK)	93		62		nsec
t35	SCLK low time (1 × SCLK)	75		43		nsec
t35a	SCLK low time (2 × SCLK)	32		22		nsec
t36	SCLK high tim (1 × SCLK)	82		55		nsec
t36a	SCLK high time (2 × SCLK)	40		27		nsec
t37	DREQx setup to SCLK	0		0		nsec
t38	HRQ valid from SCLK		120		75	nsec
t39	HLDA setup to SCLK	75		45		nsec
t40	$\overline{\text{AENx}}$ valid delay from SCLK		175		105	nsec
t41	$\overline{\text{AENx}}$ invalid delay from SCLK	TBD	130	TBD	80	nsec
t42	ADSTBx valid delay from SCLK		80		50	nsec
t43	ADSTBx invalid delay from SCLK		120		120	nsec
t44	XD0-XD7 active delay from SCLK		110		60	nsec
t45	XD0-XD7 valid setup to ADSTBx low	80		65		nsec
t46	XD0-XD7 hold time from ADSTBx low	25		25		nsec
t47	XD0-XD7 tristate delay from SCLK		170		135	nsec
t48	Address valid delay from SCLK	110		60	nsec	
t49	Address hold time from $\overline{\text{DMAMEMR}}$ high	66		50		nsec
t50	Address tristate delay from SCLK		90		55	nsec
t51	DACKx delay from SCLK		170		105	nsec
t52	Command enable delay from SCLK		150		90	nsec
t53	Command active delay from SCLK		190		120	nsec
t54	Write command inactive delay from SCLK		130		80	nsec
t55	Address hold time from write high	116		75		nsec
t56	Command tristate delay from SCLK		120		75	nsec
t57	Read command inactive delay from SCLK		190		115	nsec
t58	TC delay from SCLK		100		60	nsec
t59	XD0-XD7 setup to read command inactive	155		90		nsec
t60	XD0-XD7 hold from read command inactive	0		0		nsec
t61	XD0-XD7 valid delay from SCLK		190		120	nsec
t62	XD0-XD7 hold from write inactive	15		15		nsec
t63	IOCHRDY input setup to SCLK	50		35		nsec
t64	IOCHRDY input hold time from SCLK	35		20		nsec

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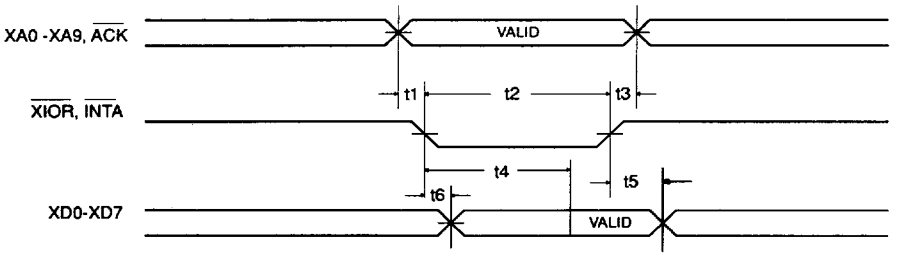
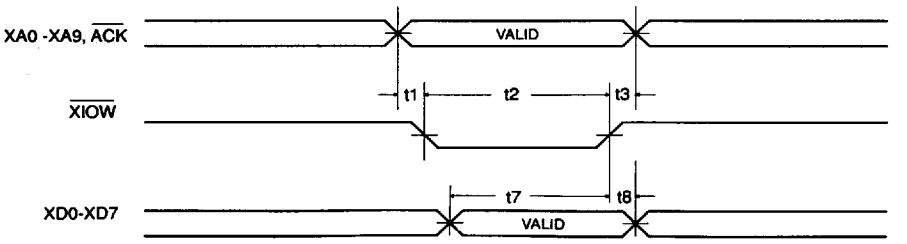
IMP82C206 TIMING DIAGRAMS

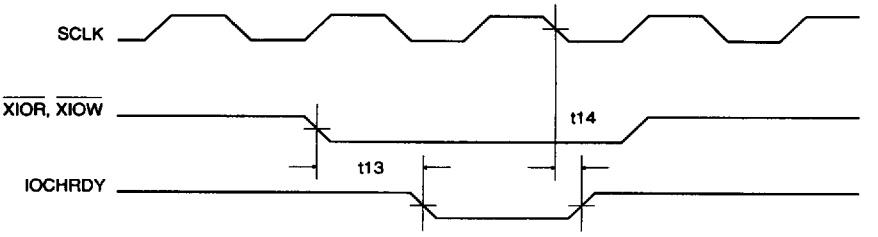


PERIPHERAL READ / INTA CYCLE

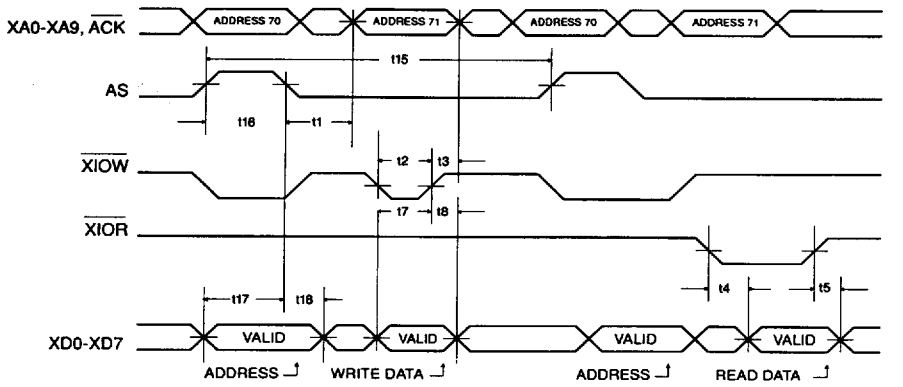


PERIPHERAL WRITE CYCLE

COMMAND RECOVERY



IOCHRDY OUTPUT



REAL TIME CLOCK ACCESS CYCLE

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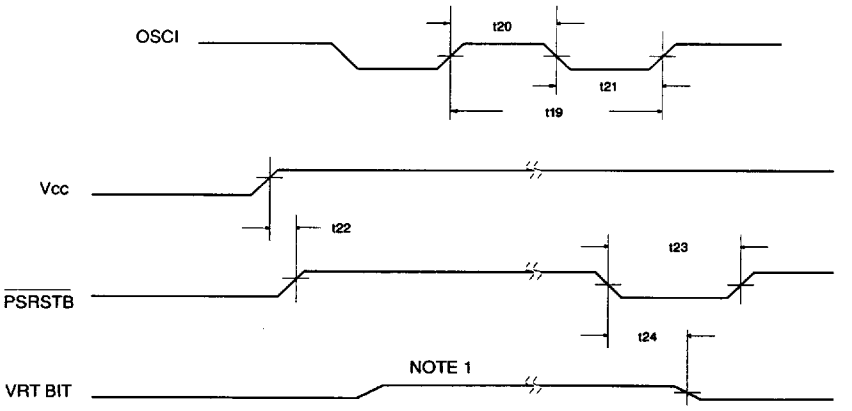
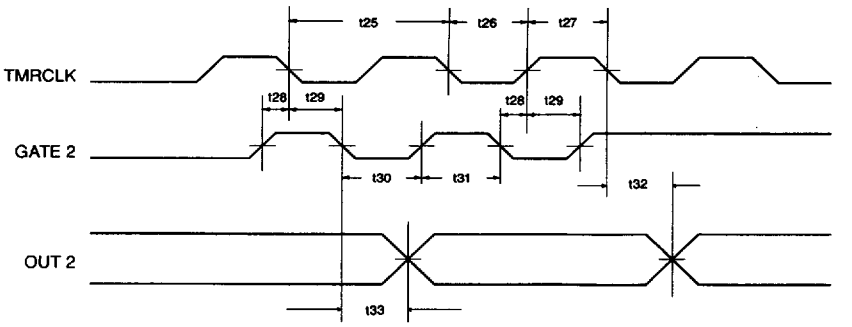
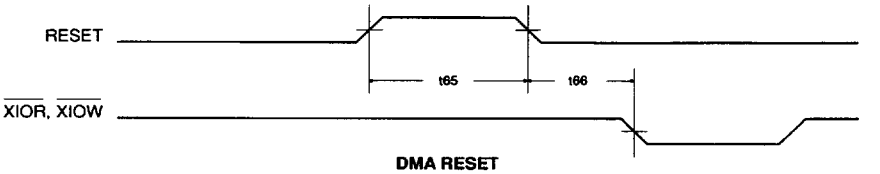
IMP82C206 TIMING DIAGRAMS



REAL TIME CLOCK POWER-UP SEQUENCE



COUNTER/TIMER PARAMETER



DMA RESET

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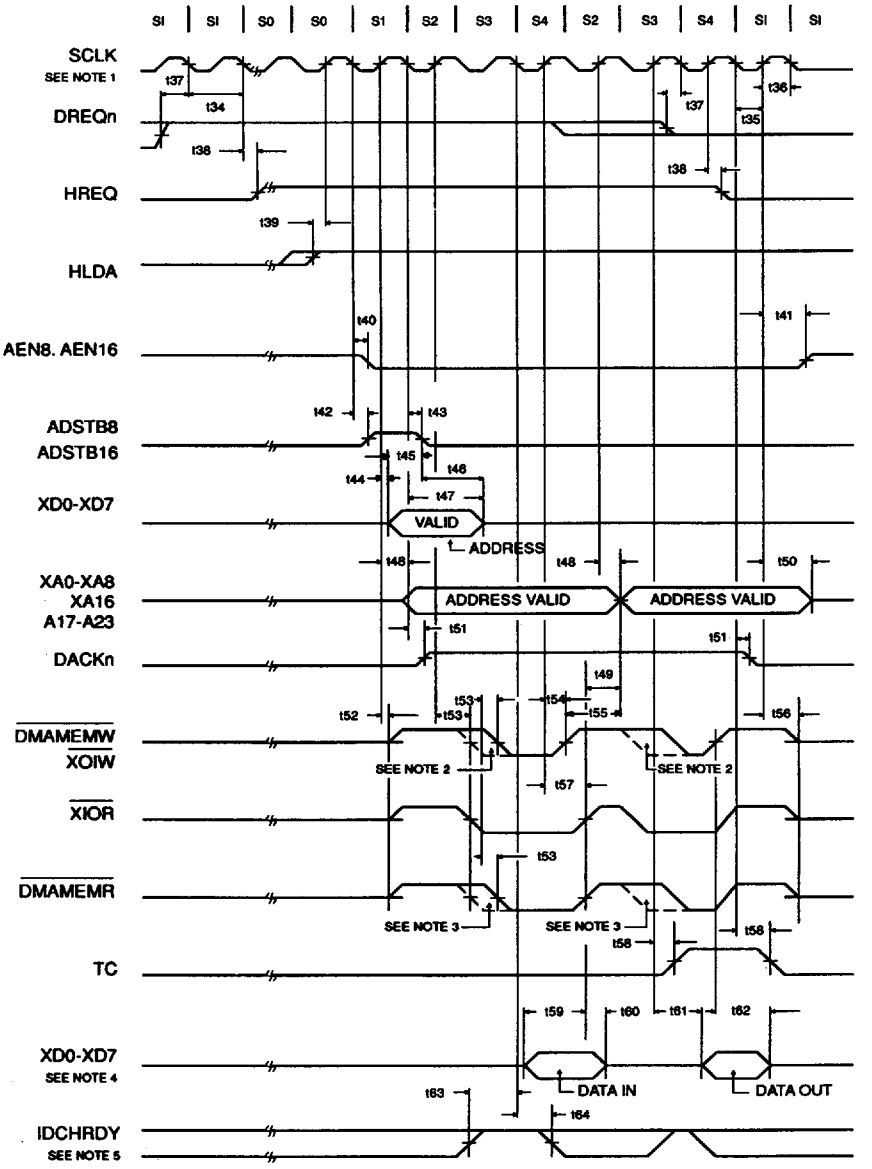
IMP82C206 TIMING DIAGRAMS



NOTE:

1. All timing reference to SCLK are independent of the state of the clock select bit in the configuration register. SCLK shown in this diagram is the undivided clock directly from the input
2. Extended Write mode selected
3. Extended Read mode selected
4. Data Bus during Memory-to-Memory Transfer
5. IOCHRDY Input Timing

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