Single Chip Bell 212A/CCITT V.22 Modem

GENERAL DESCRIPTION

The XR-2130 is a single chip modem which supplies the complete Bell 212A or CCITT V.22 function. The XR-2130 is designed to interface directly to the XR-2131 modem controller to form a complete smart modem, such as a Hayes compatible type.

The XR-2130 supplies the modulation and demodulation for 1200 BPS DPSK (212A/V.22) and 300 BPS FSK (212A). For 1200 BPS operation, advanced circuit techniques are utilized such as digital echo modulation for precise transmit carrier spectrum shaping and coherent Costas Loop type demodulator for excellent BER vs. S/N performance.

The XR-2130 is also very feature intensive, supporting virtually all the "smart modem" functions. These include call progress monitoring (CPM), DTMF dialing, and both analog and digital test facilities (ALB and DLB).

Fabricated in silicon gate CMOS, the XR-2130 offers low power operation from ±5 volt power supplies. The XR-2130 is available in a 28 pin plastic or ceramic DIP, or a range of surface mount packages.

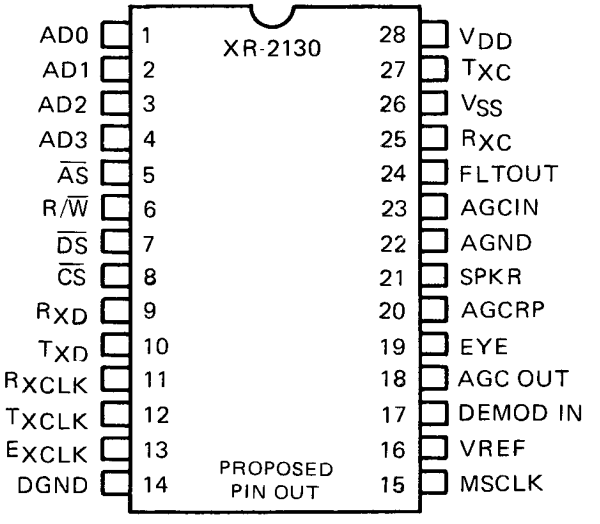
FEATURES

Bell 212A/CCITT V.22 Operation
1200 BPS DPSK/300 BPS FSK
Universal Microcontroller Interface
Costas Loop Coherent PSK Demodulator
Call Progress Monitoring
ALB and DLB Test Modes
DTMF Dialing
Voice Output Port
Hayes Type Software Available
(XR-2131 Modem Controller)
Low Power CMOS
Eye Pattern Output (Quality)

APPLICATIONS

Stand Alone Modem
Internal Modem
Smart Modem
Bell 212A Type Modem
CCITT V.22 Type Modem
Hayes Compatible Modem

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Power Supply	
V_{DD}	−0.3 to 7 V
V_{SS}	0.3 to −7 V
Input Voltage	V_{SS} −0.3 V to V_{DD} +0.3 V
DC Input Current	±10 mA
Power Dissipation	
(Package Limitation)	
Plastic DIP	750 mW
Ceramic DIP	1000 mW
Derate Above 25°C	
Plastic DIP	5 mW/°C
Ceramic DIP	7.5 mW/°C
Storage Temperature Range	−65°C to +150°C

ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-2130CN	Ceramic	0°C to 70°C
XR-2130CP	Plastic	0°C to 70°C

Consult factory for surface mount package ordering information.

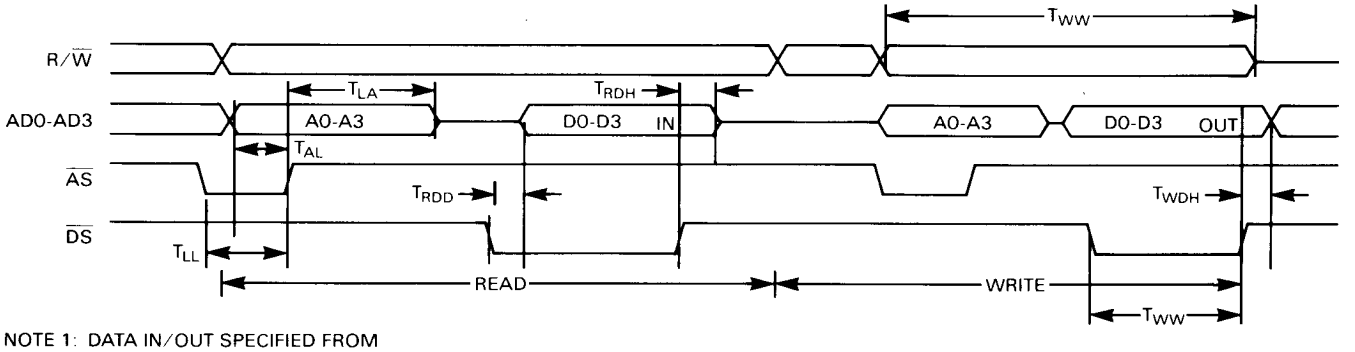
SYSTEM DESCRIPTION

The XR-2130, when connected to the XR-2131 or other suitable controller, forms a complete smart 212A/V.22 type modem. The XR-2130 has also been designed with a universal microcontroller interface so that other controllers may also be used.

ELECTRICAL CHARACTERISTICS

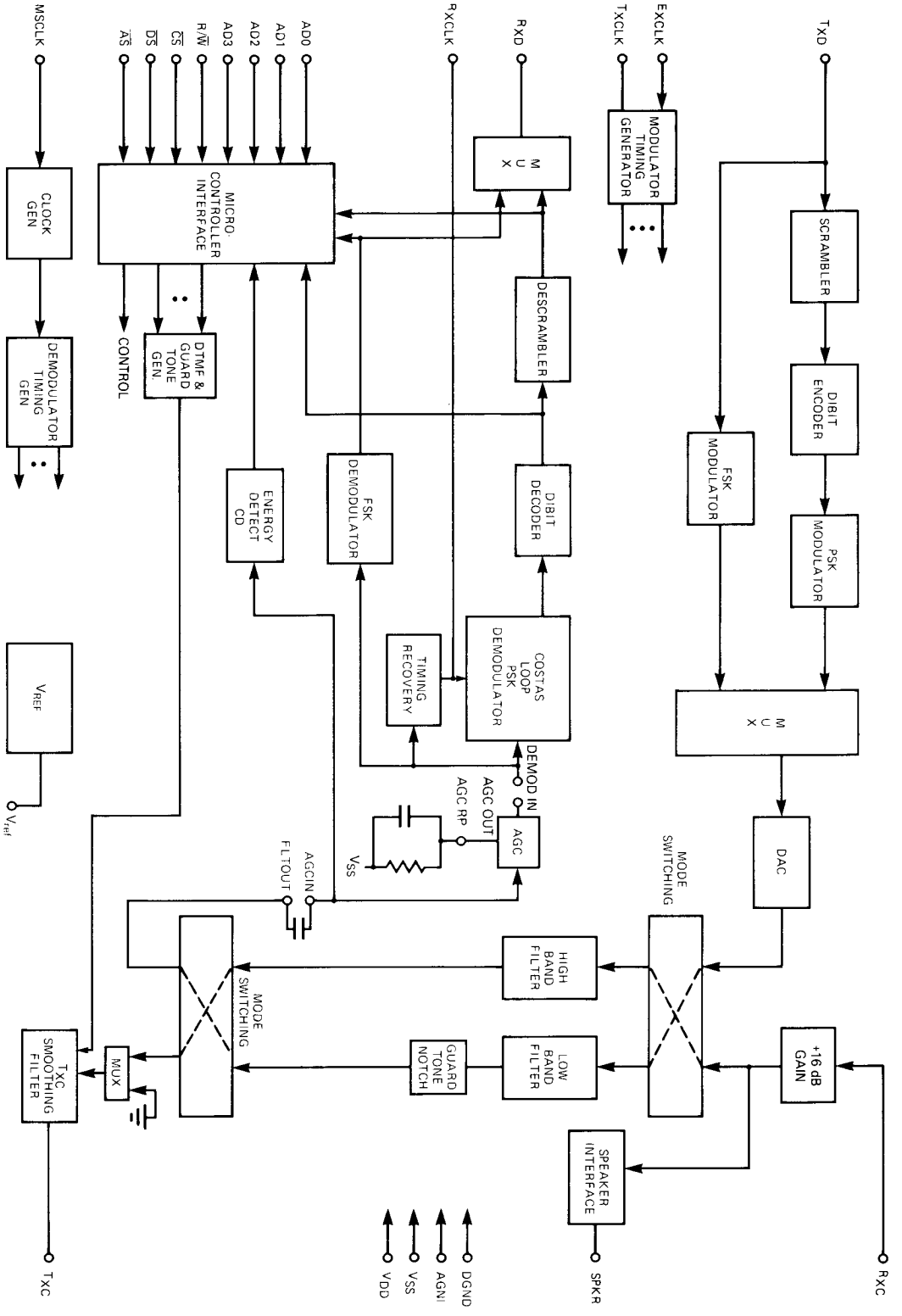
Test Conditions: V_{DD} = +5 V, V_{SS} = -5 V, MSCLK = 11.0592 MHz, T_A = +25°C, unless otherwise specified.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	CONDITION
V_{DD}	Positive Supply	4.75	5.0	5.25	V	
V_{SS}	Negative Supply	-5.25	-5.0	-4.75	V	
I_{DD}	Positive Supply Current		18		mA	
I_{SS}	Negative Supply Current		18		mA	
V_{IH}	Input High Voltage	2.0			V	
V_{IL}	Input Low Voltage			0.8	V	
V_{OH}	Output High Voltage	2.4			V	I_{OH} = 400 µA
V_{OL}	Output Low Voltage			0.4	V	I_{OL} = 1.6 mA
T_{AL}	Address Valid Before AS Goes High	30			ns	
T_{LA}	Address Hold After AS Goes High	20			ns	
T_{WDD}	Data Valid Before DS Goes High	50			ns	Write Mode
T_{LL}	Address Latch Pulse Width	60			ns	
T_{WDH}	Data Hold After DS Goes High	20			ns	
T_{WW}	R/W and DS	80			ns	
T_{RDH}	Data Hold After DS Goes High	0		50	ns	Read Mode
T_{RDD}	Data Valid After DS Goes Low			50	ns	Read Mode



NOTE 1: DATA IN/OUT SPECIFIED FROM MICRO CONTROLLER STANDPOINT
2: R/W ACTIVE LOW COVER DS LOW IN WRITE MODE

Controller Interface Timing



XR-2130 EQUIVALENT SCHEMATIC DIAGRAM

PRINCIPLES OF OPERATION

The XR-2130 performs the complete 1200/300 BPS modem function when used with the XR-2131 modem controller or equivalent. The following discusses the function of each section of the XR-2130.

MODULATOR

Modulator data to be transmitted, T_{XD}, from the RS-232C port pin 2 first enters the XR-2131 modem controller. For 1200 BPS asynchronous operation, the T_{XD} passes through an async to sync converter. This converter function is to provide a sync T_{XD} and associated transmit clock, T_{XCLK}, to the demodulaor. The async input T_{XD} is character async as shown in Figure 1.

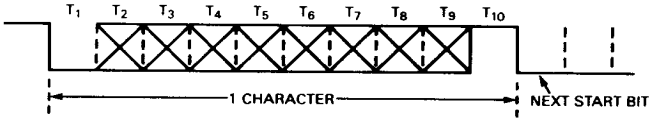


Figure 1. Async Character

The actual data, shown here as T2—T9, is bracketed by a start bit (T1) and stop bit (T10). The T_{XD} async data rate is 1200 BPS +1%/—2.5%. However the sync T_{XD} data rate must be 1200 BPS ± 0.01%. The async to sync converter corrects for this speed variation by adding or deleting stop bits.

For 300 BPS or 1200 BPS synchronous operation the input buffer is bypassed. The transmit clock and T_{XD} relationships are shown in Figure 2.

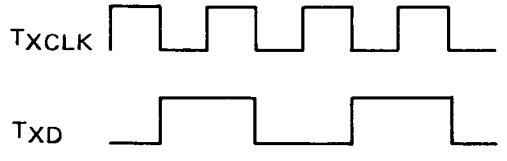


Figure 2. T_{XD}/T_{XCLK} Relationship

The T_{XCLK} is normally derived by the XR-2130. However, an external T_{XCLK} may be supplied to Pin 13, $E_{X\ CLK}$. This signal will then be used to control the clocking of the T_{XD} into the XR-2130. Again, the data must be valid on the rising edge of the T_{XCLK}.

T_{XD} enters the XR-2130 through Pin 10, T_{XD}, where 1200 BPS data goes through a scrambling process. The scrambler is used to randomize the T_{XD} as certain data patterns may make it difficult to extract the necessary R_{XCLK} from the R_{XC}. The scrambler circuitry and algorithm are shown in Figure 3.

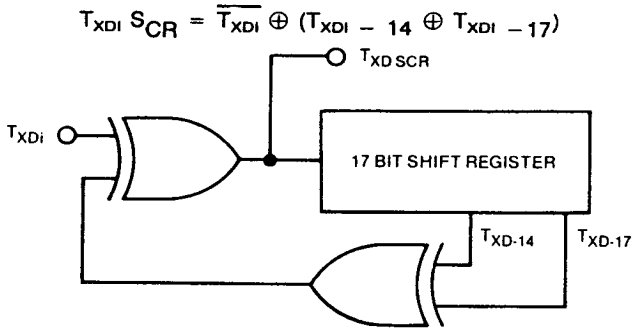


Figure 3. 17 Bit Psuedo Random Scrambler

The scrambled data then passes through a dibit encoder. This circuit groups the data in pairs of bits and generates differential phase information from the data pairs as shown in Figure 4.

T_{XDN}	T_{XDN+1}	PHASE SHIFT
0	0	90°
0	1	0°
1	1	270°
1	0	180°

T_{XDN}, T_{XDN+1}: Successive Data Bits Group To Form a Dibit

Figure 4. Dibit/Phase Shift Encoding

The dibit encoded information does not present sudden phase jumps but gradual ones. This allows precise shaping of the transmit carrier, T_{XC}, and is accomplished through digital echo modulation circuit techniques. The T_{XC} goes to an output T_{XC} MUX to select between T_{XC} 1200 BPS and T_{XC} 300 BPS.

300 BPS T_{XD} bypasses the scrambler and dibit encoder, and goes directly into a single tone sinewave synthesizer for generating the mark/space frequency pairs for answer and originate modes, shown in Figure 5. This circuitry is also used to generate the 2100 Hz for V.22 answer tones.

T_{XD}	MODE	CARRIER FREQUENCY
0	ANS	1070 Hz
1	ANS	1270 Hz
0	ORIG	2025 Hz
1	ORIG	2225 Hz

0 = space, 1 = mark

Figure 5. 300 BPS T_{XC} Frequencies

The FSK encoded carrier then goes to the output T_X MUX.

The T_{XC} MUX feeds a six bit output DAC to supply the T_{XC} to be filtered and sent to the telephone hybrid cicuitry.

FILTER

The filter on the XR-2130 is used for transmit and receive filtering as well as in the call progress mode. For transmit and receive modes, each filter provides a high order 600 Hz wide bandpass filter centered at either 1200 Hz or 2400 Hz. Each of these filters also provide half-channel compromise group delay equalizers. Figure 6 shows the transmit/receive frequency assignment for each mode. A notch filter at both 550 Hz and 1800 Hz is also included in the lowband to remove the locally generated guard tone during V.22 operation.

The output of the filters also have 2 pole smoothing filters to remove the clock frequency.

MODE	TRANSMIT FILTER	RECEIVE FILTER
Answer	2400 Hz	1200 Hz
Originate	1200 Hz	2400 Hz

Figure 6. Transmit/Receive Frequency Assignments

During the call progress mode, the low band filter (1200 Hz) is scaled down by a factor of 2.5 to a center frequency of 480 Hz. For this mode of operation, the call progress tones are monitored through the scaled low band filter and at the same time, answer tone or voice signal can be monitored through the unscaled high band filter. Figure 7B shows the control states for setting the CD circuit in high or low band. The signals detected by CD in low band are dial tone, busy tone, and ring back. In the high band, CD is used for answer tone. Figure 8 shows the timing characteristics of each of these signals.

A/$\overline{O}$	ALB	CPM	CD FREQUENCY BAND
0	0	1	High
1	0	1	Low

Figure 7B. CD Frequency Band Assignments

CD FREQUENCY BAND	SIGNAL	TIMING
Low	Dial Tone	Continuous
Low	Busy Tone	0.5 sec on/off
Low	Ring Back	2 sec on/4 sec off
High	Answer Tone	Continuous

Figure 8. Call Progress Tones

An example of call progress detection mode is as follows: (See Figure 7A.)

1. Set the call progress mode bit.
2. Carrier detection (CD) is set to low band (see Figure 7B).
3. The phone line is put in the "off hook" position (μP port).
4. The dial tone is monitored by checking CD for a continuous period, set by the "watch dog timer." If no CD is seen by the end of the timer period, echo "no dial tone."
5. If a dial tone is detected, send out a DTMF digit, turn T_{XEN} on and then off, and monitor CD again. CD is now checked again, and if it still detects a dial tone, echo "dial number not accepted, check phone number or change to pulse dialing." This procedure will be continued until all digits are sent out.
6. The microcontroller is now expecting one of the following signals:

   A) Busy Tone
   B) Ring Back
   C) Answer Tone

The controller will first check CD for a busy tone. If the busy tone is not present, the ring back signal will be checked. After two seconds of checking for ring back, the controller will look at CD in the high band for answer tone. If answer tone is detected, prepare for the handshake sequence, otherwise, go back and check CD for busy or ring back tones again.

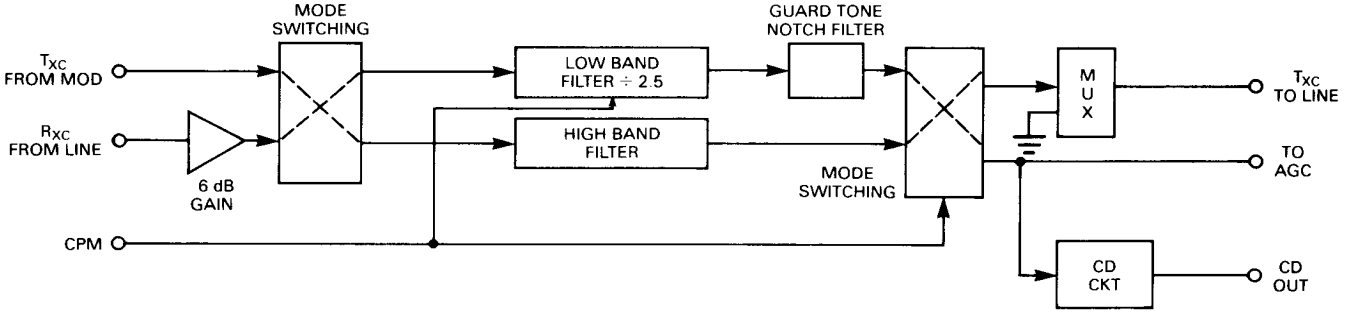


Figure 7 A. Call Progress Mode

AGC CIRCUIT

Following the receive filter output is an AGC circuit. This circuit is a digitally programmable gain amplifier which has 46.5 dB of dynamic range in 1.5 dB steps, 31 steps total.

The gain of the AGC circuit is compared to a preset window. If the ouput of the AGC goes outside the window, a 5 bit up/down counter will adjust the AGC to bring the level back within this window.

The AGC loop response is controlled by an external R/C filter which can be tailored by the user to his specific application.

DEMODULATION

The AGC output routes the received modulated carrier into both FSK and DPSK demodulators.

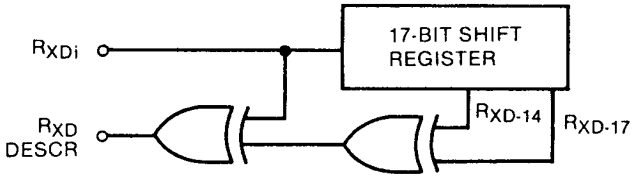
The DPSK (1200 BPS) demodulator utilizes a Costas Loop PLL coherent demodulation technique.

The AGC output is mixed together with inphase and quadphase carrier generated from the carrier recovery circuit.

A mixer, or phase detector circuit, generates I and Q signals which are each low pass filtered and passed through slicer circuits.

The slicer outputs and filter outputs are cross multiplied to generate the Costas Loop error voltage and eye diagram output, which can be used to monitor the demodulation quality.

A timing recovery pulse sets the point of sampling of the eye output at its maximum opening. The resultant sampled data will then be decoded from dibit information back to normal serial data. The data is then descrambled as shown in Figure 9.



$R_{XD\ DESCR} = R_{XDi}\ (1 \oplus R_{XD\ -14} \oplus R_{XD\ -17})$

Figure 9. 17 Bit Psuedo Random Descrambler and Algorithm

⊕ = Exclusive OR function

The descrambled data then passes through a sync to async converter to put it into a character async format for the RS-232 port.

The 300 BPS FSK demodulator also gets its input from the output of the AGC circuit. First, the signal passes through a slicer and then into a digital PLL. The PLL error voltage passes through a low pass filter and slicer to produce demodulated FSK data.

The DPSK and FSK demodulated data outputs are run to an output mux to select the proper output.

CARRIER DETECTION (CD)

The CD circuit is a peak detector circuit with typically -47 dBM as an upper threshold and -52 dBM as a lower threshold. These levels are set such that with a 4 dB hybrid loss, the CD levels at Tip and Ring will be -43 dBM and -48 dBM. The CD circuit has 2 dB of hysteresis built-in.

The detection levels of the CD circuit are changed during the call progress detection mode to typically -34 dBm detect level and -40 dBm reject level, again with 2 dB of hystersis.

LOOPBACK TEST FACILITIES

Analog loopback (ALB) is a local test mode which verifies the proper operation of the entire local modem. The analog transmit carrier will be connected from the transmit filter output to the AGC input, bypassing the receive filter. The line signal will be squelched.

During ALB, the microcontroller can also monitor ring indicator and terminate ALB if it becomes active and transmit answer tone immediately.

The following describes the control for ALB:

CPM = 0, ALB = 1, $A/\overline{O}$ = 0
T_X = Low Band (Bypass R_X High Band Filter)
R_X = Low Band

CPM = 0, ALB = 1, $A/\overline{O}$ = 1
T_X = High Band (Bypass R_X Low Band Filter)
R_X = High Band

Digital loopback (DLB) is used to check the remote modem (RDLB). The modem controller will check undescrambled data to recognize the RDLB request and set the RDLB bit to connect the R_{XCLK} to TXCLK and R_{XD} to T_{XD}.

PIN DESCRIPTIONS

Pin No.	Name	I/O	DESCRIPTION
Power			
28	V_{DD}	I	Positive Supply +5 V ± 5%
26	V_{SS}	I	Negative Supply -5 V ± 5%
22	A_{GND}	I	Analog Ground
14	D_{GND}	I	Digital Ground

Clock

15	MSCLK	I	Master Clock Input 11.0592 MHz ± 0.01%

Modem Controller Interface

5	$\overline{AS}$	I	Address Latch Strobe
1	AD0	I/O	Address/Data Bus 0
2	AD1	I/O	Address/Data Bus 1
3	AD2	I/O	Address/Data Bus 2
4	AD3	I/O	Address/Data Bus 3
6	R/$\overline{W}$	I	Read/$\overline{Write}$
7	$\overline{DS}$	I	$\overline{Data\ Strobe}$
8	$\overline{CS}$	I	$\overline{Chip\ Select}$

RS-232C Interface

13	E_{XCLK}	I	External T_{XCLK} Input for external timing during sync mode.
12	T_{XCLK}	O	Transmit Clock Output. Used in sync mode to latch data on TXD pin. External mode: lock with E_{XCLK}.
11	R_{XCLK}	O	Receive Clock Output derived from the sync clock. The falling edge coincides with R_{XD} transitions.
10	T_{XD}	I	Transmit Data Input 1200 BPS ±0.01% for PSK, 300 BPS for FSK.
9	R_{XD}	O	Receive Data Output 1200 BPS ±0.01% for PSK and 300 BPS for FSK.

Analog Interface

25	R_{XC}	I	Received FSK/DPSK Modulated Carrier Signal
27	T_{XC}	O	Transmitter Carrier Signal
20	AGCRP	I	AGC Response Control. R/C to VSS. R = 220kΩ, C = 0.1 μF typically.
23	AGCIN	I	AGC Input. Capacitively coupled from FLTOUT pin.
24	FLTOUT	O	Received Filter Output. Capacitively coupled to AGCIN.
19	EYE	O	Eye Pattern Output. Can be used to monitor demodulation quality.
21	SPKR	O	Audio Output to Speaker
17	DEMOD IN	I	Demodulator Input
18	AGCOUT	O	AGC Output
16	VREF	O	Reference Voltage Output

MODEM CONTROLLER INTERFACE

The XR-2130 may be connected directly with the XR-2131 modem controller or other common microcontrollers, such as an 8051 type. The controller interface is based on nibble data transferring, timing is shown in the Controller Interface Timing illustration on page 2.

Bit mapping of the write register and read registers are shown in Figure 11 and 12 respectively.

Address	Bit 3	Bit 2	Bit 1	Bit 0
0	SCREN	A/O	RDLB	FSK/$\overline{PSK}$
1	E_{XCKEN}	T_{XEN}	CPM	ALB
2	R_{XDMK}	SPKR	GTE	GTS
3	DIL3	DIL2	DIL1	DIL0
4	DTMF	T_{XL2}	T_{XL1}	T_{XL0}
5	ANS21	DIS64	PDN	HS
6	–	–	–	–
7	–	–	–	–

Figure 11. Write Register Bit Mapping

Address	Bit 3	Bit 2	Bit 1	Bit 0
0	–	–	–	CD
1	–	–	UNRXD	RXD

Figure 12. Read Register Bit Mapping

FUNCTION DESCRIPTIONS

The following is a description of the function and state of each of the write bits:

Name	Logic Level	Function
SCREN	1	Scrambler/Descrambler On
	0	Scrambler/Descrambler Off
A/$\overline{O}$	1	Answer Mode
	0	Originate Mode
RDLB	1	Remote Digital Loopback
	0	Normal Mode
FSK/$\overline{PSK}$	1	FSK Operation
	0	PSK Operation

EXCKEN	1	Enable External Clock for TXCLK
	0	Internal Clock for TXCLK
TXEN	1	Transmitter Enable
	0	Transmitter Disable
CPM	1	Call Progress Mode
	0	Normal Mode
ALB	1	Analog Loopback Enable
	0	Normal Mode
RKDMK	1	RXD Clamped to Mark State
	0	RXD Normal
SPKR	1	Speaker Output On
	0	Speaker Output Off
GTE	1	Enable Guard Tone to High Band
	0	Disable Guard Tone
GTS	1	Select 550 Hz Guard Tone
	0	Select 1800 Hz Guard Tone

The DTMF dialing tone is enabled with T_{XEN} = 1, 1 = DTMF Tone Enable, 0 = DTMF Tone Disable.

The output transmit level is set using three T_{XL} bits as shown in Figure 13.

TXL2	TXL1	TXL0	TXC LEVEL
0	0	0	0 dBM
0	0	1	-1.5 dBM
0	1	0	-3.0 dBM
0	1	1	-4.5 dBM
1	0	0	-6.0 dBM
1	0	1	-7.5 dBM
1	1	0	-9.0 dBM
1	1	1	-10.5 dBM

Figure 13. TXC Output Level

The following illustrates the DTMF set bits and frequency pairs.

DIL3	DIL2	DIL1	DIL0	DIGIT	TONE PAIRS (Hz)	
0	0	0	0	0	941	1336
0	0	0	1	1	697	1209
0	0	1	0	2	697	1336
0	0	1	1	3	697	1477
0	1	0	0	4	770	1209
0	1	0	1	5	770	1336
0	1	1	0	6	770	1477
0	1	1	1	7	852	1209
1	0	0	0	8	852	1336
1	0	0	1	9	852	1477
1	0	1	0	*	941	1209
1	0	1	1	#	941	1477
1	1	0	0	–	697	1633
1	1	0	1	–	770	1633
1	1	1	0	–	852	1633
1	1	1	1	–	941	1633

The remaining four write bits are as follows:

Name	Logic Level	Function
ANS21 A/$\overline{O}$ = 1 FSK/$\overline{PSK}$ = 1	1	Generate 2100 Hz Answer Tone
	0	No 2100 Hz Answer Tone
DIS64	1	Disable 64 Bit Mark Detector
	0	Enable 64 Bit Mark Detector
PDN	1	Power Down Mode
	0	Normal Operation
HS	1	Handshake Mode - widen capture range of R_{XCLK} recovery circuit for fast response. Also generate a new sync pulse to force an immediate DPLL lock on 0 to 1 transition of HS bit.
	0	Normal Mode

The following is a description of the function and state of each of the read register bits:

CD 1 = Energy Detected
0 = No Energy

CPM	ALB	A/$\overline{O}$	CD
1	0	0	Receiving high band, monitoring for answer tone.
1	0	1	Receiving low band filter output with this filter scaled down by a factor of 2.5. Detecting dial tone, busy and ring back signals.
0	0	0	Normal high band received energy detect.
0	0	1	Normal low band received energy detect.

Received data is available at two different outputs:

UNRXD = Undescrambled Received Data
RXD = Descrambled Received Data for PSK or FSK Data.

MASTER CLOCK CIRCUIT

This input is the master clock input for the XR-2130. The frequency of this input controls the transmit data clock and other critical frequencies. The nominal frequency should be 11.0592 MHz with plus or minus 0.01% accuracy.

APPLICATIONS

A complete stand alone bell 212A or CCITT V.22 modem is shown in Figure 14.

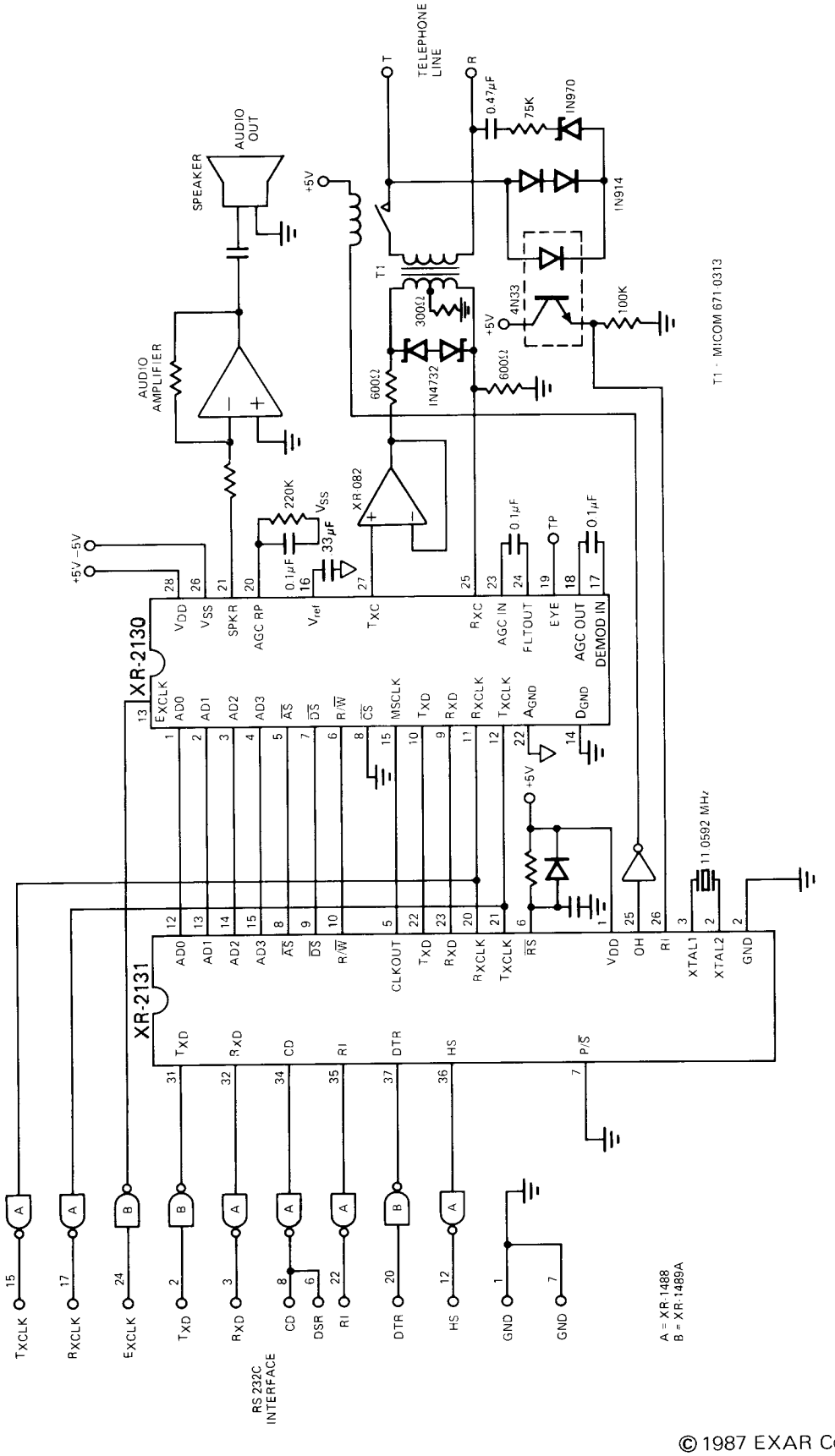


Figure 14. Complete 212A/V.22 Modem Stand Alone Application