

Quad Schottky Diode Array

FEATURES

- Matched, Four-Diode Monolithic Array
- High Peak Current
- Low-Cost MINIDIP Package
- Low-Forward Voltage
- Parallelable for Lower V_F or Higher I_F
- Fast Recovery Time
- Military Temperature Range Available

DESCRIPTION

This four-diode array is designed for general purpose use as individual diodes or as a high-speed, high-current bridge. It is particularly useful on the outputs of high-speed power MOSFET drivers where Schottky diodes are needed to clamp any negative excursions caused by ringing on the driven line.

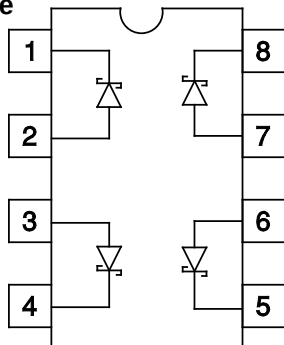
These diodes are also ideally suited for use as voltage clamps when driving inductive loads such as relays and solenoids, and to provide a path for current free-wheeling in motor drive applications.

The use of Schottky diode technology features high efficiency through lowered forward voltage drop and decreased reverse recovery time.

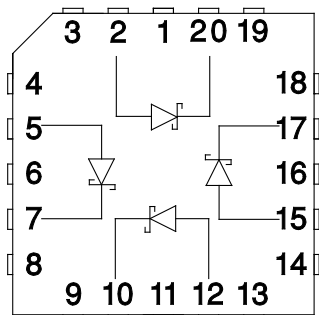
This single monolithic chip is fabricated in both hermetic CERDIP and copper-leaded plastic packages. The UC1611 in ceramic is designed for -55°C to $+125^{\circ}\text{C}$ environments but with reduced peak current capability: while the UC3611 in plastic has higher current rating over a 0°C to $+70^{\circ}\text{C}$ ambient temperature range.

CONNECTION DIAGRAM

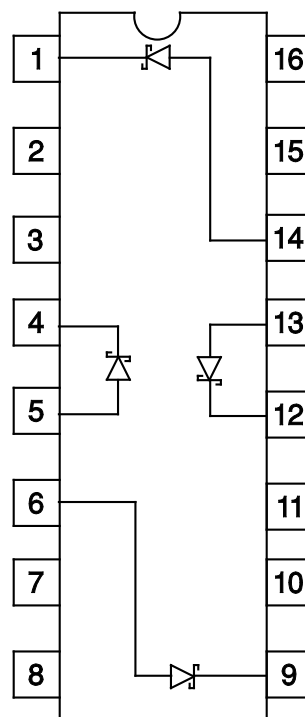
DIL-8 (TOP VIEW)
N or J Package



PLCC-20 (TOP VIEW)
Q Package



SOIC-16 (TOP VIEW)
DW Package



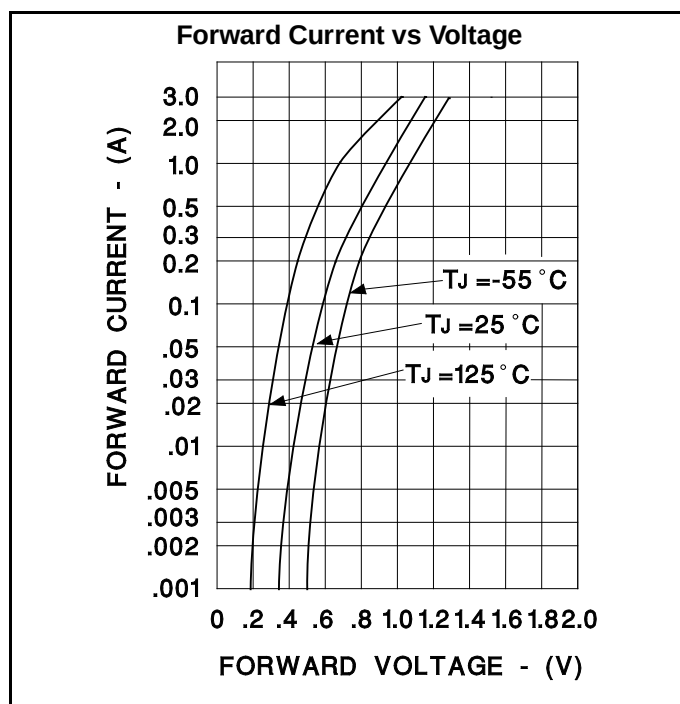
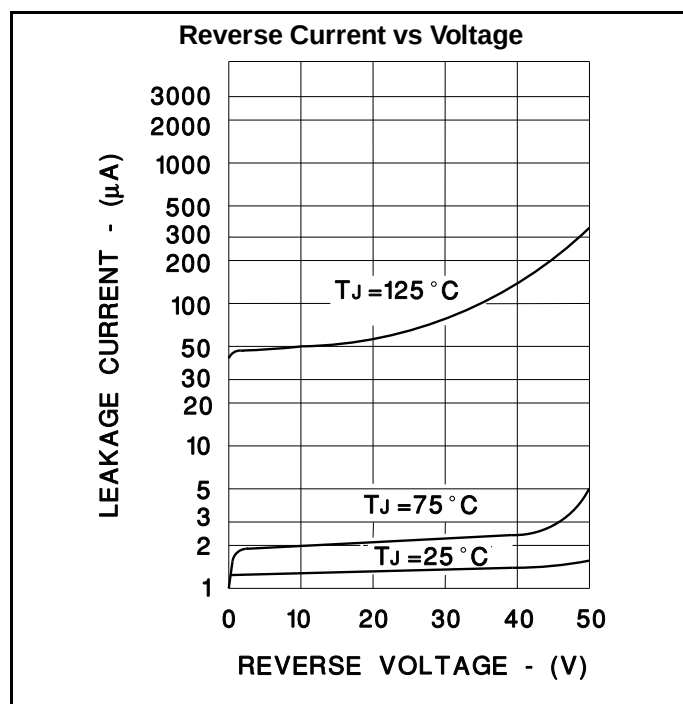
ABSOLUTE MAXIMUM RATINGS

Peak Inverse Voltage (per Diode). 50V
 Diode-to-Diode Voltage. 80V
 Peak Forward Current
 UC1611 1A
 UC3611 3A
 Power Dissipation at $T_A = +70^{\circ}\text{C}$ 1W
 Storage Temperature Range -65°C to $+150^{\circ}\text{C}$
 Lead Temperature (Soldering, 10 Seconds). $+300^{\circ}\text{C}$
Note: Please consult Packaging Section of Databook for thermal limitations and considerations of package.

ELECTRICAL CHARACTERISTICS: All specifications apply to each individual diode. $T_J = +25^{\circ}\text{C}$ except as noted.
 $T_A = T_J$.

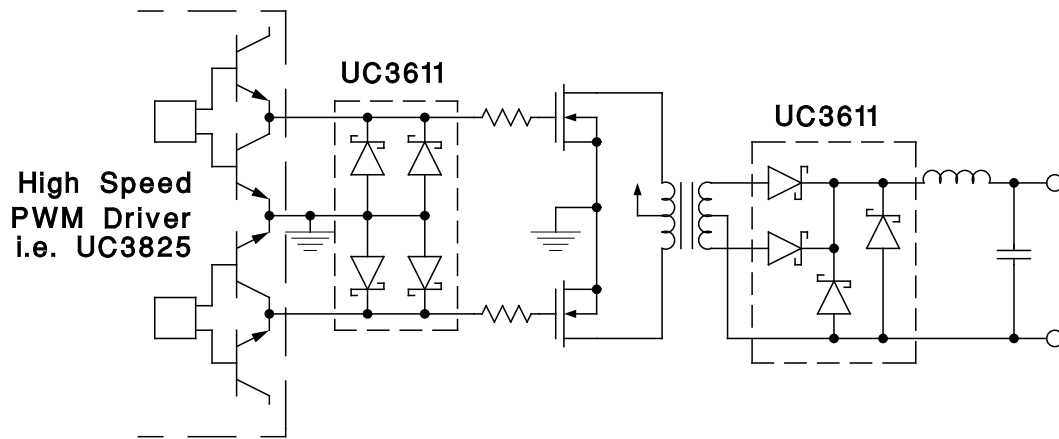
PARAMETER	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
Forward Voltage Drop	$I_F = 100\text{mA}$	0.3	0.4	0.7	V
	$I_F = 1\text{A}$		0.9	1.2	V
Leakage Current	$V_R = 40\text{V}$		0.01	0.1	mA
	$V_R = 40\text{V}, T_J = +100^{\circ}\text{C}$		0.1	1.0	mA
Reverse Recovery	0.5A Forward to 0.5A Reverse		20		ns
Forward Recovery	1A Forward to 1.1V Recovery		40		ns
Junction Capacitance	$V_R = 5\text{V}$		100		pF

Note: At Forward currents of greater than 1.0A, a parasitic current of approximately 10mA may be collected by adjacent diodes.

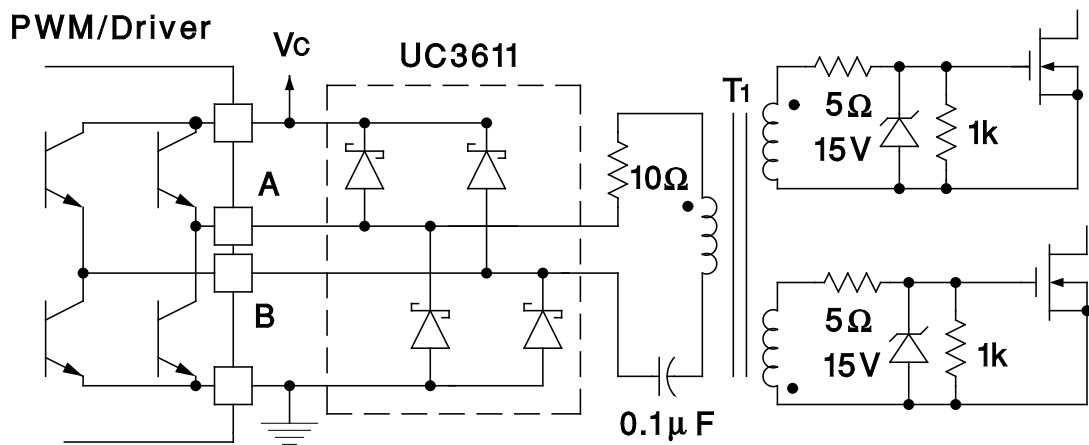


TYPICAL APPLICATIONS

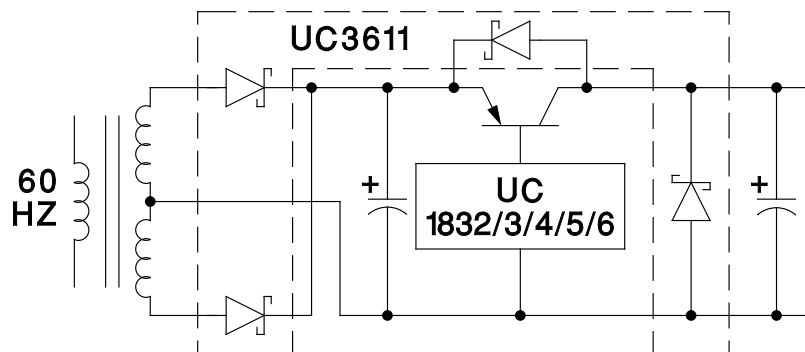
A. Clamp Diodes - PWMS and Drivers



B. Transformer Coupled Drive Circuits



C. Linear Regulations



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Power Management

[Power Management](#) > [Power Supply Support](#) > [Schottky Diode Arrays](#)



UC1611, QUAD SCHOTTKY DIODE ARRAY

Device Status: Active

- > [Description](#)
- > [Features](#)
- > [Datasheets](#)
- > [Pricing/Samples/Availability](#)
- > [Application Notes](#)

Parameter Name	UC1611
Output Current (A)	1
Vin (V)	0
Vin (max) (V)	50
Pin Count	8

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To view the following documents, [Acrobat Reader 3.x](#) is required.

To download a document to your hard drive, right-click on the link and choose 'Save'.

Datasheets

Full datasheet in Acrobat PDF: [slus338.pdf](#) (158 KB)

Pricing/Samples/Availability

<u>Orderable Device</u>	<u>Package</u>	<u>Pins</u>	<u>Temp (°C)</u>	<u>Status</u>	<u>Price/unit USD (100-999)</u>	<u>Pack Qty</u>	<u>DSCC Number</u>	<u>Availability / Samples</u>
5962-90538012A	<u>L</u>	20	-55 TO 125	ACTIVE	40.75	1		Check stock or order
5962-9053801PA	<u>J</u>	8	-55 TO 125	ACTIVE	20.86	1		Check stock or order
UC1611J	<u>J</u>	8	-55 TO 125	ACTIVE	16.40	1		Check stock or order
UC1611J883B	<u>J</u>	8	-55 TO 125	ACTIVE	20.86	1		Check stock or order
UC1611L	<u>L</u>	20	-55 TO 125	ACTIVE	54.33	1		Check stock or order
UC1611L883B	<u>L</u>	20	-55 TO 125	ACTIVE	40.75	1	5962-90538012A	Check stock or order

Application Reports

- [ELECTROSTATIC DISCHARGE APPLICATION NOTE \(SSYA008 - Updated: 05/05/1999\)](#)
- [THERMAL CHARACTERISTICS OF LINEAR AND LOGIC PACKAGES USING JEDEC PCB DESIGNS \(SZZA017A - Updated: 09/10/1999\)](#)

Table Data Updated on: 8/16/2000