12.0 ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings †

Ambient Temperature under bias ..... –40° to +125°C

Storage Temperature ..... –65° to +150°C

Voltage on any pin with respect to Vss (except VDD and $\overline{MCLR}$) .....–0.3V to VDD + 0.3V

Voltage on VDD with respect to Vss ..... 0 to +7.5V

Voltage on $\overline{MCLR}$ with respect to Vss (Note 2) .....0 to +14V

Total power Dissipation (Note 1) 1.0W

Maximum Current out of Vss pin .....300 mA

Maximum Current into VDD pin .....250 mA

Input Clamp Current, IIK (VI<0 or VI> VDD) .....±20 mA

Output Clamp Current, IOK (Vo <0 or Vo>VDD) .....±20 mA

Maximum Output Current sunk by any I/O pin .....25 mA

Maximum Output Current sourced by any I/O pin.....25 mA

Maximum current sunk by PORTA, PORTB, and PORTE (combined) (Note 2).....200 mA

Maximum current sourced by PORTA, PORTB, and PORTE (combined) (Note 2).....200 mA

Maximum current sunk by PORTC and PORTD (combined) (Note 2).....200 mA

Maximum current sourced by PORTC and PORTD (combined) (Note 2).....200 mA

Note 1: Power dissipation is calculated as follows: $P_{DIS} = V_{DD} \times \{I_{DD} - \sum I_{OH}\} + \sum \{(V_{DD}-V_{OH}) \times I_{OH}\} + \sum(V_{OL} \times I_{OL})$

Note 2: PORTD and PORTE are not implemented on the PIC16C641 and PIC16C642.

† **NOTICE**: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 12-1: CROSS REFERENCE OF DEVICE SPECS FOR OSCILLATOR CONFIGURATIONS AND FREQUENCIES OF OPERATION (COMMERCIAL DEVICES)

OSC	PIC16C641-04 PIC16C642-04 PIC16C661-04 PIC16C662-04	PIC16C641-10 PIC16C642-10 PIC16C661-10 PIC16C662-10	PIC16C641-20 PIC16C642-20 PIC16C661-20 PIC16C662-20	PIC16LC641-04 PIC16LC642-04 PIC16LC661-04 PIC16LC662-04	JW Devices
RC	VDD: 4.0V to 6.0V IDD: 5 mA max. @ 5.5V IPD: 21 µA max. @ 4.0V Freq: 4.0 MHz max.	VDD: 4.5V to 5.5V IDD: 2.7 mA typ. @ 5.5V IPD: 1.5 µA typ. @ 4.0V Freq: 4.0 MHz max.	VDD: 4.5V to 5.5V IDD: 2.7 mA typ. @ 5.5V IPD: 1.5 µA typ. @ 4.0V Freq: 4.0 MHz max.	VDD: 3.0V to 6.0V IDD: 2.0 mA typ. @ 3.0V IPD: 0.9 µA typ. @ 3.0V Freq: 4.0 MHz max.	VDD: 4.0V to 6.0V IDD: 5 mA max. @ 5.5V IPD: 21 µA max. @ 4.0V Freq: 4.0 MHz Max.
XT	VDD: 4.0V to 6.0V IDD: 5 mA max. @ 5.5V IPD: 21 µA max. @ 4.0V Freq: 4.0 MHz max.	VDD: 4.5V to 5.5V IDD: 2.7 mA typ. @ 5.5V IPD: 1.5 µA typ. @ 4.0V Freq: 4.0 MHz max.	VDD: 4.5V to 5.5V IDD: 2.7 mA typ. @ 5.5V IPD: 1.5 µA typ. @ 4.0V Freq: 4.0 MHz max.	VDD: 3.0V to 6.0V IDD: 2.0 mA typ. @ 3.0V IPD: 0.9 µA typ. @ 3.0V Freq: 4.0 MHz max.	VDD: 4.0V to 6.0V IDD: 5 mA max. @ 5.5V IPD: 21 µA max. @ 4.0V Freq: 4.0 MHz max.
HS	VDD: 4.5V to 5.5V IDD: 13.5 mA typ. @ 5.5V IPD: 1.5 µA typ. @ 4.5V Freq: 4.0 MHz max.	VDD: 4.5V to 5.5V IDD: 30 mA max. @ 5.5V IPD: 1.5 µA typ. @ 4.5V Freq: 10 MHz max.	VDD: 4.5V to 5.5V IDD: 30 mA max. @ 5.5V IPD: 1.5 µA typ. @ 4.5V Freq: 20 MHz max.	Do not use in HS mode	VDD: 4.5V to 5.5V IDD: 30 mA max. @ 5.5V IPD: 1.5 µA typ. @ 4.5V Freq: 10 MHz max.
LP	VDD: 4.0V to 6.0V IDD: 52.5 µA typ. @ 32 kHz, 4.0V IPD: 0.9 µA typ. @ 4.0V Freq: 200 kHz max.	Do not use in LP mode	Do not use in LP mode	VDD: 3.0V to 6.0V IDD: 48 µA max. @ 32 kHz, 3.0V IPD: 5.0 µA max. @ 3.0V Freq: 200 kHz max.	VDD: 3.0V to 6.0V IDD: 48 µA max. @ 32 kHz, 3.0V IPD: 5.0 µA max. @ 3.0V Freq: 200 kHz max.

The shaded sections indicate oscillator selections which are tested for functionality, but not for MIN/MAX specifications. It is recommended that the user select the device type that ensures the specifications required.

12.1 DC Characteristics: PIC16C641/642/661/662-04 (Commercial, Industrial, Automotive) PIC16C641/642/661/662-10 (Commercial, Industrial, Automotive) PIC16C641/642/661/662-20 (Commercial, Industrial, Automotive)

Standard Operating Conditions (unless otherwise stated)
Operating temperature –40°C ≤ TA ≤ +85°C for industrial,
0°C ≤ TA ≤ +70°C commercial, and
–40°C ≤ TA ≤ +125°C automotive

Param No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
D001	VDD	Supply Voltage	4.0	–	6.0	V	XT, RC and LP osc configuration
D001A			4.5	–	5.5	V	HS osc configuration
D002*	VDR	RAM Data Retention Voltage(1)	1.5	–	–	V	Device in SLEEP mode
D003	VPOR	VDD start voltage to ensure internal Power-on Reset signal	–	VSS	–	V	See section on Power-on Reset for details
D004*	SVDD	VDD rise rate to ensure internal Power-on Reset signal	0.05	–	–	V/ms	See section on Power-on Reset for details
D005	VBOR	Brown-out Reset Voltage	3.7	4.0	4.3	V	BODEN configuration bit is clear
			3.7	4.0	4.4	V	Automotive
D010	IDD	Supply Current(2)	–	2.7	5	mA	XT and RC osc configuration FOSC = 4 MHz, VDD = 5.5V, WDT disabled (4)
D010A			–	35	70	µA	LP osc configuration, PIC16C64X & PIC16C66X-04 only FOSC = 32 kHz, VDD = 4.0V, WDT disabled
D013			–	13.5	30	mA	HS osc configuration FOSC = 20 MHz, VDD = 5.5V, WDT disabled
		Module Differential Current (5)					
D015	ΔIBOR	Brown-out Reset Current	–	350	425	µA	BODEN bit is clear, VDD = 5.0V
D016	ΔICOMP	Comparator Current for each Comparator	–	–	100	µA	VDD = 4.0V
D017	ΔIVREF	VREF Current	–	–	300	µA	VDD = 4.0V
D021	ΔIWDT	WDT Current	–	6.0	20	µA	VDD = 4.0V
			–	–	25	µA	Automotive
D021	IPD	Power-down Current (3)	–	1.5	21	µA	VDD = 4.0V, WDT disabled
			–	2.5	24	µA	Automotive

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5.0V, 25°C, unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as I/O pin loading and switching rate, oscillator type, internal code execution pattern, and temperature also have an impact on the current consumption.
The test conditions for all IDD measurements in active operation mode are:
OSC1 = external square wave, from rail to rail; all I/O pins tri-stated™, pulled to VDD,
$\overline{MCLR}$ = VDD; WDT enabled/disabled as specified.

3: The power-down current in SLEEP mode does not depend on the oscillator type. Power-down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD or VSS.

4: For RC osc configuration, current through Rext is not included. The current through the resistor can be estimated by the formula Ir = VDD/2Rext (mA) with Rext in kΩ.

5: The Δ current is the additional current consumed when this peripheral is enabled. This current should be added to the base IDD or IPD measurement.

12.2 DC Characteristics: PIC16LC641/642/661/662-04 (Commercial, Industrial)

Standard Operating Conditions (unless otherwise stated) Operating temperature –40°C ≤ TA ≤ +85°C for industrial and 0°C ≤ TA ≤ +70°C commercial							
Param No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
D001	VDD	Supply Voltage	3.0	–	6.0	V	XT, RC, and LP osc configuration
D002*	VDR	RAM Data Retention Voltage (1)	1.5	–	–	V	Device in SLEEP mode
D003	VPOR	VDD start voltage to ensure internal Power-on Reset signal	–	Vss	–	V	See section on Power-on Reset for details
D004*	SVDD	VDD rise rate to ensure internal Power-on Reset signal	0.05	–	–	V/ms	See section on Power-on Reset for details
D005	VBOR	Brown-out Reset Voltage	3.7	4.0	4.3	V	BODEN configuration bit is clear
D010	IDD	Supply Current (2)	–	2.0	3.8	mA	XT and RC osc configuration FOSC = 4.0 MHz, VDD = 3.0V, WDT disabled (4)
D010A			–	22.5	48	µA	LP osc configuration FOSC = 32 kHz, VDD = 3.0V, WDT disabled
		Module Differential Current (5)					
D015	ΔIBOR	Brown-out Reset Current	–	350	425	µA	BODEN bit is clear, VDD = 5.0V
D016	ΔICOMP	Comparator Current for each Comparator	–	–	100	µA	VDD = 3.0V
D017	ΔIVREF	VREF Current	–	–	300	µA	VDD = 3.0V
D021	ΔIWDT	WDT Current	–	6.0	20	µA	VDD = 3.0V
D021	IPD	Power-down Current (3)	–	0.9	5	µA	VDD = 3.0V, WDT disabled

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5.0V, 25°C, unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as I/O pin loading and switching rate, oscillator type, internal code execution pattern, and temperature also have an impact on the current consumption.
The test conditions for all IDD measurements in active operation mode are:
OSC1=external square wave, from rail to rail; all I/O pins tristated, pulled to VDD,
MCLR = VDD; WDT enabled/disabled as specified.

3: The power-down current in SLEEP mode does not depend on the oscillator type. Power-down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD or Vss.

4: For RC osc configuration, current through Rext is not included. The current through the resistor can be estimated by the formula Ir = VDD/2Rext (mA) with Rext in kΩ.

5: The Δ current is the additional current consumed when this peripheral is enabled. This current should be added to the base IDD or IPD measurement.

12.3 DC Characteristics: PIC16C641/661 (Commercial, Industrial, Automotive) PIC16C642/662 (Commercial, Industrial, Automotive) PIC16LC641/661 (Commercial, Industrial) PIC16LC642/662 (Commercial, Industrial)

Standard Operating Conditions (unless otherwise stated)
Operating temperature –40°C ≤ TA ≤ +85°C for industrial,
0°C ≤ TA ≤ +70°C commercial, and
–40°C ≤ TA ≤ +125°C automotive
Operating voltage VDD range as described in DC spec Section 12.1 and 12.2

Param No.	Sym	Characteristic	Min	Typ †	Max	Unit	Conditions
	VIL	**Input Low Voltage**					
		I/O ports					
D030		with TTL buffer	Vss	-	0.15VDD	V	For entire VDD range
			Vss	-	0.8V	V	4.5V ≤ VDD ≤ 5.5V
D031		with Schmitt Trigger input	Vss	-	0.2VDD	V	
D032		$\overline{MCLR}$, RA4/T0CKI,OSC1 (in RC mode)	Vss	-	0.2VDD	V	(1)
D033		OSC1 (XT and HS modes)	Vss	-	0.3VDD	V	
		OSC1 (LP modes)	Vss	-	0.6VDD-1.0	V	
	VIH	**Input High Voltage**					
		I/O ports					
D040		with TTL buffer	2.0	-	VDD	V	
D041		with Schmitt Trigger input	0.25VDD to 0.8V	-	VDD	V	
D042		$\overline{MCLR}$ RA4/T0CKI	0.8VDD	-	VDD	V	
D043		OSC1 (XT, HS, LP modes)	0.7VDD	-	VDD	V	
D043A		OSC1 (RC mode)	0.9VDD	-	-	V	(1)
D070	IPURB	**PORTB weak pull-up current**	50	200	400	µA	VDD = 5.0V, VPIN = VSS
	IIL	**Input Leakage Current(2,3)**					
		I/O ports (Except PORTA)	-	-	±1.0	µA	Vss ≤ VPIN ≤ VDD, pin at hi-impedance
D060		PORTA	-	-	±0.5	µA	Vss ≤ VPIN ≤ VDD, pin at hi-impedance
D061		RA4/T0CKI	-	-	±1.0	µA	Vss ≤ VPIN ≤ VDD
D063		OSC1, $\overline{MCLR}$	-	-	±5.0	µA	Vss ≤ VPIN ≤ VDD, XT, HS and LP osc configuration
	VOL	**Output Low Voltage**					
D080		I/O ports	-	-	0.6	V	IOL = 8.5 mA, VDD = 4.5V, -40° to +85°C
			-	-	0.6	V	IOL = 7.0 mA, VDD = 4.5V, +125°C
D083		OSC2/CLKOUT	-	-	0.6	V	IOL = 1.6 mA, VDD = 4.5V, -40° to +85°C
		(RC only)	-	-	0.6	V	IOL = 1.2 mA, VDD = 4.5V, +125°C

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: In RC oscillator configuration, the OSC1 pin is a Schmitt Trigger input. It is not recommended that the PIC16C64X & PIC16C66X be driven with external clock in RC mode.

2: The leakage current on the $\overline{MCLR}$ pin is strongly dependent on applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

3: Negative current is defined as coming out of the pin.

Standard Operating Conditions (unless otherwise stated)
Operating temperature –40°C ≤ TA ≤ +85°C for industrial,
0°C ≤ TA ≤ +70°C commercial, and
–40°C ≤ TA ≤ +125°C automotive
Operating voltage VDD range as described in DC spec Section 12.1 and 12.2

Param No.	Sym	Characteristic	Min	Typ †	Max	Unit	Conditions
	VOH	Output High Voltage (3)					
D090		I/O ports (Except RA4)	VDD-0.7	-	-	V	IOH = -3.0 mA, VDD = 4.5V, -40° to +85°C
			VDD-0.7	-	-	V	IOH = -2.5 mA, VDD = 4.5V, +125°C
D092		OSC2/CLKOUT	VDD-0.7	-	-	V	IOH = -1.3 mA, VDD=4.5V, -40° to +85°C
		(RC only)	VDD-0.7	-	-	V	IOH = -1.0 mA, VDD = 4.5V, +125°C
		Capacitive Loading Specs on Output Pins					
D100	COSC2	OSC2 pin	-	-	15	pF	In XT, HS and LP modes when external clock used to drive OSC1.
D101	CIO	All I/O pins/OSC2 (in RC mode)	-	-	50	pF	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: In RC oscillator configuration, the OSC1 pin is a Schmitt Trigger input. It is not recommended that the PIC16C64X & PIC16C66X be driven with external clock in RC mode.

2: The leakage current on the $\overline{MCLR}$ pin is strongly dependent on applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

3: Negative current is defined as coming out of the pin.

TABLE 12-2: COMPARATOR SPECIFICATIONS

Operating Conditions: 3.0V < VDD < 6.0V, -40°C < TA < +125°C, unless otherwise stated. Current consumption is specified in Table 12-1.

Characteristics	Sym	Min	Typ	Max	Units	Comments
Input offset voltage		-	± 5.0	± 10	mV	
Input common mode voltage*		0	-	VDD - 1.5	V	
CMRR*		35	-	-	db	
Response Time(1)*		-	150	400 600	ns ns	PIC16C64X/66X PIC16LC64X/66X
Comparator Mode Change to Output Valid*		-	-	10	µs	

* These parameters are characterized but not tested.

Note 1: Response time measured with one comparator input at (VDD - 1.5)/2 while the other input transitions from VSS to VDD.

TABLE 12-3: VOLTAGE REFERENCE SPECIFICATIONS

Operating Conditions: 3.0V < VDD < 6.0V, -40°C < TA < +125°C, unless otherwise stated. Current consumption is specified in Table 12-1.

Characteristics	Sym	Min	Typ	Max	Units	Comments
Resolution		VDD/24	-	VDD/32	LSb	
Absolute Accuracy		- -	- -	1/4 1/2	LSb LSb	Low Range (VRR = 1) High Range (VRR = 0)
Unit Resistor Value (R)*		-	2k	-	Ω	Figure 8-2
Settling Time(1)*		-	-	10	µs	

* These parameters are characterized but not tested.

Note 1: Settling time measured while VRR = 1 and VR<3:0> transitions from 0000 to 1111.

12.4 Timing Parameter Symbology

The timing parameter symbols have been created with one of the following formats:

1. TppS2ppS
2. TppS

T	
F Frequency	T Time

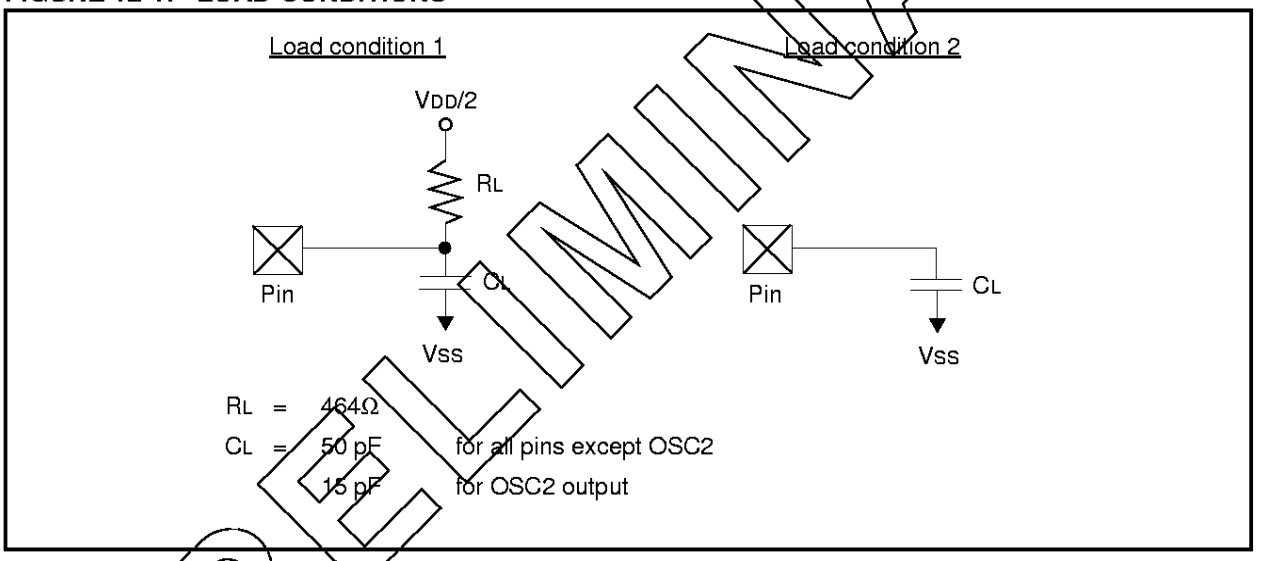
Lowercase subscripts (pp) and their meanings:

pp	
ck CLKOUT	osc OSC1
io I/O port	t0 T0CKI
mc $\overline{\text{MCLR}}$	

Uppercase letters and their meanings:

S	
F Fall	P Period
H High	R Rise
I Invalid (Hi-impedance)	V Valid
L Low	Z Hi-Impedance

FIGURE 12-1: LOAD CONDITIONS



12.5 Timing Diagrams and Specifications

FIGURE 12-2: EXTERNAL CLOCK TIMING

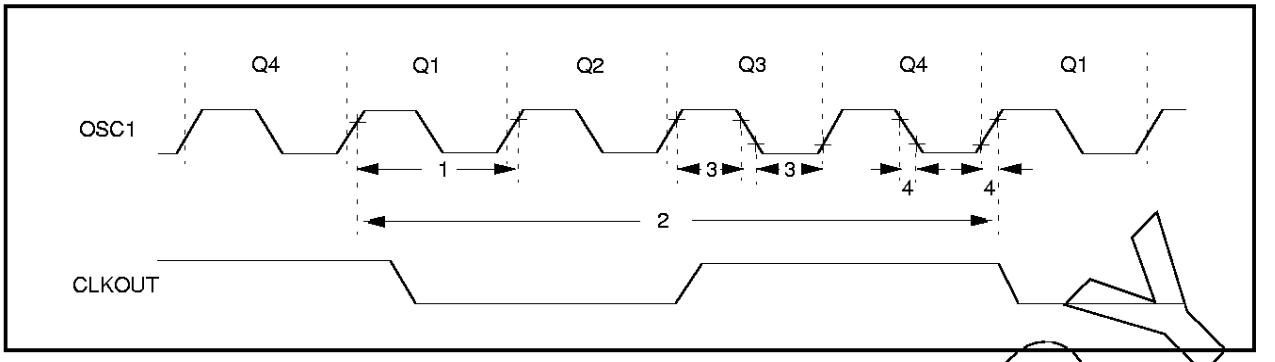


TABLE 12-4: EXTERNAL CLOCK TIMING REQUIREMENTS

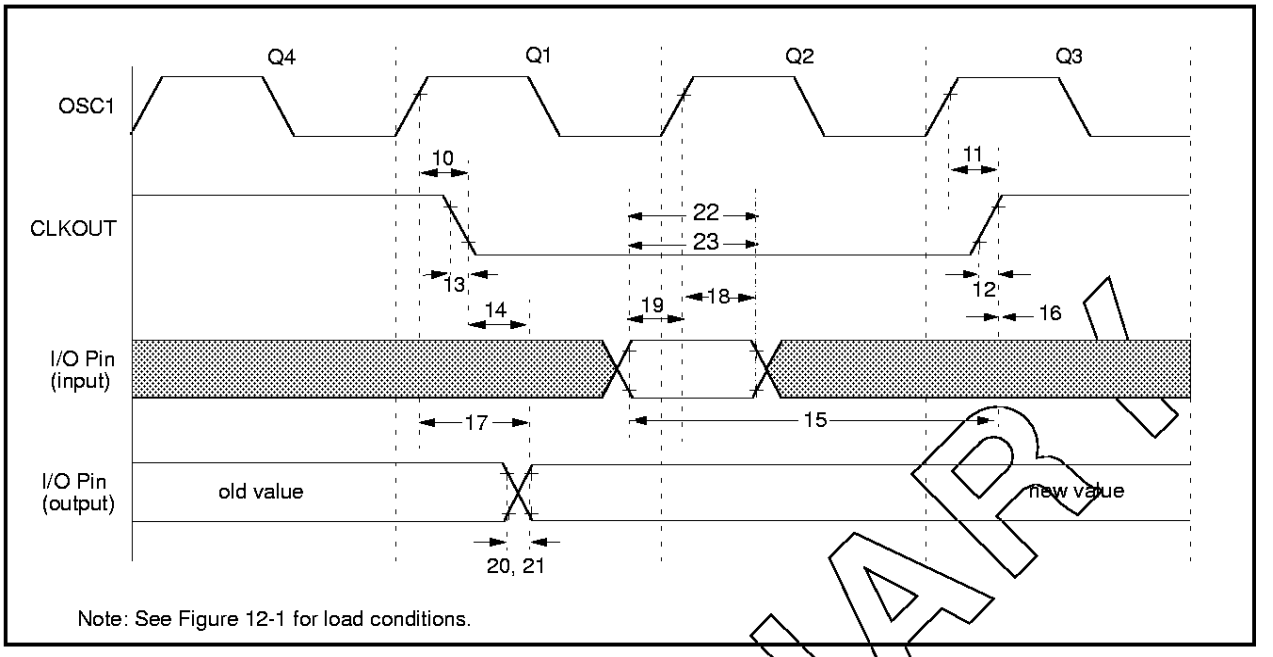
Param No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
	Fosc	**External CLKIN Frequency(1)**	DC	—	4	MHz	XT and RC osc mode, VDD = 5.0V
			DC	—	20	MHz	HS osc mode
			DC	—	200	kHz	LP osc mode
		Oscillator Frequency (1)	DC	—	4	MHz	RC osc mode, VDD = 5.0V
			0.1	—	4	MHz	XT osc mode
			4	—	20	MHz	HS osc mode
			5	—	200	kHz	LP osc mode
1	Tosc	**External CLKIN Period(1)**	250	—	—	ns	XT and RC osc mode
			50	—	—	ns	HS osc mode
			5	—	—	µs	LP osc mode
		Oscillator Period(1)	250	—	—	ns	RC osc mode
			250	—	10,000	ns	XT osc mode
			50	—	250	ns	HS osc mode
			5	—	—	µs	LP osc mode
2	TCY	**Instruction Cycle Time(1)**	200	—	DC	ns	TCY = FOSC/4
3*	TosL, TosH	**External Clock in (OSC1) High or Low Time**	100	—	—	ns	XT osc mode
			2.5	—	—	µs	LP osc mode
			15	—	—	ns	HS osc mode
4*	TosR, TosF	**External Clock in (OSC1) Rise or Fall Time**	—	—	25	ns	XT osc mode
			—	—	50	ns	LP osc mode
			—	—	15	ns	HS osc mode

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: Instruction cycle period (TCY) equals four times the input oscillator time-base period. All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. All devices are tested to operate at "min." values with an external clock applied to the OSC1 pin.
When an external clock input is used, the "Max." cycle time limit is "DC" (no clock) for all devices.

FIGURE 12-3: CLKOUT AND I/O TIMING



Note: See Figure 12-1 for load conditions.

TABLE 12-5: CLKOUT AND I/O TIMING REQUIREMENTS

Parameter No.	Sym	Characteristic		Min	Typ†	Max	Units	Conditions
10*	TosH2ckL	OSC1↑ to CLKOUT↓		—	75	200	ns	Note 1
11*	TosH2ckH	OSC1↑ to CLKOUT↑		—	75	200	ns	Note 1
12*	TckR	CLKOUT rise time		—	35	100	ns	Note 1
13*	TckF	CLKOUT fall time		—	35	100	ns	Note 1
14*	TckL2ioV	CLKOUT ↓ to Port out valid		—	—	0.5TCY + 20	ns	Note 1
15*	TioV2ckH	Port in valid before CLKOUT ↑		TOSC + 200	—	—	ns	Note 1
16*	TckH2iol	Port in hold after CLKOUT ↑		0	—	—	ns	Note 1
17*	TosH2ioV	OSC1↑ (Q1 cycle) to Port out valid		—	50	150	ns	
18*	TosH2iol	OSC1↑ (Q2 cycle) to Port input invalid (I/O in hold time)	PIC16C64X/66X	100	—	—	ns	
			PIC16LC64X/66X	200	—	—	ns	
19*	TioV2osH	Port input valid to OSC1↑ (I/O in setup time)		0	—	—	ns	
20*	TioR	Port output rise time	PIC16C64X/66X	—	10	40	ns	
			PIC16LC64X/66X	—	—	80	ns	
21*	TioF	Port output fall time	PIC16C64X/66X	—	10	40	ns	
			PIC16LC64X/66X	—	—	80	ns	
22††	Tinp	INT pin high or low time		TCY	—	—	ns	
23††	Trbp	RB7:RB4 change INT high or low time		TCY	—	—	ns	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

†† These parameters are asynchronous events not related to any internal clock edges.

Note 1: Measurements are taken in RC Mode where CLKOUT output is 4 x TOSC.

FIGURE 12-4: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER, AND POWER-UP TIMER TIMING

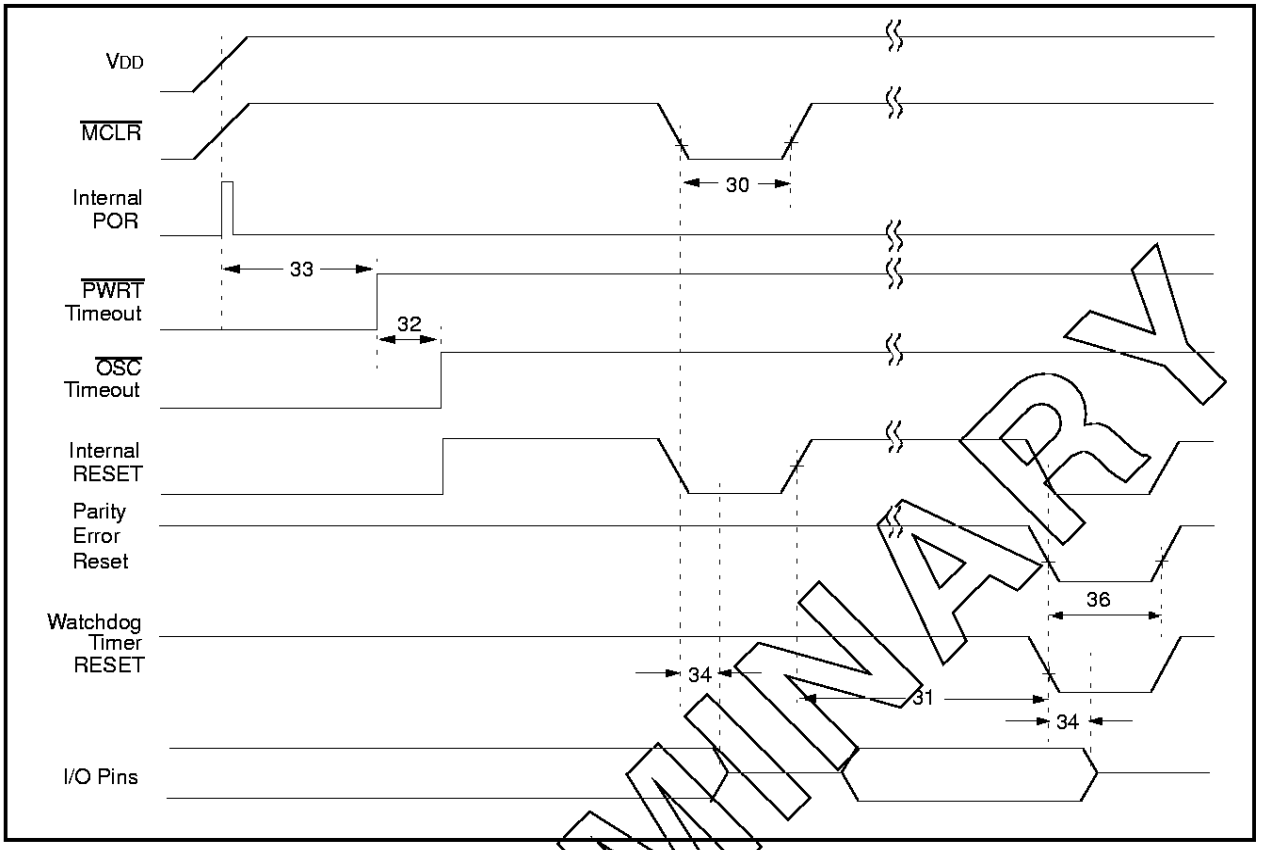


FIGURE 12-5: BROWN-OUT RESET TIMING

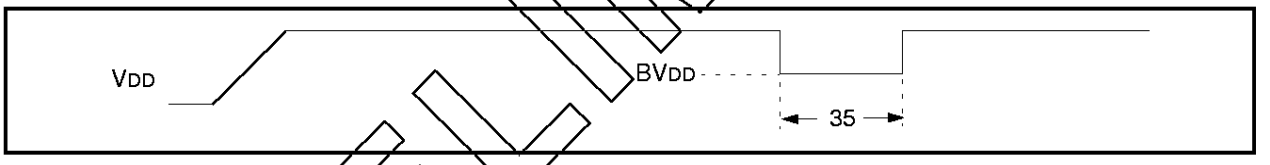


TABLE 12-6: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER, POWER-UP TIMER, AND BROWN-OUT RESET REQUIREMENTS

Parameter No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
30	TmcL	MCLR Pulse Width (low)	2	—	—	µs	VDD = 5V, -40°C to +125°C
31*	Twdt	Watchdog Timer Time-out Period (No Prescaler)	7	18	33	ms	VDD = 5V, -40°C to +125°C
32	Tost	Oscillation Start-up Timer Period	—	1024TOSC	—	—	TOSC = OSC1 period
33*	Tpwrt	Power up Timer Period	28	72	132	ms	VDD = 5V, -40°C to +125°C
34	TIOZ	I/O Hi-impedance from MCLR Low or Watchdog Timer Reset	—	—	2.1	µs	
35	TBOR	Brown-out Reset pulse width	100	—	—	µs	VDD ≤ BVDD (D005)
36	TPER	Parity Error Reset	—	TBD	—	µs	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

FIGURE 12-6: TIMER0 CLOCK TIMING

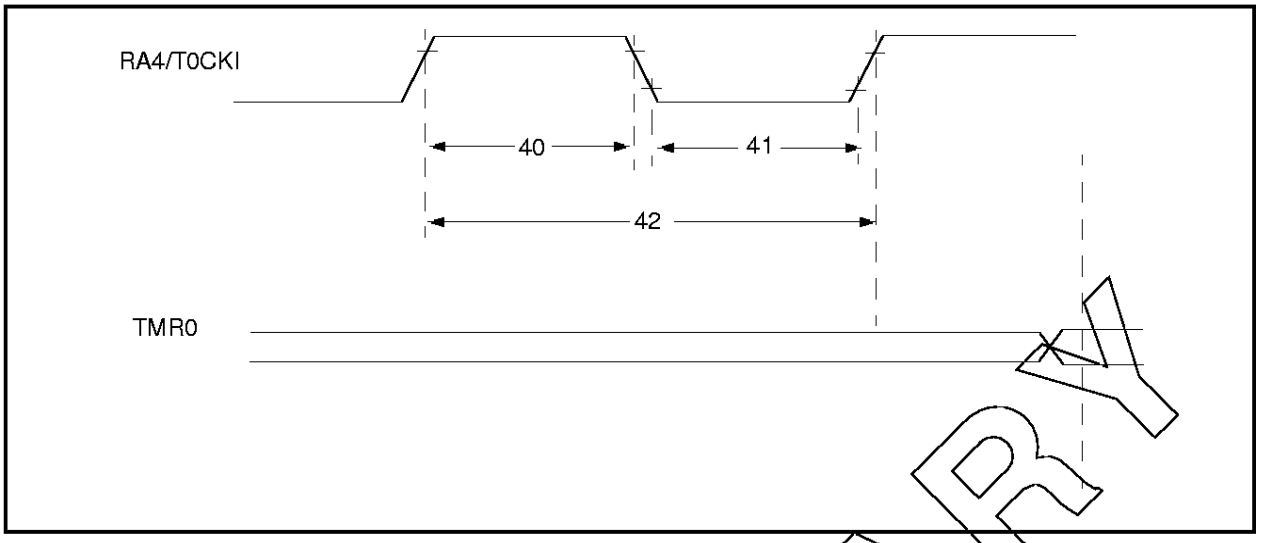


TABLE 12-7: TIMER0 CLOCK REQUIREMENTS

Param No.	Sym	Characteristic		Min	Typ†	Max	Units	Conditions
40*	Tt0H	T0CKI High Pulse Width	No Prescaler	0.5Tcy + 20	—	—	ns	
			With Prescaler	10	—	—	ns	
41*	Tt0L	T0CKI Low Pulse Width	No Prescaler	0.5Tcy + 20	—	—	ns	
			With Prescaler	10	—	—	ns	
42*	Tt0P	T0CKI Period		$\frac{Tcy + 40}{N}$	—	—	ns	N = prescale value (1, 2, 4, …, 256)

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

FIGURE 12-7: PARALLEL SLAVE PORT TIMING (PIC16C661 AND PIC16C662)

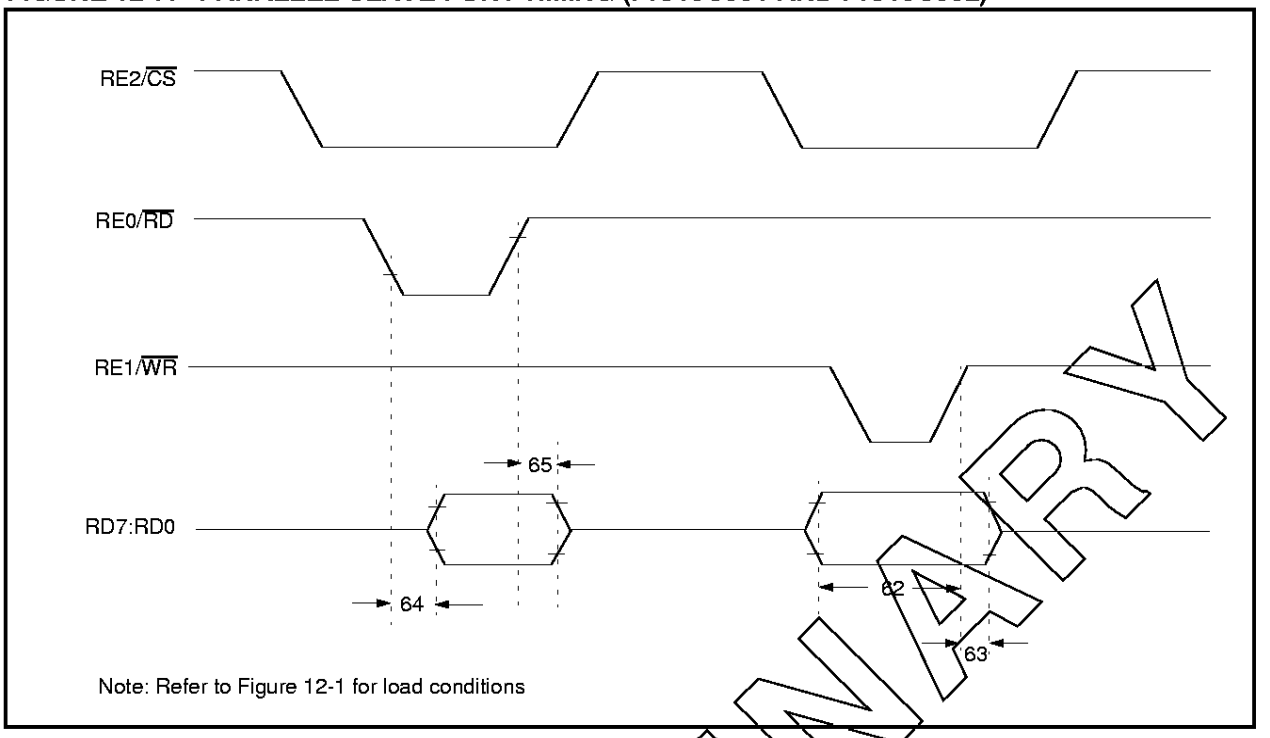


TABLE 12-8: PARALLEL SLAVE PORT REQUIREMENTS (PIC16C661 AND PIC16C662)

Parameter No.	Sym	Characteristic		Min	Typ†	Max	Units	Conditions
62	TdtV2wrH	Data in valid before WR↑ or CS↑ (setup time)		20	—	—	ns	
63*	TwrH2dtI	WR↑ or CS↑ to data–in invalid (hold time)	PIC16C66X	20	—	—	ns	
			PIC16LC66X	35	—	—	ns	
64	TrdL2dtV	RD↓ and CS↓ to data–out valid		—	—	80	ns	
65	TrdH2dtI	RD↑ or CS↓ to data–out invalid		10	—	30	ns	

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

