Ordering number : EN7619

Discontinued

SANYO Semiconductors
DATA SHEET

Monolithic Linear IC

LA5679T — 3ch Switching Regulator Control IC

Overview

The LA5679T is an 3ch switching regulator control IC.

Functions

- Operable on low voltage, min 1.8V.
- OUT1 to drive an external PNP.
- OUT2 to 3 to drive an external NPN.
- 3ch independent standby circuit incorporated.
- Reference voltage accuracy ±1%.
- MOS transistor driving possible.

Specifications

Absolute Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{CC} max		14	V
Allowable power dissipation	Pd max	Independent IC	0.4	W
Operating temperature	Topr		-20 to +85	°C
Storage temperature	Tstg		-55 to +150	°C

Operating Conditions at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage 1	V_{CC}		1.8 to 11	V
Supply voltage 2	VBIAS		1.8 to 11	V
Output sync current	ISINK max		0 to 30	mA
Reference voltage output current	IREF		0 to 1	mA
Timing resistor	RT		3 to 30	kΩ
Timing capacity	CT		100 to 1000	pF
Triangular wave frequency	f_{OSC}		0.1 to 1	MHz

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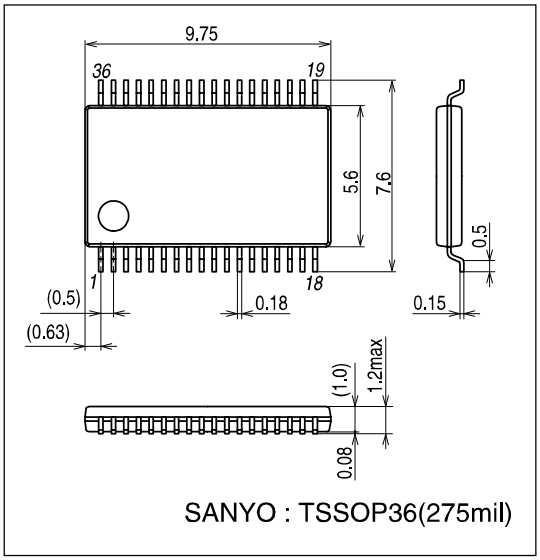
Electrical Characteristics at Ta = 25°C, V_{CC} = VSTBY1 to 3 = 3V, SCP = 0V

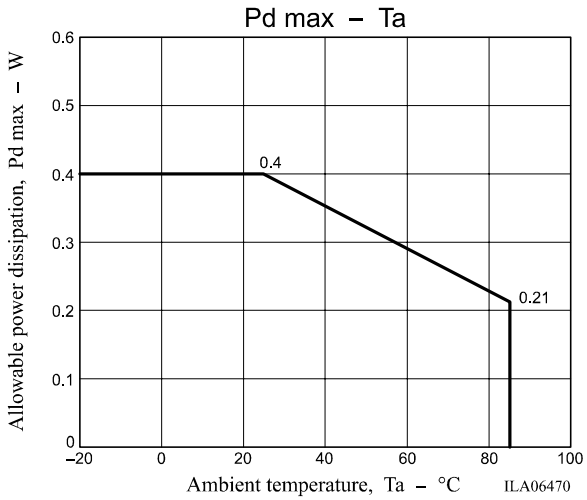
Parameter		Symbol	Conditions	Ratings			Unit
				min	typ	max	
[Error amplifier]							
IN+pin internal bias voltage		VB_IN+	IN2+, IN3+ pin	0.500	0.506	0.512	V
Output "Low" voltage	CH1	VLow_FB1	IN1- = 0.5V, IN1+ = 0V, IFB1 = 20µA			1	V
	CH2, CH3	VLow_FB2	IN2, 3- = 1V			0.2	V
Output "Hi" voltage	CH1	VHi_FB1	IN1- = 0.5V, IN1+ = 2V, IFB1 = -20µA	2.25			V
	CH2, CH3	VHi_FB2	IN2, 3- = 0V	0.81			V
Common-mode input voltage range	CH1	VICM_IN		0		2	V
[Protection circuit]							
Threshold voltage		VSCP		1.1	1.25	1.4	V
[SCP pin current]		ISCP			3.8		µA
[Still period adjusting section]							
Input bias current		IB_DTC		-15	-3		µA
Threshold voltage 1	CH1	VTH1_DTC	FB1 = 0.5V Duty cycle = 100%	0.35	0.4	0.45	V
Threshold voltage 2	CH1	VTH2_DTC	FB1 = 0.5V Duty cycle = 0%	0.67	0.77	0.87	V
Threshold voltage 3	CH2, CH3	VTH3_DTC	FB2, 3 = 1V Duty cycle = 100%	0.80	0.88	0.96	V
Threshold voltage 4	CH2, CH3	VTH4_DTC	FB2, 3 = 1V Duty cycle = 0%	0.40	0.45	0.50	V
[Output block 1 (ch1)]							
OUT pin source current		$I_{OUT}1$_SOUR	FB1 = 2V, DTC1 = 0V, RSET1 = 3.3Ω, $V_{OUT}1$ = 2.7V, ICAPH = 0.5mA	10			mA
OUT pin sync current		$I_{OUT}1$_SINK	FB1 = 0.5V, DTC1 = 0V, RSET1 = 3.3Ω, $V_{OUT}1$ = 2.3V	20	30	40	mA
ISET pin voltage		VISET	FB1 = 0.5V, DTC1 = 0V, RSET1 = 3.3Ω, $V_{OUT}1$ = 2.3V	0.065	0.1	0.135	V
[Output block 2 to 3 (ch2 to ch3)]							
OUT pin source current		$I_{OUT}23$_SOUR	RSET2, 3 = 680Ω, $V_{OUT}2$, 3 = 0.9V, DTC2, 3 = 1V, FB2, 3 = 1V	20	30	40	mA
OUT pin sync current		$I_{OUT}23$_SINK	RSET2, 3 = 680Ω, $V_{OUT}2$, 3 = 0.3V, DTC2, 3 = 1V, FB2, 3 = 0V	30			mA
OUT pin High voltage		$V_{OUT}23$_Hi	RSET2, 3 = 680Ω, $I_{OUT}2$, 3= -10mA, DTC2, 3 = 1V, FB2, 3 = 1V	2			V
OUT pin low voltage		$V_{OUT}23$_LOW	RSET2, 3 = 680Ω, $I_{OUT}2$, 3 = 10mA, DTC2, 3=1V, FB2, 3 = 0V			0.2	V
ISET pin voltage		VISET23	RSET2, 3 = 680Ω, $V_{OUT}2$, 3 = 0.9V, DTC2, 3 = 1V, FB2, 3 = 1V	0.230	0.350	0.470	V
[Triangular wave generator]							
Current setting pin voltage		VT_RT	RT = 5.6kΩ	1.190	1.260	1.330	V
Output current		I_{OH}_CT	VCT = 0.5V, RT = 5.6kΩ		230		µA
Output current ratio		ΔI_O_CT		0.8	1.0	1.2	
Oscillation frequency		$f_{OSC}1$		200	260	320	kHz
[Reference voltage block]							
Reference voltage		VREF	IREF = -1mA	1.244	1.257	1.270	V
Line regulation		VLN_REF	V_{CC} = 1.8V to 11V			10	mV
Load regulation		VLD_REF	IREF = -0.1mA to -1mA			10	mV
[STBY circuit]							
ON voltage		VON_STBY		1.15			V
OFF voltage		VOFF_STBY				0.2	V
Pin input current		I_{IN}_STBY	VSTBY1 to 3 = 3V			70	µA
[All circuit]							
Operating current dissipation (I_{CC}+IBIAS1 to 3)		$I_{CC}1$	FB1 = 0.5V, FB2, 3 = 1V, DTC1 = 0V, DTC2, 3 = 1V, RSET2, 3 = 680Ω, RSET1 = 3.3Ω		12	15	mA
Standby current dissipation (I_{CC}+IBIAS1 to 3)		$I_{CC}2$	VSTBY1 to 3 = 0V			1	µA

Package Dimensions

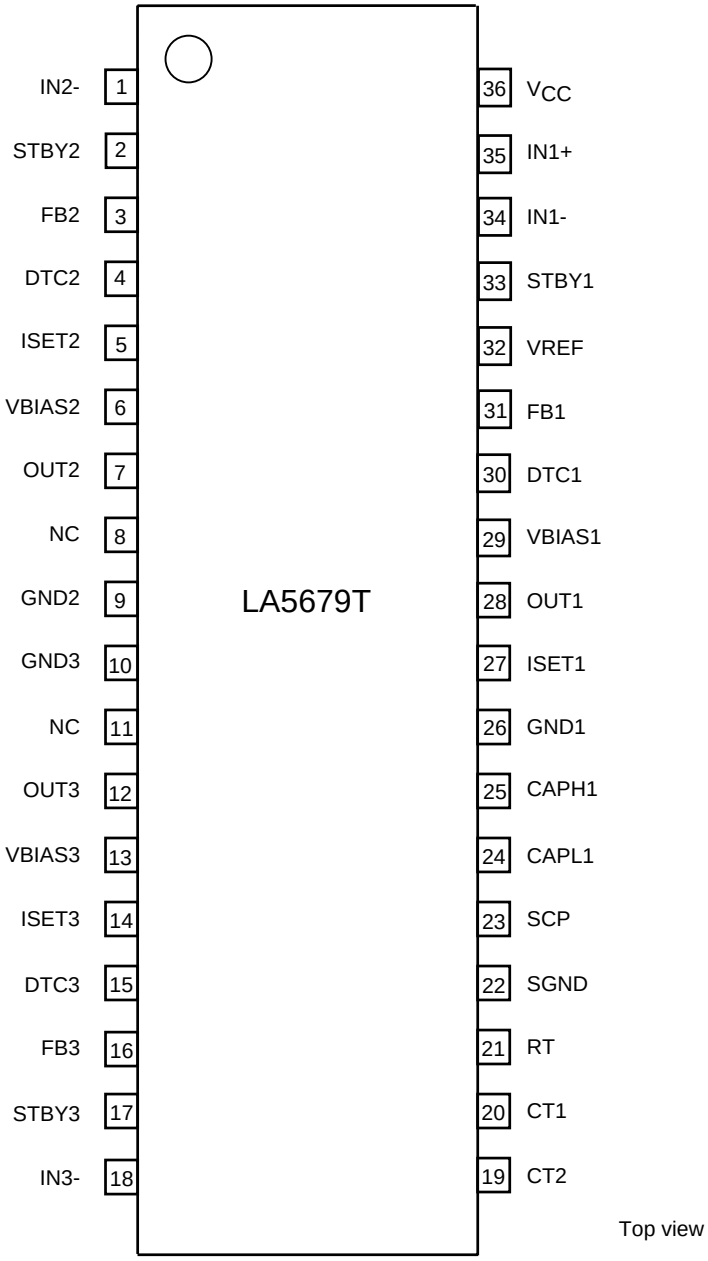
unit : mm

3253B



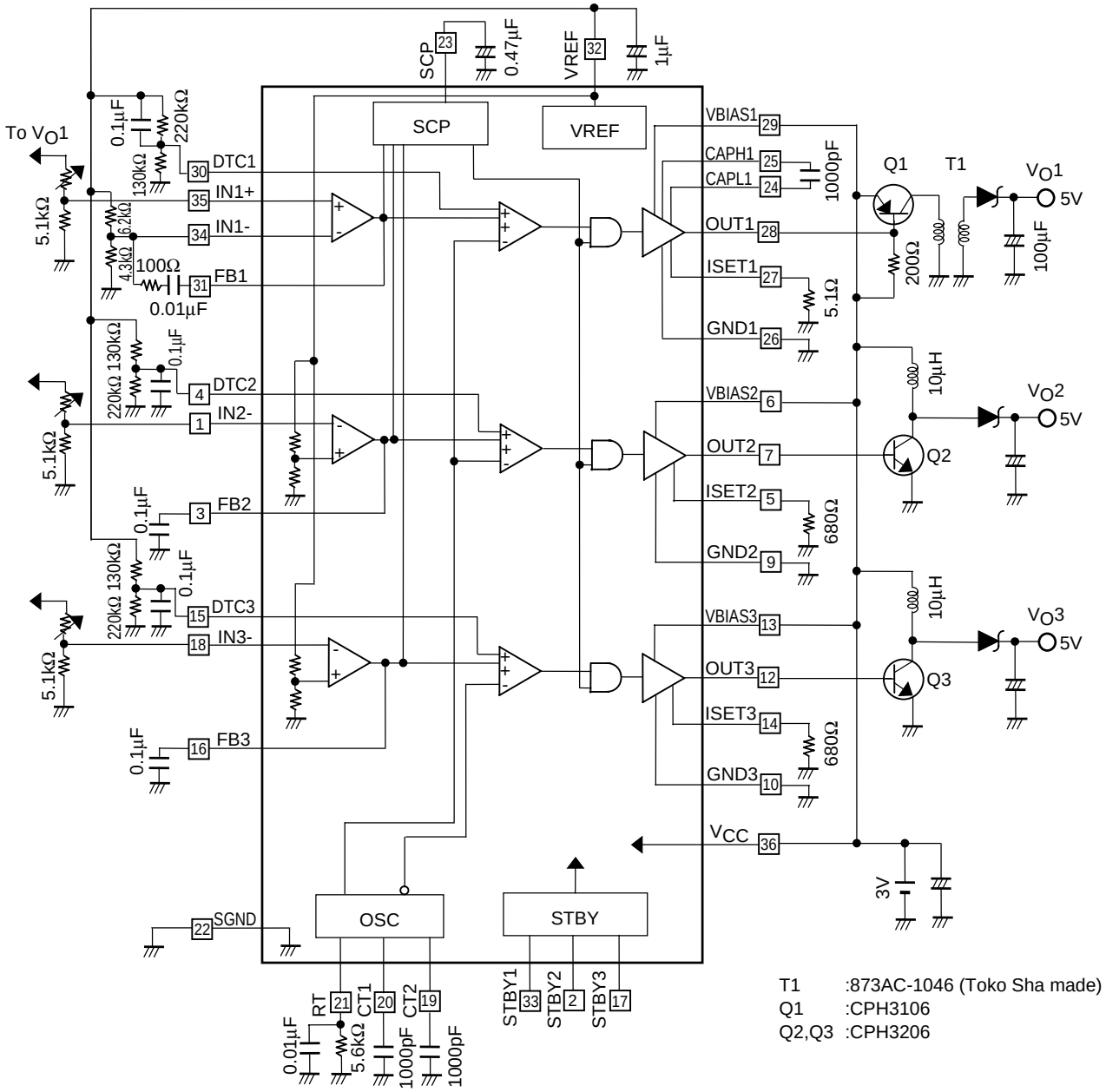


Pin Assignment



Top view

Block Diagram



T1 :873AC-1046 (Toko Sha made)
Q1 :CPH3106
Q2,Q3 :CPH3206

Note) Soft start of Ch2 and Ch3 may not occur in certain condition.
For details, refer to “Ch2 and Ch3 Soft Start” of the specification.

Output stage

(1) For Ch1

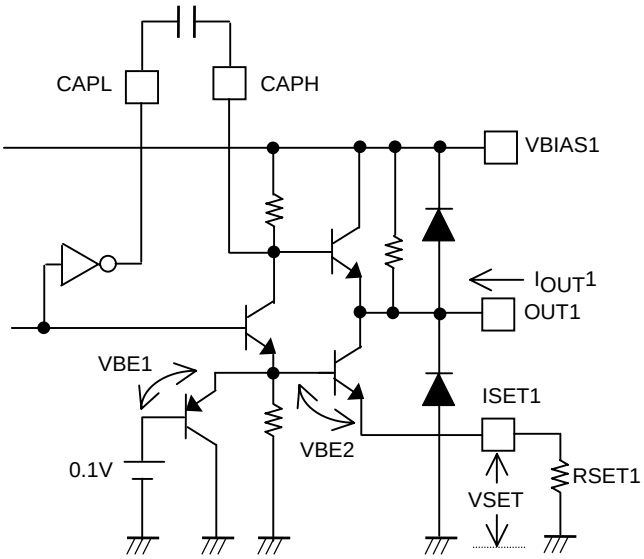
Output current $I_{OUT}1$ (sink) of Ch1 can be set freely by means of the resistance of ISET1 to GND and can be represented as follows:

$$I_{OUT}1 = \frac{0.1+VBE1-VBE2}{RSET2} \text{ [A]}$$

With VBE1 = VBE2,

$$I_{OUT}1 = \frac{0.1}{RSET2} \text{ [A]}$$

As VBE2 changes with $I_{OUT}1$ and thus VBE1 = VBE2 is not necessarily established, refer to the I_{OUT} (sink)-RSET characteristics for setting of RSET1.



$I_{OUT}1$ sink current

(2) For Ch2 (and for Ch3)

Output current $I_{OUT}2$ (source) can be set freely by means of the resistance of ISET2 to GND and can be represented as follows:

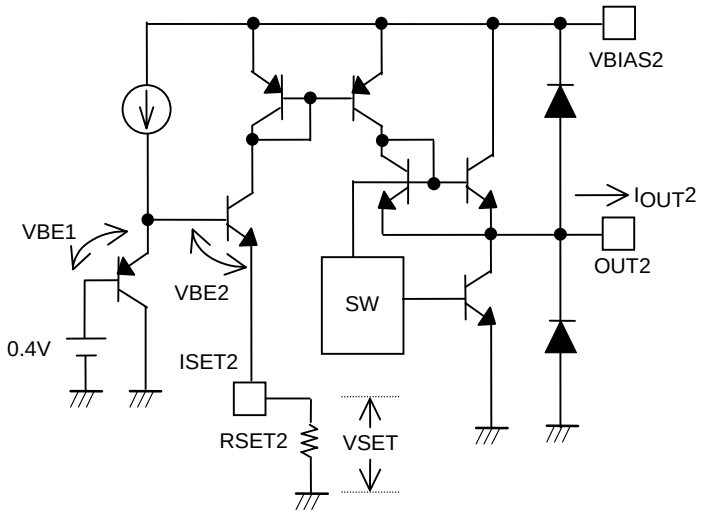
$$I_{OUT}2 = \frac{0.4+VBE1-VBE2}{RSET2} \times 61.4 \text{ [A]}$$

When VBE1=VBE2,

$$I_{OUT}2 = \frac{0.4}{RSET2} \times 61.4 \text{ [A]}$$

* The equation is for Ch2. The same applies to Ch3.

As VBE2 varies with ISET2, VBE1 is not always equal to VBE2. Besides, the current magnification of 61.4 varies slightly with VSET2 and $I_{OUT}2$. Refer to I_{OUT} (source)-RSET characteristic when setting RSET.

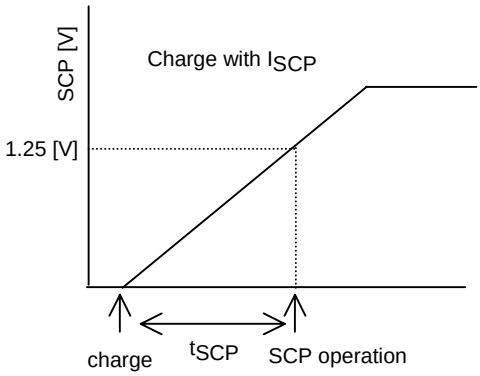


$I_{OUT}2$ source current

* Figure shows a case with Ch2 as well as a case with Ch3.

SCP pin

With FB1 being LOW (FB2 and 3 HI) because of load short-circuit, SCP charge begins. If FB1 is not reset within the set time, t_{SCP}, a protective circuit is activated. (The entire OUT is turned OFF when this circuit is activated.)



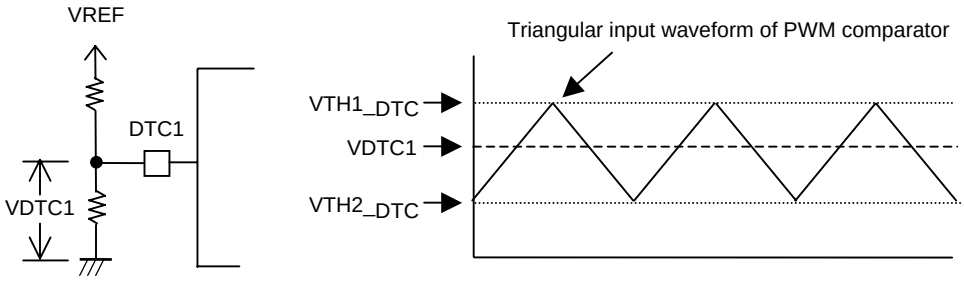
SCP charge

$$t_{SCP} = \frac{C_{SCP} \cdot V_{SCP}}{I_{SCP}} \quad [s]$$

Setting the dead time

(1) For Ch1

The dead time of Ch1 can be set with the DTC1 voltage.

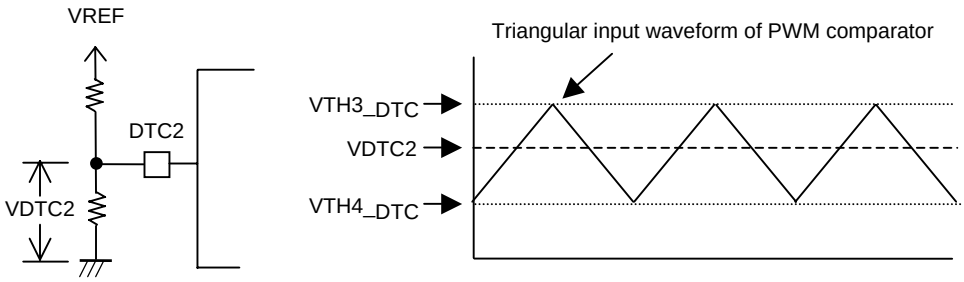


Duty D1 is represented as follows:

$$D1 = (1 - \frac{VDTC - VTH2\_DTC}{VTH1\_DTC - VTH2\_DTC}) \times 100\ [\%]$$

(2) For Ch2 (and Ch3)

The dead time of Ch2 can be set with the voltage of DTC2.



* Figure shows a case with Ch2 as well as a case with Ch3.

Duty D2 is represented as follows:

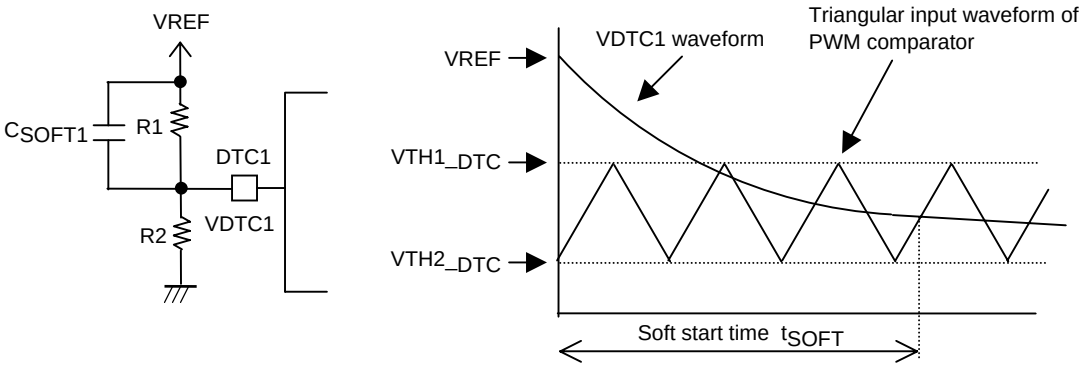
$$D2 = \frac{VDTC2 - VTH4\_DTC}{VTH3\_DTC - VTH4\_DTC} \times 100\ [\%]$$

* The equation is for Ch2. The same applies to Ch3.

Method to set the soft start time

(1) For Ch1

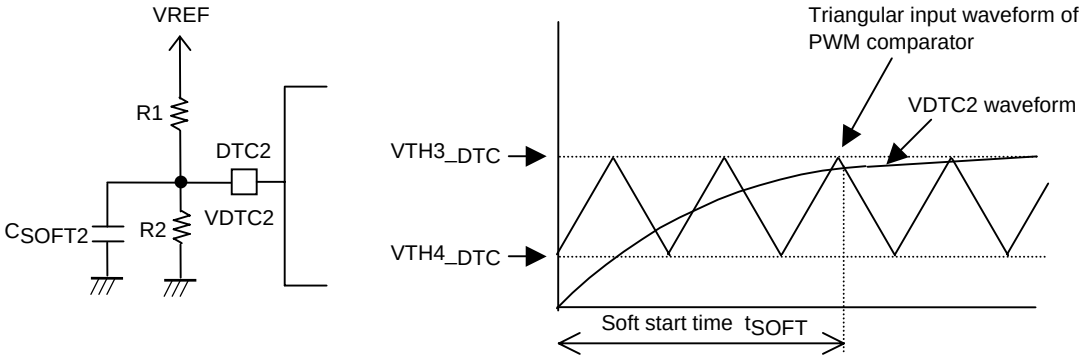
The Ch1 soft start time is set with a capacity connected between DTC pin and VREF.



$$t_{SOFT1} = \frac{C_{SOFT1} \cdot R1 \cdot R2}{R1+R2} \ln \frac{VDTC1 \cdot (R1+R2) - R2 \cdot VREF}{R1 \cdot VREF} \ [s]$$

(2) For Ch2 (and Ch3)

The Ch2 soft start time is set with a capacity connected between DTC2 and 3 pins and GND.



* Figure shows a case with Ch2 as well as a case with Ch3.

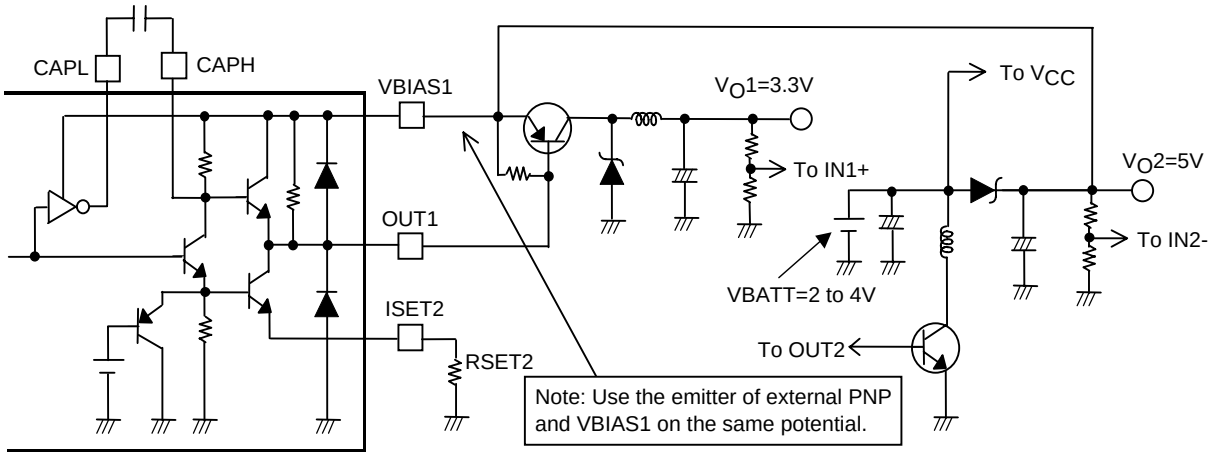
$$t_{SOFT2} = -C_{SOFT2} \cdot R2 \ln \left(1 - \frac{VDTC2}{VREF - VDTC2} \cdot \frac{R1}{R2}\right) \ [s]$$

* The equation is for Ch2. The same applies to Ch3.

Typical circuit using VBIAS1

As the power to the output stage is supplied with VBAIASI, the application shown in the figure can be made. The voltage of 5V stepped up with CH2 is applied to VBAIASI to obtain V_O1 = 3.3V. This is stepped up/down against the change of V_{CC} = 2 to 4V.

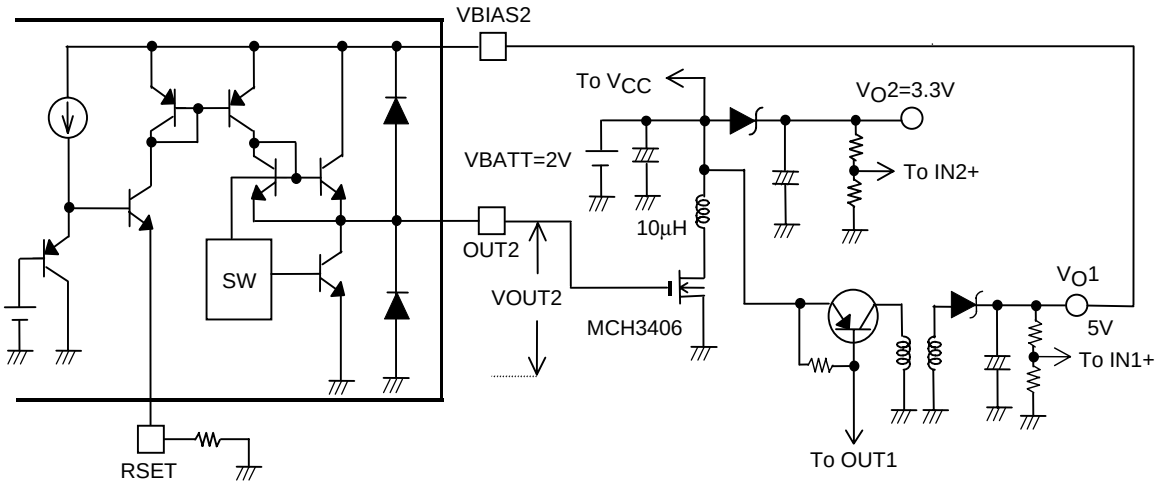
* Use the emitter of external PNP and VBAIS1 on the same potential.



Typical use of VBISA1

Typical circuit using VBIAS2 (and VBIAS3)

As the power to the output stage is supplied with VBAIAS2, the application shown in the figure can be made. The voltage of V_O1 = 5V stepped up with CH1 is applied to VBAIAS2. As the voltage of about VBIAS2-1V is generated, MOS transistor can be driven even when VBATT is low as shown in the typical circuit.



Typical VBIAS2 circuit

* Figure shows a case with VBIAS2 as well as for a case with VBIAS3.

During operation at low voltage (For V_{CC}, VBIAS1 to 3, 1.8 V or less)

A circuit to turn OFF the output when detecting V_{CC} and VBIAS1 to 3 during low voltage is not inserted. Turn OFF the output in STBY below the operation range.

CT1 and CT2

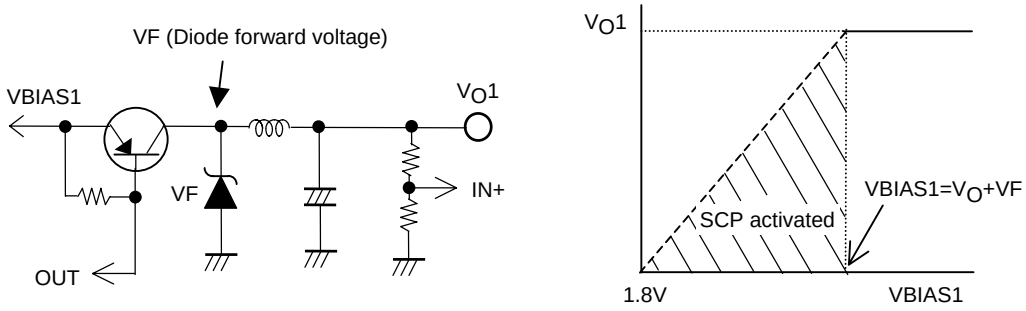
CT1 and CT2 have the waveform mutually displaced by 180 degrees in the phase. Independent frequency setting is impossible. Set the same value for capacitors to be connected, CT1 and CT2.

Relationship between short-circuit protection and soft start

The soft start condition is judged to be a short-circuit condition and charge to C_{SCP} is continued. Set the soft start time t_{SOFT} shorter than the set time t_{SCP} for short-circuit protection.

Use in the step-down circuit (ch1)

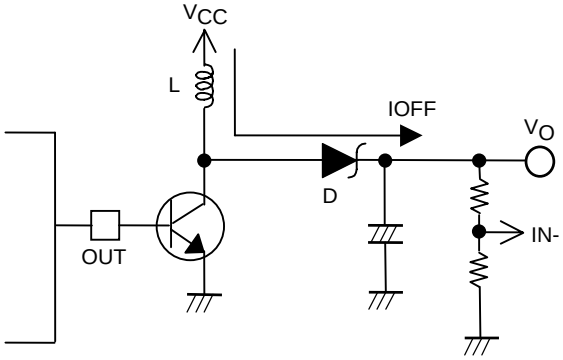
The step-down application as shown below is judged to be the short-circuit condition withVBIAS1 lower than the set voltage of V_O+VF and SCP is activated.



With VBIAS1<V_O+VF at step-down

Use of the step-up circuit (Ch2, Ch3)

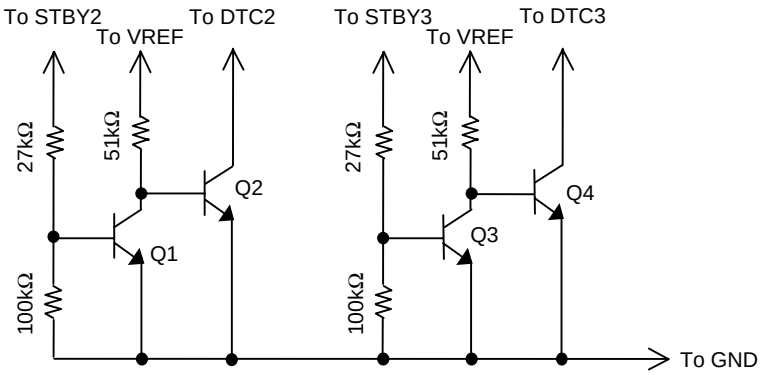
As shown in the figure, the step-up application forms a through via a V_{CC}→L→D route in the STBY OFF mode, so that the voltage remains in V_O. Similarly, the voltage remains in V_O in the SCP run mode. If necessary, cut off the through route with a switch.



When a chopper step-up circuit is used

Soft start of Ch2 and Ch3

Ch2 and Ch3 cannot perform soft start when VREF is started in advance because a DTC discharge circuit is not provided. Provide this discharge circuit.

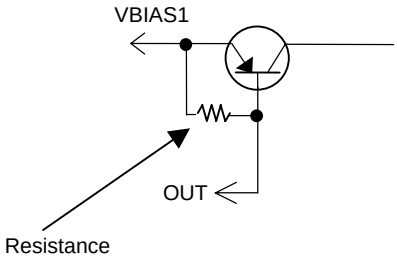


Set Q1 and Q3 to the threshold value of 0.89 V while assuming VBE = 0.7V.

Plan with an external DTC pin discharge circuit

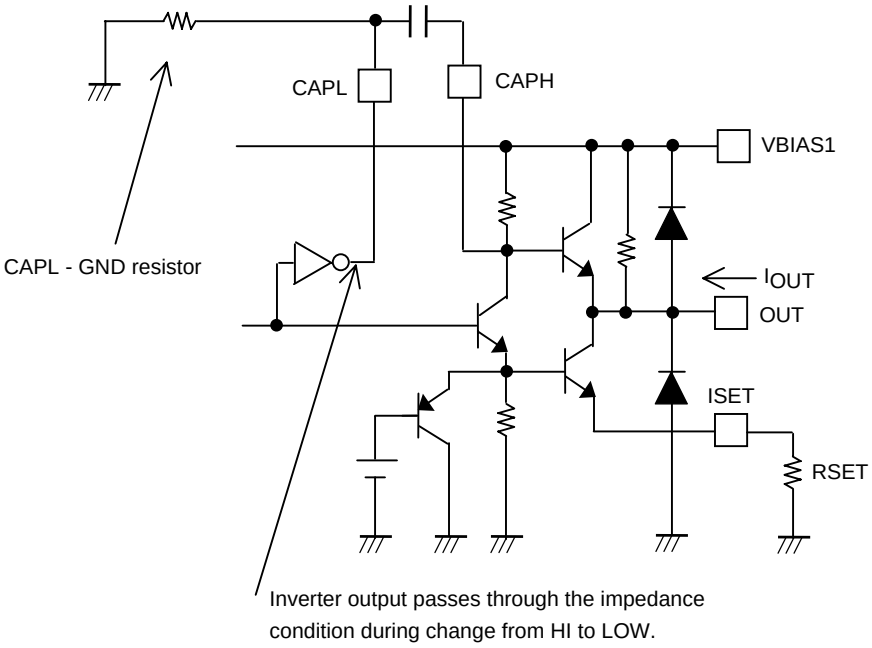
Resistance between the base and emitter of external PNP transistor (or between the gate and source in the case of MOS transistor)

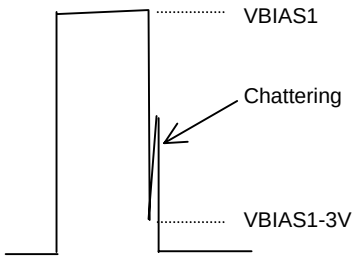
During light-load operation, the switching speed of transistor on the sink side of output stage is delayed, so that the external transistor cannot be turned OFF completely, resulting in increase in the current drain. Insert resistance between the base and emitter of external PNP transistor (or between the gate and source of MOS transistor) to ensure switching-off under light load and to prevent increase in the current drain.



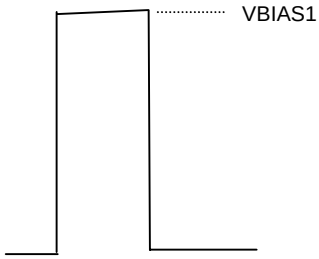
Resistance between CAPL and GND during MOS drive

V_{OUT} develops chattering with VBIAS1 at about -3V. This is considered due to the high impedance condition sensitive to noise in the course of change of the inverter output shown below from HI to LOW. Provide a resistor to CAPL - GND to improve the high impedance condition to eliminate chattering.





V_{OUT} waveform



V_{OUT} waveform
(Resistor between CAPL and GND)