

Dual Channel High CMR High Speed Hermetically Sealed Optocouplers

Technical Data

**6N134
6N134/883B
8102801EX**

Features

- Dual Marked with DESC Standard Military Drawing
- Manufactured and Tested on a MIL-STD-1772 Certified Line
- QML-MIL-H-38534, Class H
- Hermetically Sealed 16-pin Dual In-Line Package
- Performance Guaranteed Over -55°C to +125°C
- MIL-H-38534 Class H
- Internal Shield for Higher CMR; Selections Available
- 1500 Vdc Withstand Test Voltage
- High Radiation Immunity
- HCPL-2631, -56XX, -66XX Function Compatibility
- Reliability Data Available
- Space Level Processing Available
- Available with TXV or TXVB Part Marking

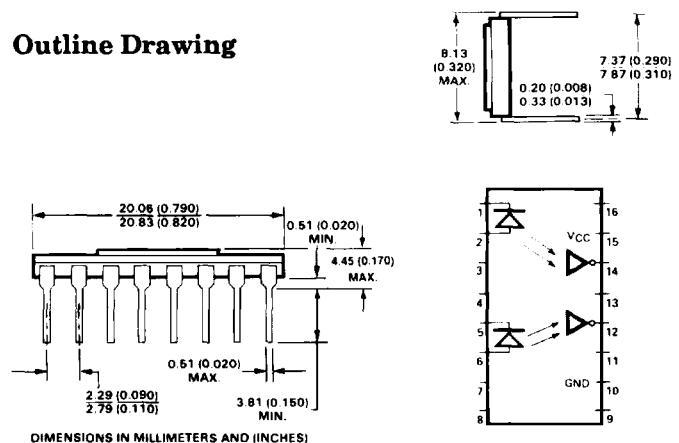
Description

The 6N134, 6N134/883B, and 8102801EX units are hermetically sealed, high CMR, high speed optocouplers. The products are capable of operation and storage over the full military temperature range and

can be purchased as either a standard product (6N134), with full MIL-H-38534 Class Level H testing (6N134/883B) or from the DESC Drawing 81028 as (8102801EX). All three products are dual channel in sixteen pin hermetic dual in-line packages. These parts are normally shipped with gold plated leads. They are also available with solder dipped leads by replacing C with A in the DESC part #, or by adding option #200 to the part number for 883B marked parts.

Each channel contains a GaAsP light emitting diode which is optically coupled to an integrated high speed photon detector. The output of the detector is an open collector Schottky clamped transistor. Internal shields provide a guaranteed common mode transient immunity specification of 1000 V/μs. Selection for higher CMR values are available by special request.

Outline Drawing



For Gull-wing or Butt-joint lead form options, contact your local Hewlett-Packard field representative.

This unique optocoupler design provides maximum dc and ac circuit isolation between each input and output while achieving TTL circuit compatibility. These optocouplers operate such that a minimum input current of 10 mA in each channel will sink a six gate fanout (10 mA) at the output with 4.5 to 5.5 V V_{CC} applied to the detector. This isolation and coupling is achieved with a typical propagation delay of 55 nsec.

The test program performed on the 8102801EX is in compliance with DESC Drawing 81028. The electrical characteristics table shows Group A Subgroup testing requirements from this drawing.

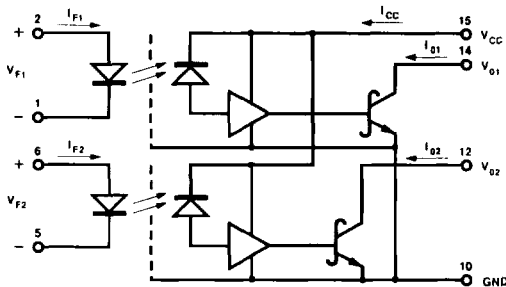
All devices are manufactured and tested on a MIL-STD-1772

certified line and are included in the DESC Qualified Manufacturers List (QML) in accordance with requirements for MIL-H-38534.

Applications

- Military/High Reliability Systems

Schematic



NOTE:
A 0.01 TO 0.1 μ F BYPASS CAPACITOR MUST BE CONNECTED BETWEEN PINS 15 AND 10.

- Transportation and Life Critical Systems
- Logic Ground Isolation
- Line Receiver
- Computer-Peripheral Interface
- Vehicle Command/Control Isolation
- Harsh Industrial Environments
- System Test Equipment Isolation

Absolute Maximum Ratings

| | |
|--|-------------------------------|
| Storage Temperature | -65°C to +150°C |
| Operating Temperature | -55°C to +125°C |
| Lead Temperature (soldering, 10 seconds) | +260°C |
| Junction Temperature (T_J) | +175°C |
| Peak Forward Input Current (each channel) | 40 mA (≤ 1 ms Duration) |
| Average Input Forward Current (each channel) | 20 mA |
| Input Power Dissipation (each channel) | 35 mW |
| Reverse Input Voltage (each channel) | 5 V |
| Supply Voltage - V_{CC} | 7 V (1 minute max.) |
| Output Current - I_O (each channel) | 25 mA |
| Output Power Dissipation (each channel) | 40 mW |
| Output Voltage - V_O (each channel) | 7 V* |
| Total Power Dissipation (both channels) | 350 mW |

*Selection for higher output voltages up to 20 V is available.

Recommended Operating Conditions

| Parameter | Symbol | Minimum | Maximum | Units |
|---|----------|---------|---------|-----------|
| Input Current, Low Level, Each Channel | I_{FL} | 0 | 250 | μ A |
| Input Current, High Level, Each Channel | I_{FH} | 12.5* | 16 | mA |
| Supply Voltage | V_{CC} | 4.5 | 5.5 | V |
| Fan Out (@ $R_L = 4$ k Ω), Each Channel | N | | 5 | TTL Loads |
| Operating Temperature | T_A | -55 | 125 | °C |

*12.5 mA condition permits at least 20% CTR degradation guardband. Initial switching threshold is 10 mA or less.

Electrical Specifications

| Test | Symbol | Conditions | Group A Sub-groups ⁽¹¹⁾ | Limits | | | Unit | Fig. | Note |
|---|-------------|--|------------------------------------|--------|--------|------|------------------|------|--------------|
| | | | | Min. | Typ.** | Max. | | | |
| Low Level Output Voltage | V_{OL}^* | $V_{CC} = 5.5 \text{ V}; I_F = 10 \text{ mA}$ $I_{OC} = 10 \text{ mA}$ | 1, 2, 3 | – | 0.4 | 0.6 | V | 4 | 1, 9 |
| Current Transfer Ratio | h_F CTR | $V_O = 0.6 \text{ V}; I_F = 10 \text{ mA}$ $V_{CC} = 5.5 \text{ V}$ | 1, 2, 3 | 100 | | – | % | | 1 |
| High Level Output Current | I_{OH}^* | $V_{CC} = 5.5 \text{ V}; V_O = 5.5 \text{ V}$ $I_F = 250 \mu\text{A}$ | 1, 2, 3 | – | 5 | 250 | $\mu\text{A dc}$ | | 1 |
| High Level Supply Current | I_{OCH}^* | $V_{CC} = 5.5 \text{ V}; I_{F1} = I_{F2} = 0 \text{ mA}$ | 1, 2, 3 | – | 18 | 28 | mA dc | | |
| Low Level Supply Current | I_{OCL}^* | $V_{CC} = 5.5 \text{ V}; I_{F1} = I_{F2} = 20 \text{ mA}$ | 1, 2, 3 | – | 26 | 36 | mA dc | | |
| Input Forward Voltage | V_F^* | $I_F = 20 \text{ mA}$ | 1, 2 | – | 1.55 | 1.75 | V dc | 1 | 1 |
| | | | 3 | – | | 1.85 | | | |
| Input Reverse Breakdown Voltage | V_{BR}^* | $I_R = 10 \mu\text{A}$ | 1, 2, 3 | 5.0 | | – | V dc | | 1 |
| Input to Output Insulation Leakage Current | $I_{i.o}^*$ | $V_{i.o} = 1500 \text{ V dc}$ Relative Humidity = 45% $t = 5 \text{ seconds}$ | 1 | – | | 1.0 | $\mu\text{A dc}$ | | 2, 10 |
| Capacitance Between Input/Output | $C_{i.o}$ | $f = 1 \text{ MHz}; T_C = 25^\circ\text{C}$ | 4 | – | | 4.0 | pF | | 3 |
| Propagation Delay Time, Low to High Output Level | t_{PLH}^* | $R_L = 510 \Omega; C_L = 50 \text{ pF}$ $I_F = 13 \text{ mA}$ | 9 | – | | 100 | ns | 2, 3 | 1, 5 |
| | | | 10, 11 | – | | 140 | | | |
| Propagation Delay Time, High to Low Output Level | t_{PHL}^* | $R_L = 510 \Omega; C_L = 50 \text{ pF}$ $I_F = 13 \text{ mA}$ | 9 | – | | 100 | ns | 2, 3 | 1, 6 |
| | | | 10, 11 | – | | 120 | | | |
| Output Rise Time | t_{LH} | $R_L = 510 \Omega$ $C_L = 50 \text{ pF};$ $I_F = 13 \text{ mA}$ | 9, 10, 11 | – | | 90 | ns | | |
| Output Fall Time | t_{HL} | | | – | | 40 | | | |
| Common Mode Transient Immunity at High Output Level | $ CM_H $ | $V_{CM} = 50 \text{ V (peak)};$ $V_O = 2 \text{ V minimum};$ $R_L = 510 \Omega;$ $I_F = 0 \text{ mA}$ | 9, 10, 11 | 1000 | 10000 | – | V μs | 6 | 1, 7, 11, 12 |
| Common Mode Transient Immunity at Low Output Level | $ CM_L $ | $V_{CM} = 50 \text{ V (peak)};$ $V_O = 0.8 \text{ V max.}$ $R_L = 510 \Omega;$ $I_F = 10 \text{ mA}$ | 9, 10, 11 | 1000 | 10000 | – | V μs | 6 | 1, 8, 11, 12 |

*For JEDEC registered parts.

**All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

Typical Specifications $T_A = 25^\circ\text{C}$, $V_{CC} = 5\text{ V}$ each channel

| Parameter | Symbol | Min. | Typ. | Max. | Units | Test Conditions | Fig. | Note |
|-------------------------------------|---------------------------------|------|-----------|------|----------------------|--|------|------|
| Input Capacitance | C_{IN} | | 60 | | pF | $V_F = 0$, $f = 1\text{ MHz}$ | | 1 |
| Input Diode Temperature Coefficient | $\frac{\Delta V_F}{\Delta T_A}$ | | -1.5 | | mV/ $^\circ\text{C}$ | $I_F = 20\text{ mA}$ | | 1 |
| Resistance (Input-Output) | $R_{I,O}$ | | 10^{12} | | Ω | $V_{I,O} = 500\text{ V}$ | | 3 |
| Input-Input Leakage Current | $I_{I,I}$ | | 0.5 | | nA | Relative Humidity = 45% $V_{I,I} = 500\text{ V}$, $t = 5\text{ s}$ | | 4 |
| Resistance (Input-Input) | $R_{I,I}$ | | 10^{12} | | Ω | $V_{I,I} = 500\text{ V}$ | | 4 |
| Capacitance (Input-Input) | $C_{I,I}$ | | 0.55 | | pF | $f = 1\text{ MHz}$ | | 4 |
| Output Rise Time (10-90%) | t_r | | 35 | | ns | $R_L = 510\ \Omega$, $C_L = 15\text{ pF}$ $I_F = 13\text{ mA}$ | | 1 |
| Output Fall Time (90-10%) | t_f | | 35 | | ns | | | |

Notes:

- Each channel.
- Measured between pins 1 through 8 shorted together and pins 9 through 16 shorted together.
- Measured between pins 1 and 2 or 5 and 6 shorted together, and pins 10, 12, 14 and 15 shorted together.
- Measured between pins 1 and 2 shorted together, and pins 5 and 6 shorted together.
- The t_{pLH} propagation delay is measured from the 6.5 mA point on the trailing edge of the input pulse to the 1.5 V point on the trailing edge of the output pulse.
- The t_{pHL} propagation delay is measured from the 6.5 mA point on the leading edge of the input pulse to the 1.5 V point on the leading edge of the output pulse.
- CM_{IH} is the max. tolerable common mode transient to assure that the output will remain in a high logic state (i.e., $V_o > 2.0\text{ V}$).
- CM_{IL} is the max. tolerable common mode transient to assure that the output will remain in a low logic state (i.e., $V_o < 0.8\text{ V}$).
- It is essential that a bypass capacitor (0.1 μF , ceramic) be connected from pin 10 to pin 15. Total lead length between both ends of the capacitor and the isolator pins should not exceed 20 mm.
- This is a momentary withstand test, not an operating condition.
- Standard parts receive 100% testing at 25°C (Subgroups 1 and 9). SMD and /883B parts receive 100% testing at 25, 125, and -55°C (Subgroups 1 and 9, 2 and 10, 3 and 11, respectively).
- Subgroups 10 and 11 shall be tested as part of device initial characterization and after design and process changes. Subgroups 10 and 11 shall be guaranteed to the limits specified in table I for all lots not specifically tested. Subgroup 9 shall be tested with every lot.

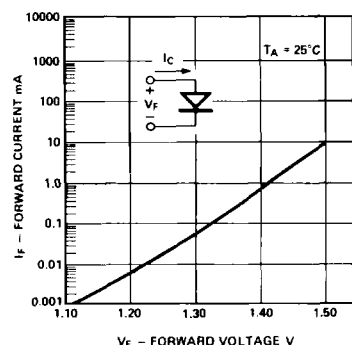
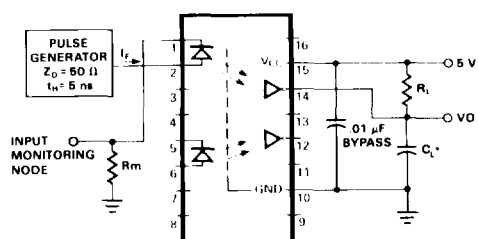


Figure 1. Input Diode Forward Current vs. Forward Voltage



* C_b INCLUDES PROBE AND STRAY WIRING CAPACITANCE.

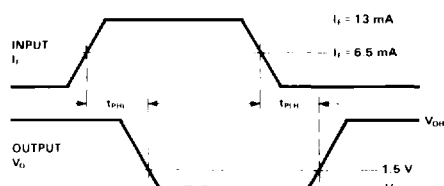


Figure 2. Test Circuit for t_{PRL} and t_{PLH} *

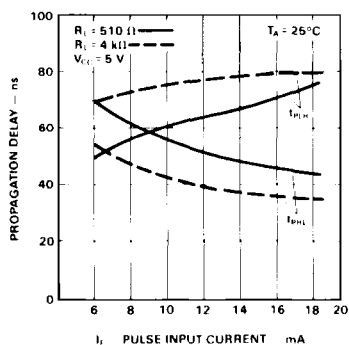


Figure 3. Propagation Delay, t_{PRL} and t_{PLH} vs. Pulse Input Current, I_i

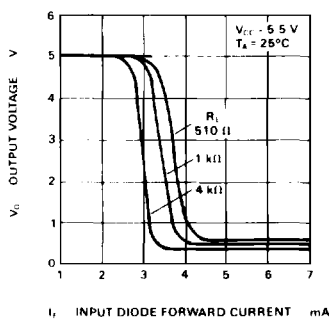
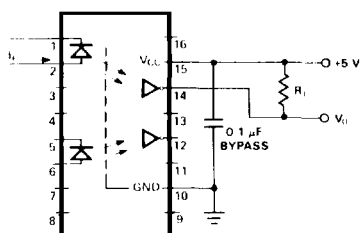


Figure 4. Input-Output Characteristics

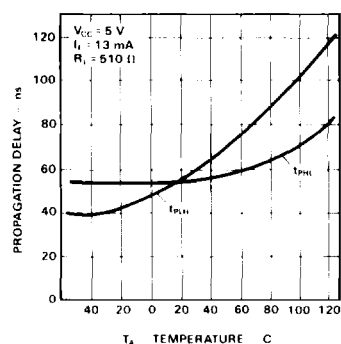


Figure 5. Propagation Delay vs. Temperature

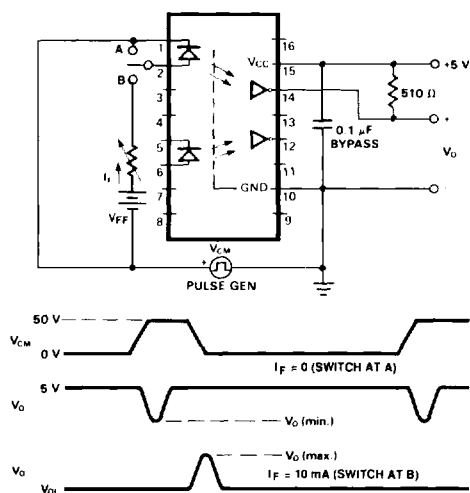


Figure 6. Typical Common Mode Rejection Characteristics/Circuit

8102801EC and MIL-H-38534 Class H Test Program

Hewlett-Packard's Hi-Rel Optocouplers are in compliance with MIL-H-38534 and DESC drawing 81028.

Testing consists of 100% screening and quality conformance to MIL-H-38534.

Part Numbering System

| Commercial Product | Class H Product | DESC Product | Class K Product |
|--------------------|-----------------|--------------|-----------------|
| 6N134 | 6N134/883B | 8102801EX | TBA |

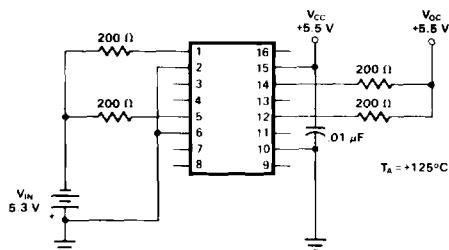


Figure 7. Operating Circuit for Burn-In and Steady State Life Tests

Part Marking Orientation for 6N134 Base Product and Related DESC Product

6N134
ESD Class 3

HP Logo →
Pin One/ →
ESD Ident

| |
|--------------------------|
| HP YYWWZ 6N134 USA |
|--------------------------|

← Date Code, Suffix (if needed)
← HP P/N
← Country of Mfr.

6N134/883B
8102801EX*
ESD Class 3

HP Logo →
HP P/N →
DESC SMD →
Country of Mfr. →
Pin One/ →
ESD Ident

| |
|--|
| HP QYYWWZ 6N134/883B 8102801EX USA 50434 |
|--|

← Compliance Indicator,
Date Code, Suffix (if needed)
← HP FSCN

6N134TXV
ESD Class 3

HP P/N →
Country of Mfr. →
Pin One/ →
ESD Ident

| |
|--|
| CHYYWWZ 6N134TXV USA HP 50434 |
|--|

← Compliance Indicator,
Date Code, Suffix (if needed)
← HP Logo
← HP FSCN

6N134TXVB
ESD Class 3

HP P/N →
Pin One/ →
ESD Ident

| |
|---|
| CHYYWWZ 6N134TXVB USA HP 50434 |
|---|

← Compliance Indicator,
Date Code, Suffix (if needed)
← HP Logo
← HP FSCN

**X" is not marked on device. Replace "X" with "C" for gold leads; replace "X" with "A" for solder dipped leads.