8-Bit Single Chip Microcontroller

SAB 80515 Microcontroller with factory mask-programmable ROM

SAB 80535 Microcontroller for external ROM

- 8K × 8 ROM (SAB 80515 only)
- 256 × 8 RAM
- Six 8-bit I/O ports, one 8-bit input port for analog signals
- Three 16-bit timer/counters
- Highly flexible reload, capture, compare capabilities
- Full-duplex serial channel
- Twelve interrupt vectors, four priority levels
- 8-bit A/D converter with eight multiplexed inputs and programmable internal reference voltages
- 16-bit watchdog timer
- V_{PD} provides standby current for 40 bytes of RAM
- Boolean processor
- 256 bit-addressable locations
- Most instructions execute in 1 µs
- 4 µs multiply and divide
- External memory expandable up to 128 Kbyte
- Backwardly compatible with SAB 8051
- 68-pin plastic leaded chip carrier package (PL-CC-68)
- Three temperature ranges available:
  0 to 70°C
  -40 to 85°C (T40/85)
  -40 to 110°C (T40/110)

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Figure 17
Logic Symbol

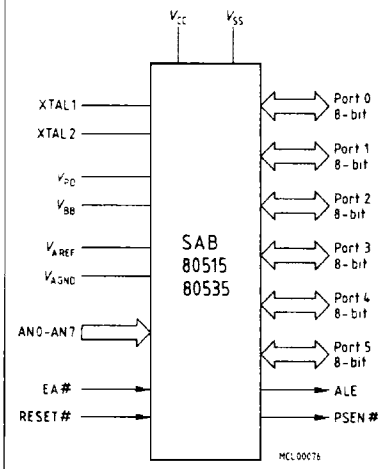
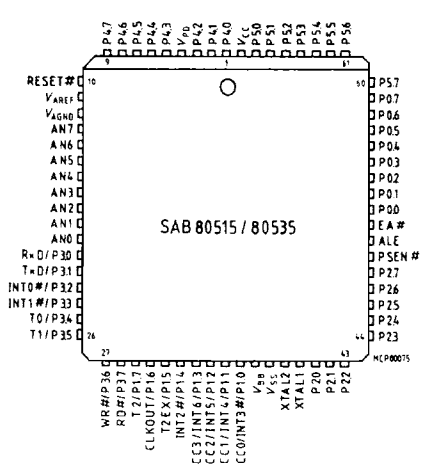


Figure 18
Pin Configuration (PL-CC-68)



The SAB 80515/80535 is a powerful member of the Siemens SAB 8051 family of 8-bit microcontrollers. It is fabricated in + 5 V N-channel, silicon-gate Siemens MYMOS technology. The SAB 80515/80535 is a stand-alone, high-performance single-chip microcontroller based on the SAB 8051 architecture. While maintaining all the SAB 8051 operating characteristics, the SAB 80515/80535 incorporates several enhancements which significantly increase design flexibility and overall system performance. The SAB 80535 is identical with the SAB 80515 except that it lacks the on-chip program memory. The SAB 80515/80535 is supplied in a 68-pin plastic leaded chip carrier package (P-LCC-68).

Ordering Information

Type	Description
SAB 80515-N	8-bit single-chip microcontroller with mask-programmable ROM
SAB 80535-N	for external memory
SAB 80515-N-T40/85	with mask-programmable ROM, EXT. Temperature
SAB 80535-N-40/85	for external memory, EXT. Temperature
SAB 80515-N-T40/110	with mask-programmable ROM, EXT. Temperature
SAB 80535-N-T40/110	for external memory, EXT. Temperature

Pin Definitions and Functions

Symbol	Pin	Input (I) Output (O)	Function
P4.0-P4.7	1-3, 5-9	I/O	Port 4 is an 8-bit quasi-bidirectional I/O port. Port 4 can sink/source 4 LS-TTL loads.
V_{PD}	4		Power down supply. If V_{PD} is held within its specs while V_{CC} drops below specs, V_{PD} will provide standby power to 40 byte of the internal RAM. When V_{PD} is low, the RAM's current is drawn from V_{CC}.
$\overline{\text{RESET}}$	10	I	A low level on this pin for the duration of two machine cycles while the oscillator is running resets the SAB 80515. A small internal pullup resistor permits power-on reset using only a capacitor connected to V_{SS}.
V_{AREF}	11		Reference voltage for the A/D converter
V_{AGND}	12		Reference ground for the A/D converter
AN7-AN0	13-20	I	Multiplexed analog inputs
P3.0-P3.7	21-28	I/O	Port 3 is an 8-bit quasi-bidirectional I/O port. It also contains the interrupt, timer, serial port and external memory strobe pins that are used by various options. The output latch corresponding to a secondary function must be programmed to a one (1) for that function to operate. Port 3 can sink/source 4 LS-TTL loads. The secondary functions are assigned to the pins of port 3, as follows: – RxD (P3.0): serial port's receiver data input (asynchronous) or data input/output (synchronous) – TxD (P3.1): serial port's transmitter data output (asynchronous) or clock output (synchronous) – $\overline{\text{INT0}}$ (P3.2): interrupt 0 input / timer 0 gate control input – $\overline{\text{INT1}}$ (P3.3): interrupt 1 input / timer 1 gate control input – T0 (P3.4): counter 0 input – T1 (P3.5): counter 1 input – $\overline{\text{WR}}$ (P3.6): the write control signal latches the data byte from port 0 into the external data memory – $\overline{\text{RD}}$ (P3.7): the read control signal enables the external data memory to port 0
P1.7-P1.0	29-36	I/O	Port 1 is an 8-bit quasi-bidirectional I/O port. It is used for the low-order address byte during program verification. It also contains the interrupt, timer, clock, capture and compare pins that are used by various options. The output latch must be programmed to a one (1) for that function to operate (except when used for the compare functions). Port 1 can sink/source 4 LS-TTL loads. The secondary functions are assigned to the port 1 pins, as follows: – $\overline{\text{INT3}}$/CC0 (P1.0): interrupt 3 input/compare 0 output/ capture 0 input – INT4/CC1 (P1.1): interrupt 4 input/compare 1 output/ capture 1 input – INT5/CC2 (P1.2): interrupt 5 input/compare 2 output/ capture 2 input – INT6/CC3 (P1.3): interrupt 6 input/compare 3 output/ capture 3 input

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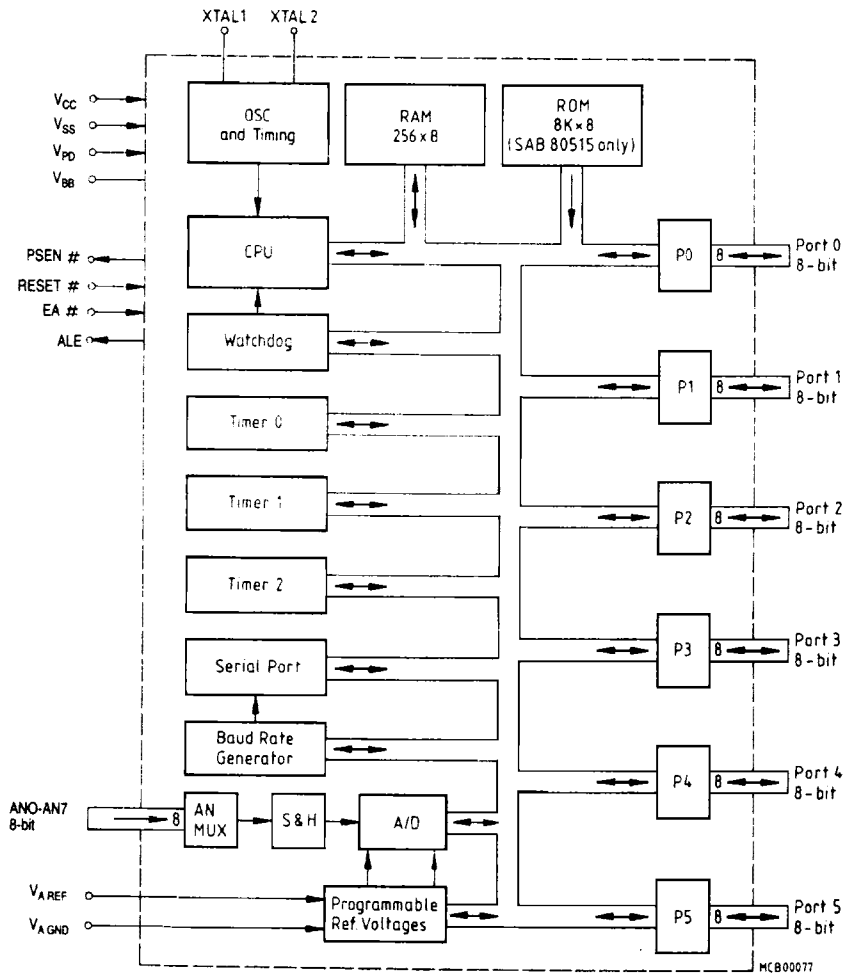
Pin Definitions and Functions (cont'd)

Symbol	Pin	Input (I) Output (O)	Function
P1.7-P1.0 (cont'd)			– $\overline{INT2}$ (P1.4): interrupt 2 input – T2EX (P1.5): timer 2 external reload trigger input – CLKOUT (P1.6): system clock output – T2 (P1.7): counter 2 input
V_{BB}	37		Substrate pin. Must be connected to V_{SS} through a capacitor (47 to 100 nF) for proper operation of the A/D converter.
XTAL2	39		XTAL2 is the output from the oscillator's amplifier.Input to the internal timing circuitry. A crystal, ceramic resonator, or external source can be used.
XTAL1	40		XTAL1 is the input to the oscillator's high gain amplifier. Required when a crystal or ceramic resonator is used. Connect to V_{SS} when external source is used on XTAL2.
P2.0-P2.7	41-48	I/O	Port 2 is an 8-bit quasi-bidirectional I/O port. It also emits the high-order address byte when accessing external memory. It is used for the high-order address and the control signals during program verification. Port 2 can sink/source 4 LS-TTL loads.
$\overline{PSEN}$	49	O	The program store enable output is a control signal that enables the external program memory to the bus during external fetch operations. It is activated every six oscillator periods except during external data memory accesses. Remains high during internal program execution.
ALE	50	O	Provides address latch enable output used for latching the address into external memory during normal operation. It is activated every six oscillator periods except during an external data memory access.
$\overline{EA}$	51	I	When held at a TTL high level, the SAB 80515 executes instructions from the internal ROM when the PC is less than 8192. When held at a TTL low level, the SAB 80515 fetches all instructions from external program memory. For the SAB 80535 this pin must be tied low.
P0.0-P0.7	52-59	I/O	Port 0 is an 8-bit open-drain bidirectional I/O port. It is also the multiplexed low-order address and data bus when using external memory. It is used for data output during program verification. Port 0 can sink/source 8 LS-TTL loads.
P5.7-P5.0	60-67	I/O	Port 5 is an 8-bit quasi-bidirectional I/O port. Port 5 can sink/source 4 LS-TTL loads.
V_{CC}	68		POWER SUPPLY (+ 5 V power supply during normal operation and program verification)
V_{SS}	38		GROUND (0 V)

Figure 19
Block Diagram



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Functional Description

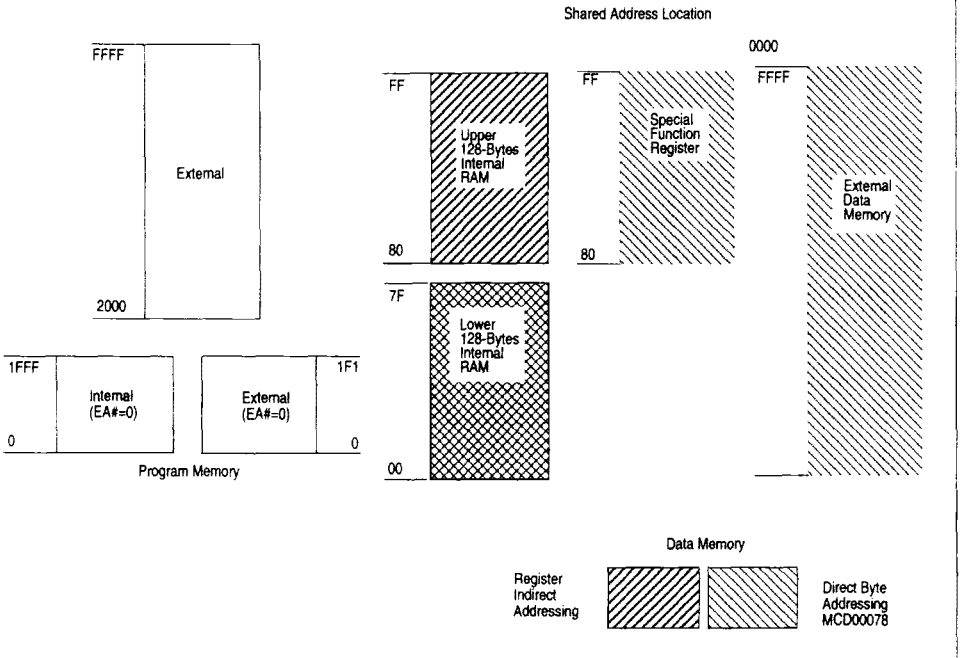
Principles of Architecture

The architecture of the SAB 80515 is based on the SAB 8051 microcontroller family. The following features of the SAB 80515 are fully compatible with the SAB 8051 features:

- Instruction set
- External memory expansion interface (port 0 and port 2)
- Full-duplex serial port
- Timer/counter 0 and 1
- Alternate functions on port 3
- The lower 128 bytes of internal RAM and the lower 4 Kbytes of internal ROM

The SAB 80515 additionally contains 128 bytes of internal RAM and 4 Kbytes of internal ROM, which results in a total of 256 bytes of RAM and 8 Kbytes of ROM on chip. The SAB 80515 has a new 16-bit timer/counter with a 2:1 prescaler, reload mode, compare and capture capability. It also contains a 16-bit watchdog timer, an 8-bit A/D converter with programmable reference voltages, two additional quasi-bidirectional 8-bit ports, one 8-bit input port for analog signals, and a programmable clock output ($f_{OSC}/12$).
Furthermore, the SAB 80515 has a powerful interrupt structure with 12 vectors and 4 programmable priority levels.
Figure 19 Block Diagram shows a block diagram of the SAB 80515.

Figure 20
Memory Address Spaces



Absolute Maximum Ratings

Ambient temperature under bias
SAB 80515/80535 ..... – 0 to +70°C
Storage temperature ..... – 65 to 150 °C
Voltage on any pin with respect
to ground (V_{SS}) .....– 0.5 to + 7 V
Power Dissipation .....2 W

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

V_{CC} = 5 V ± 10%; V_{SS} = 0 V; T_A = – 0 to + 70 °C; for SAB 80515/80535
T_A= – 40 to 85 °C; for SAB 80515/80535-T40/85
T_A= – 40 to 110 °C; for SAB 80515/80535-T40/110

Parameter	Symbol	Limit Values		Unit	Test Conditions
		min.	max.		
Input low voltage	V_{IL}	– 0.5	0.8	V	–
Input high voltage (except $\overline{RESET}$ and XTAL2)	V_{IH}	2.0	V_{CC} + 0.5	V	–
Input high voltage to XTAL2	V_{IH1}	2.5	V_{CC} + 0.5	V	XTAL 1 to V_{SS}
Input high voltage to $\overline{RESET}$	V_{IH2}	3.0	–	V	–
Power-down voltage	V_{PD}	3	5.5	V	V_{CC} = 0 V
Output low voltage, ports 1, 2, 3, 4, 5	V_{OL}	–	0.45	V	I_{OL} = 1.6 mA [1]
Output low voltage port 0, ALE, $\overline{PSEN}$	V_{OL1}	–	0.45	V	I_{OL} = 3.2 mA [1]
Output high voltage, ports 1, 2, 3, 4, 5	V_{OH}	2.4	–	V	I_{OH} = – 80 µA
Output high voltage port 0, ALE, $\overline{PSEN}$	V_{OH1}	2.4	–	V	I_{OH} = – 400 µA
Logic 0 input current ports 1, 2, 3, 4, 5	I_{IL}	–	– 800	µA	V_{IL} = 0.45 V
Logic 0 input current XTAL2	I_{IL2}	–	– 2.5	mA	XTAL1 = V_{SS} V_{IL} = 0.45 V
Input low current to $\overline{RESET}$ for reset	I_{IL3}	–	– 500	µA	V_{IL} = 0.45 V
Input leakage current to port 0, $\overline{EA}$, AN0 – AN7	I_{LI}	–	± 10	µA	0 V < V_{IN} < V_{CC}
Power supply current SAB 80515/80535 SAB 80515/80535- T40/85 SAB 80515/80535 - T40/110	 I_{CC} I_{CC} I_{CC}	 – – –	 210 230 230	 mA mA mA	All outputs disconnected
Power- down current	I_{PD}	–	3	mA	V_{CC} = 0 V
Capacitance of I/O buffer	C_{IO}	–	10	pF	f_c = 1 MHz

[1] Capacitive loading on ports 0 and 2 may cause spurious noise pulses to be superimposed on the VOL of ALE and ports 1, 3, 4, 5. The noise is due to external bus capacitance discharging into the port 0 and port 2 pins when these pins make 1-0 transactions during bus operation.

A/D Converter Characteristics

V_{CC} = 5 V ± 10%; V_{SS} = 0 V; V_{AREF} = V_{CC} = 5.0 V; V_{AGND} = V_{SS} = 0.0 V; $V_{IntAREF} - V_{IntAGND} \geq 1$ V;

Parameter	Symbol	Limit Values			Unit	Test Conditions
		min.	typ.	max.		
Analog input voltage	V_{AINPUT}	V_{AGND}- 0.2	–	V_{AREF+} 0.2	V	–
Analog input capacitance	C_I	–	25	–	pF	2)
Load time	t_L	–	–	2 t_{CY}	µs	–
Sample time (incl. load time)	t_S	–	–	5 t_{CY}	µs	–
Conversion time (including sample time)	t_C	–	–	15 t_{CY}	µs	–
Differential non-linearity	DNLE	–	± 1/2	± 1	LSB	$V_{IntAREF}$ =
Integral non-linearity	INLE	–	± 1/2	± 1	LSB	$V_{AREF} = V_{CC}$
Offset error			± 1/2	± 1	LSB	$V_{IntAGND}$ =
Gain error			± 1/2	± 1	LSB	$V_{AGND} = V_{SS}$
Total unadjusted error	TUE		± 1	± 2	LSB	2)
V_{AREF} supply current	I_{REF}	–	–	5	mA	3)
Internal reference error	$V_{IntREFER}$	–	± 5	± 30	mV	3)

2) The internal resistance of the analog source must be low enough to assure full loading of the sample capacitance (C_1) during load time (t_L). After charging of the internal capacitance (C_1)in the load time (t_L) the analog input must be held constant for the rest of the sample time (t_S).

3) The differential impedance r_D of the analog reference voltage source must be less than 1 kΩ at reference supply voltage.

AC Characteristics

V_{CC} = 5 V ± 10%; V_{SS} = 0 V;
T_A = 0 to + 70 °C; for SAB 80515/80535
T_A = -40 to + 85 °C; for SAB 80515/80535 - T40/85
T_A = -40 to + 110 °C; for SAB 80515/80535 - T40/110
(C_L for port 0, ALE and PSEN outputs = 100 pF; C_L for all other outputs = 80 pF)

Program Memory Characteristics

Parameter	Symbol	Limit Values				Unit
		12 MHz clock		Variable clock $1/t_{CLCL}$ = 1.2 MHz to 12 MHz		
		min.	max.	min.	max.	
Cycle time	t_{CY}	1000	–	$12t_{CLCL}$	–	ns
ALE pulse width	t_{LHLL}	127	–	$2t_{CLCL}-40$	–	ns
Address setup to ALE	t_{AVLL}	53	–	$t_{CLCL}-30$	–	ns
Address hold after ALE	t_{LAX1}	48	–	$t_{CLCL}-35$	–	ns
ALE to valid instruction in	t_{LLIV}	–	233	–	$4t_{CLCL}-100$	ns
ALE to $\overline{PSEN}$	t_{LLPL}	58	–	$t_{CLCL}-25$	–	ns
$\overline{PSEN}$ pulse width	t_{PLPH}	215	–	$3t_{CLCL}-35$	–	ns
$\overline{PSEN}$ to valid instruction in	t_{PLIV}	–	150	–	$3t_{CLCL}-100$	ns
Input instruction hold after $\overline{PSEN}$	t_{PXIX}	0	–	0	–	ns
Input instruction float after $\overline{PSEN}$	t_{PXIZ}*)	–	63	–	$t_{mCLCL}-20$	ns
Address valid after $\overline{PSEN}$	t_{PXAV}*)	75	–	$t_{LCL}-8$	–	ns
Address to valid instruction in	t_{AVIV}	–	302	–	$5t_{CLCL}-115$	ns
Address float to $\overline{PSEN}$	t_{AZPL}	0	–	0	–	ns

*) Interfacing the SAB 80515 to devices with float times up to 75 ns is permissible. This limited bus contention will not cause any damage to port 0 drivers.

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External Data Memory Characteristics

V_{CC} = 5 V ± 10%; V_{SS} = 0 V;
T_A = 0 to + 70 °C; for SAB 80515/80535
T_A = -40 to + 85 °C; for SAB 80515/80535 - T40/85
T_A = -40 to + 110 °C; for SAB 80515/80535 - T40/110

Parameter	Symbol	Limit Values				Unit
		12 MHz Clock		Variable Clock $1/t_{CLCL}$ = 1,2 MHz to 12 MHz		
		min.	max.	min.	max.	
$\overline{RD}$ pulse width	t_{RLRH}	400	–	$6t_{CLCL}-100$	–	ns
$\overline{WR}$ pulse width	t_{WLWH}	400	–	$6t_{CLCL}-100$	–	ns
Address hold after ALE	t_{LLAX2}	132	–	$2t_{CLCL}-35$	–	ns
$\overline{RD}$ to valid data in	t_{RLDV}	–	252	–	$5t_{CLCL}-165$	ns
Data hold after $\overline{RD}$	t_{RHDX}	0	–	0	–	ns
Data float after $\overline{RD}$	t_{RHDZ}	–	97	–	$2t_{CLCL}-70$	ns
ALE to valid data in	t_{LLDV}	–	517	–	$8t_{CLCL}-150$	ns
Address to valid data in	t_{AVDV}	–	585	–	$9tn_{CLCL}-165$	ns
ALE to $\overline{WR}$ or $\overline{RD}$	t_{LLWL}	200	300	$3t_{CLCL}-50$	$3t_{CLCL}+50$	ns
Address to $\overline{WR}$ or $\overline{RD}$	t_{AVWL}	203	–	$4t_{CLCL}-130$	–	ns
$\overline{WR}$ or $\overline{RD}$ high to ALE high	t_{WHLH}	43	123	$tnCLCL-40$	$t_{CLCL}+40$	ns
Data valid to $\overline{WR}$ transition	t_{QVWX}	33	–	$t_{CLCL}-50$	–	ns
Data setup before $\overline{WR}$	t_{QVWH}	433	–	$7t_{CLCL}-150$	–	ns
Data hold after $\overline{WR}$	t_{WHQX}	33	–	$t_{CLCL}-50$	–	ns
Address float after $\overline{RD}$	t_{RLAZ}	–	0	–	0	ns

Figure 21
Program Memory Read Cycle

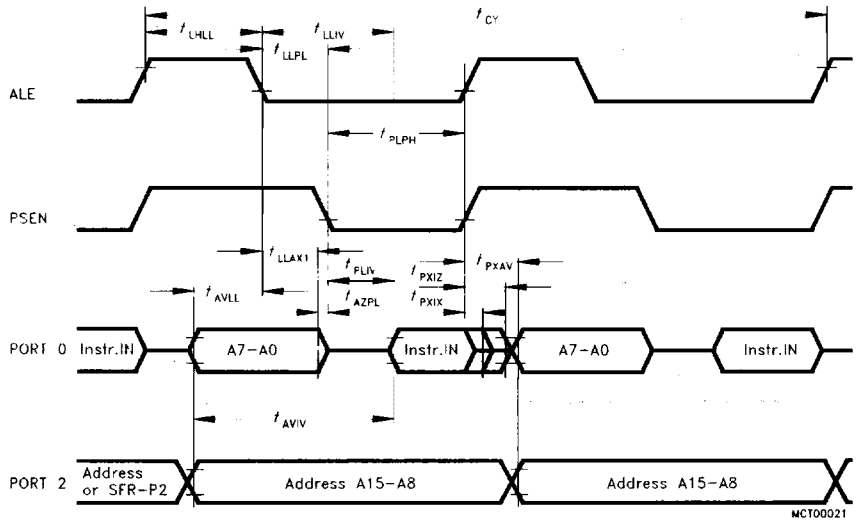


Figure 22
Data Memory Read Cycle

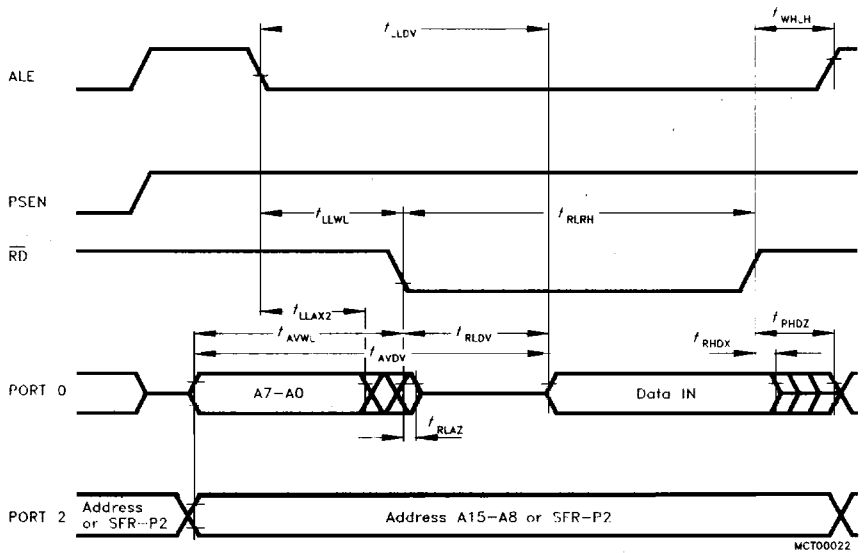


Figure 23
Data Memory Write Cycle

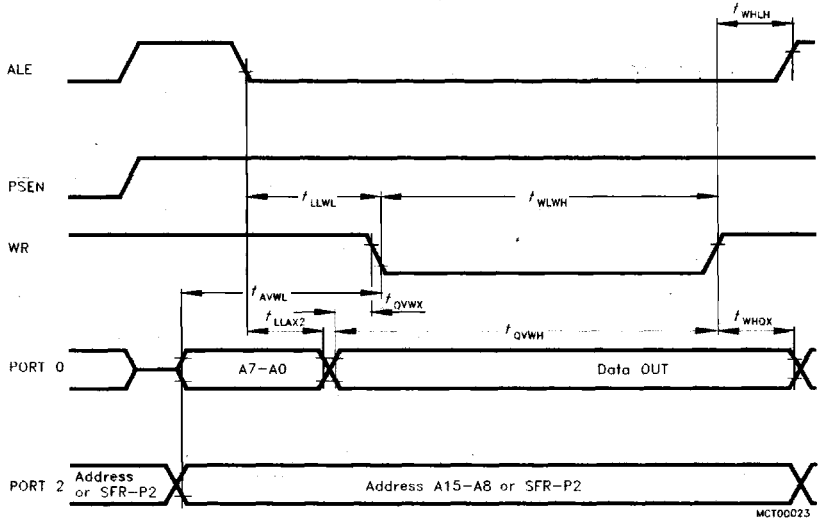
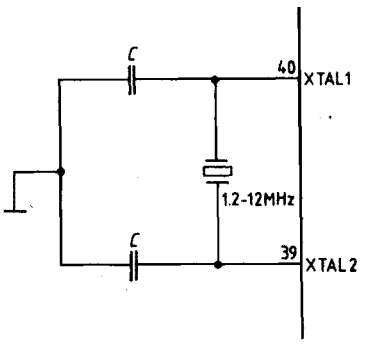
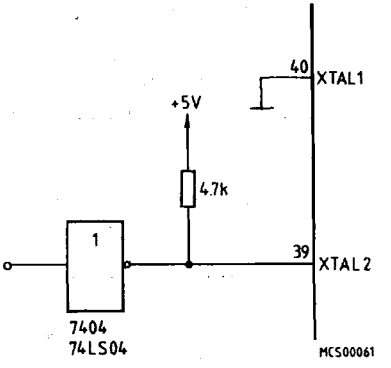


Figure 24
Recommended Oscillator Circuits



$C = 30pF \pm 10pF$

Crystal Oscillator Mode



Driving from External Source

External Clock Drive XTAL2

Parameter	Symbol	Limit Values		Unit
		Variable clock Freq = 1.2 MHz to 12 MHz		
		min.	max.	
Oscillator period	t_{CLCL}	83.3	833.3	ns
High time	t_{CHCX}	20	$t_{CLCL} - t_{CLCX}$	ns
Low time	t_{CLCX}	20	$t_{CLCL} - t_{CHCX}$	ns
Rise time	t_{CLCH}	–	20	ns
Fall time	t_{CHCL}	–	20	ns

Figure 25
External Clock Cycle

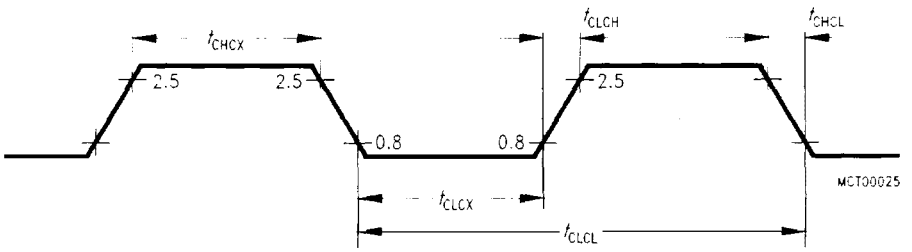
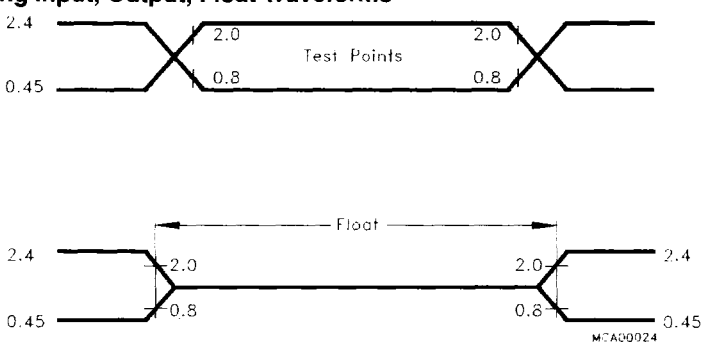


Figure 26
A.C. Testing Input, Output, Float Waveforms



A.C. testing inputs are driven at 2.4 V for a logic "1" and at 0.45 V for a logic "0".
Timing measurements are made at 2.0 V for a logic "1" and at 0.8 V for a logic "0".
For timing purposes, the float state is defined as the point at which a P0 pin sinks 3.2 mA or sources 400 µA at the voltage test levels.

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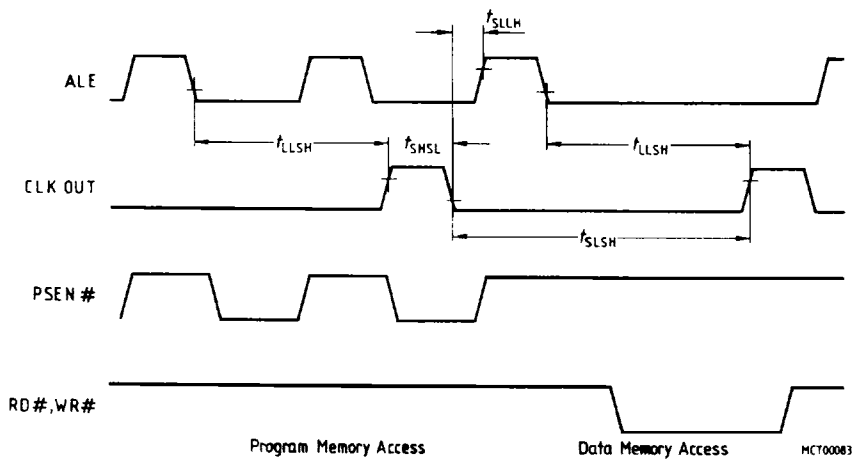
System Clock Timing

Parameter	Symbol	Limit Values				Unit
		12 MHz clock		Variable clock $1/t_{CLCL}$ = 1.2 MHz to 12 MHz		
		min.	max.	min.	max.	
ALE to CLKOUT	t_{LLSH}	543	–	$7t_{CLCL}-40$	–	ns
CLKOUT high time	t_{SHSL}	127	–	$2t_{CLCL}-40$	–	ns
CLKOUT low time	t_{SLSH}	793	–	$10t_{CLCL}-40$	–	ns
CLKOUT low to ALE high	t_{SLLH}	43	123	$t_{CLCL}-40$	$t_{CLCL}+40$	ns

Figure 27
System Clock Timing

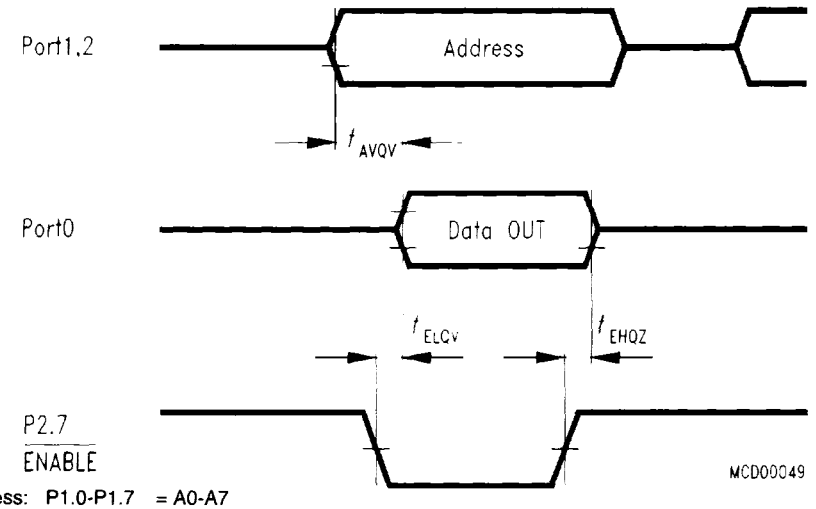


ROM Verification Characteristics

T_A = 25 °C ± °C; V_{CC} = 5 V ± 10%; V_{SS} = 0 V

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Address to valid data	t_{AVQV}	–	48 t_{CLCL}	ns
ENABLE to valid data	t_{ELQV}	–	48 t_{CLCL}	ns
Data float after ENABLE	t_{EHQZ}	0	48 t_{CLCL}	ns
Oscillator frequency	$1/t_{CLCL}$	4	6	MHz

Figure 28
ROM Verification



Address: P1.0-P1.7 = A0-A7
P2.0-P2.4 = A8-A12

Data: Port 0 = D0-D7

Inputs: P2.5-P2.6, $\overline{PSEN}$ = V_{SS}
ALE, $\overline{EA}$ = V_{IH}
$\overline{RESET}$ = V_{IL}

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