DRAM DIE

4 MEG DRAM

256K x 16

FEATURES

- Single 5.0V power supply
- Industry-standard timing and functions
- High-performance CMOS silicon-gate process
- All inputs, outputs and clocks are TTL- and CMOS-compatible
- Refresh modes: $\overline{RAS}$ ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$ (CBR), HIDDEN
- FAST PAGE MODE access cycle

GENERAL PHYSICAL SPECIFICATIONS

- Wafer thickness = 18.5 mils ±0.5 mils
- Backside wafer surface of polished bare silicon
- Typical metalization thickness 9K angstroms
- Metalization composition: 99.5% Al and 0.5% Cu over titanium
- Typical topside passivation 7.5K angstroms undoped oxide with 4K angstroms of nitride over oxide
- Typical pad openings: 4.4 x 4.4 mil
  111 x 111 µm

OPTIONS

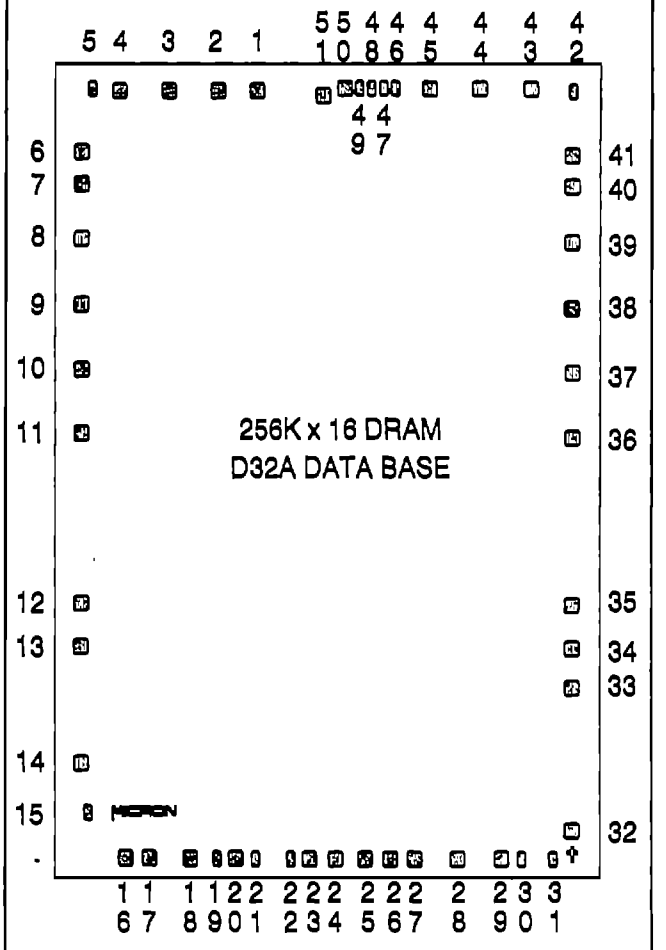
	ORDER NUMBER
• Speed probing	5V
No speed probing	None
60ns access	-6*
70ns access	-7*
80ns access	-8
• Form	
Die	D
Wafer (6" wafer)	W
• Testing levels	
Standard Probe	C1
Speed Probe	C2
PROBE$^{Plus™}$	C3
KGD$^{Plus®}$ (Known Good Die)	C7

*Not available as C1 level product.

ORDER INFORMATION

• 256K x 16	MT4C16257D32A

DIE OUTLINE (Top View)



Die size: 178 x 274 mil
4,521 x 6,960 µm
See Bond Pad Location and Identification Table.

PRODUCT #	DIE DATABASE	FORM	TESTING LEVEL	SPEED

MT4C16257D32ADC2-6

DIE TESTING PROCEDURES

Micron has established four testing levels for die products. Most Micron products are tested to Standard Probe (C1) level. Selected products are available as Speed Probe (C2) level. Customers especially concerned with reducing the infant mortality rate may choose the PROBE^{Plus} (C3) level. KGD^{Plus} (Known Good Die) (C7) level product is available on selected products as market demand dictates. Level C2, C3 and C7 products are designed to provide customers with improved yields over C1.

STANDARD PROBE (C1)

Micron probes wafers at a temperature with limits guardbanded to assure product performance from 0°C to 70°C in Micron's standard package. Since the package environment is not within Micron's control, the user must determine the necessary heat sinking requirements to ensure that the die junction temperature remains within specified limits. A high voltage functional stress test will be performed at probe to assure minimum junction breakdown integrity. V_{BB} (substrate bias voltage) is a forced condition at wafer probe.

Wafer probe consists of various functional and parametric tests of each die. Test patterns, timing, voltage margins, limits and test sequence are determined by individual product yields and reliability data.

Micron retains a wafer map of each wafer as part of the probe records along with a lot summary of wafer yields for each lot probed. Micron reserves the right to change the probe program at any time to improve the reliability, packaged device yield or performance of the product.

Die users may experience differences in performance relative to our data sheets. This is due to differences in package capacitance, inductance, resistance and trace length.

SPEED PROBE (C2)

In addition to the testing performed at Standard Probe (C1), Micron also offers Speed Probe (C2). Micron's Hot Chuck Speed Probe assures the speed performance of die products for the fastest speed grades. Speed Probe tests for most data sheet parameters, and may increase the yield over C1-level. C2-level die have not received burn-in, and are still subject to infant mortality failures.

PROBE^{Plus} (C3)

PROBE^{Plus} die incorporates all the testing done in the C2-level die as well as a burn-in step. The addition of the intelligent burn-in operates the parts until they have passed the infant mortality stage.

KGD^{Plus} (KNOWN GOOD DIE) (C7)

In order to provide the customer with fully warranted die product, Micron has developed a Known Good Die process designed to provide customers with die products of equal quality and reliability to packaged product. Micron's KGD^{Plus} process allows Micron to fully test and burn-in die product after it has been tested to C1 level.

FUNCTIONAL SPECIFICATIONS

Please refer to the packaged product data sheets found in the applicable Micron data book, for functional and parametric specifications. The specifications are provided for reference only on C1- and C2-level die product. On C2 and C3-level product ^{t}RAC and ^{t}CAC is guaranteed. C7-level product is warranted to the data sheet.

DIE AND WAFER LEVEL CONSIDERATIONS

Only C1- and C2-level products are available in wafer level form. PROBE^{Plus} die or KGD^{Plus} die are available only in die form. C2-level wafers are shipped with a user's wafer map indicating speed. Users should be aware that there may be multiple speed grades on wafers shipped with a C2 level.

BONDING INSTRUCTIONS

The D32A DRAM die has 51 bond pads. The redundant bond pads provide greater bonding flexibility in connecting the device to external components. Refer to the bond pad location and identification table for a complete list of bond pads and coordinates.

The D32A DRAM die has an internal substrate bias generator for normal operation. Bond pad 31 is used for manufacturing tests only. Normal bonding leaves bond pad 31 open (not bonded) or connected to the isolated substrate which is mounted. Micron recommends using a bond wire on each Vcc and Vss bond pad for improved noise immunity. In any event, all Vcc and Vss pads must be bonded. It is important that the back of the die be kept isolated from any other devices sharing a common package or substrate, since the die substrate is internally driven to a negative voltage.

WAFER SAW

Standard wafer saw cuts the die 100 percent through. Micron holds die dimensions to a maximum tolerance of +0/-1 mil of each cut, as measured from the vertical cut. For clarification purposes, the die size provided is measured from center to center of the die street. A finished die is approximately 1.5 mils smaller on each side due to the sawing operation. As an example, a 340 mil x 411 mil die is approximately 338.5 mil x 409.5 mil after sawing.

PACKAGING

For packaging, Micron utilizes Gel-Pak®. Additional information can be found in technical note TN-00-03, "Using Gel-Pak Trays with Micron Die." We package all die with the top metalization consistently oriented (refer to Figure 1). External packaging is suitable for electrostatic discharge protection. Each tray is individually self-locking or closed with a conductive clip and labeled with the following information:

- Generic device type and data base (Example: 16257D32A)
- Micron fabrication lot number
- Speed grade of the die (optional)
- Quantity of die in package

STORAGE REQUIREMENTS

Micron die products are packaged in a cleanroom environment for shipping. Upon receipt, the customer should transfer the Gel-Pak to a similar environment for storage. Micron recommends the die be maintained in a filtered nitrogen atmosphere until removed for assembly. The moisture content of the storage facility should be maintained at 30% ±10% relative humidity. ESD damage precautions are necessary during handling. The die must be in an ESD-protected environment at all times for inspection and assembly.

PRODUCT RELIABILITY MONITORS

Reliability of all products is monitored by ongoing QA reliability evaluations. Micron's QA department samples product families on a continuous basis for reliability studies. These studies include high temperature operating life (HTOL) tests for failure in time (FIT) calculations and high temperature steady state (HTSS) tests to monitor electromigration reliability. A summary of these product family evaluations is published on a regular basis.

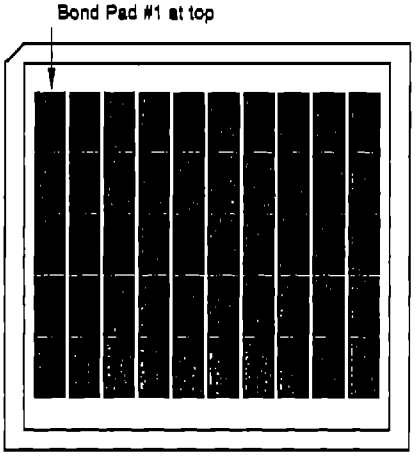
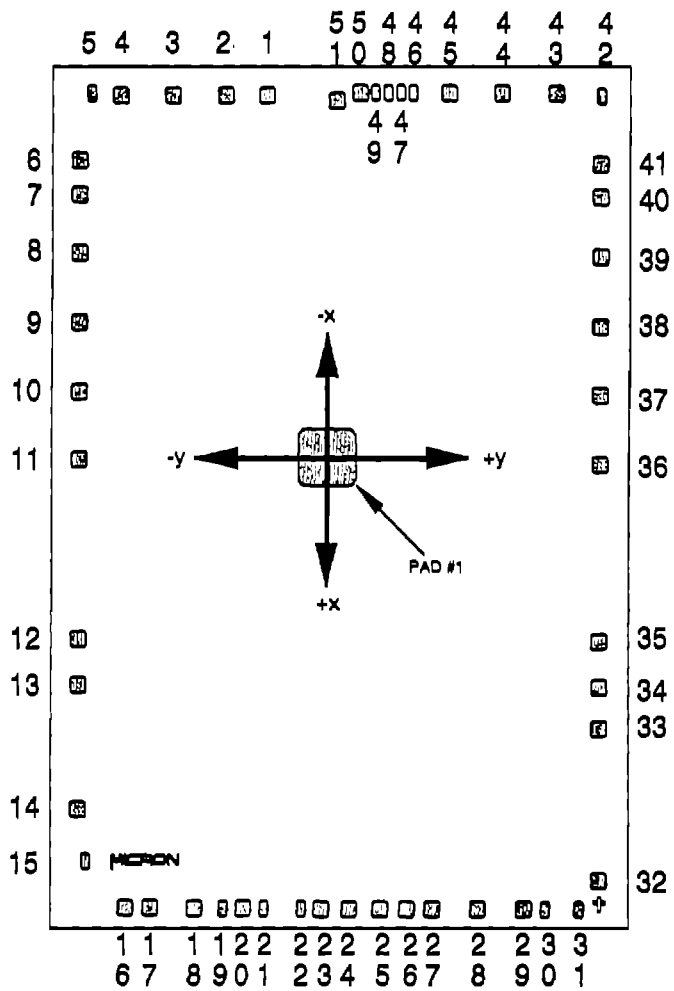


Figure 1
ORIENTATION OF DIE IN GEL-PAK

BOND PAD LOCATION AND IDENTIFICATION TABLE					
			FROM CENTER OF #1		
PAD #	MT4C16257	"X"[1] INCHES	"Y"[1] INCHES	"X"[2] MICRONS	"Y"[2] MICRONS
1	VccQ	0.000000	0.000000	0.0	0.0
2	DQ1	-0.000006	-0.013295	-0.1	-337.7
3	DQ2	-0.000006	-0.029816	-0.1	-757.3
4	DQ3	-0.000006	-0.046336	-0.1	-1176.9
5	DNU[1]	-0.000558	-0.055246	-14.2	-1403.3
6	DQ4	0.020098	-0.058446	510.5	-1484.5
7	VccQ	0.030589	-0.058441	777.0	-1484.4
8	DQ5	0.048745	-0.058446	1238.1	-1484.5
9	DQ6	0.070281	-0.058446	1785.1	-1484.5
10	DQ7	0.091816	-0.058446	2332.1	-1484.5
11	DQ8	0.113351	-0.058446	2879.1	-1484.5
12	$\overline{WE}$	0.171117	-0.058441	4346.4	-1484.4
13	$\overline{RAS}$	0.185735	-0.058441	4717.7	-1484.4
14	DNU	0.225993	-0.058441	5740.2	-1484.4
15	DNU	0.242660	-0.055814	6163.6	-1417.7
16	A0	0.258005	-0.043349	6553.3	-1101.1
17	A1	0.258005	-0.035475	6553.3	-901.1
18	A2	0.258005	-0.021523	6553.3	-546.7
19	DNU	0.258005	-0.012643	6553.3	-321.1
20	A3	0.258005	-0.006320	6553.3	-160.5
21	DNU	0.258005	0.000189	6553.3	4.8
22	DNU	0.258005	0.011782	6553.3	299.3
23	Vcc	0.258005	0.017977	6553.3	456.6
24	Vcc	0.257549	0.026897	6541.6	683.2
25	Vss	0.258005	0.036767	6553.3	933.9
26	A4	0.258005	0.044660	6553.3	1134.4
27	A5	0.258005	0.052537	6553.3	1334.4
28	A6	0.258005	0.066666	6553.3	1693.3
29	A7	0.258005	0.080946	6553.3	2056.0
30	DNU	0.258005	0.087524	6553.3	2223.1
31	V_{BB}	0.258005	0.097583	6553.3	2478.6
32	A8	0.248600	0.103714	6314.4	2634.3
33	$\overline{OE}$	0.199476	0.103525	5066.7	2629.5
34	$\overline{CASH}$	0.186081	0.103525	4726.5	2629.5
35	$\overline{CASL}$	0.171122	0.103525	4346.5	2629.5
36	DQ9	0.113728	0.103530	2888.7	2629.7
37	DQ10	0.092193	0.103530	2341.7	2629.7
38	DQ11	0.070658	0.103530	1794.7	2629.7
39	DQ12	0.049122	0.103530	1247.7	2629.7
40	VssQ	0.030531	0.103530	775.5	2629.7
41	DQ13	0.020639	0.103528	524.2	2629.6
42	DNU	-0.000401	0.103466	-10.2	2628.0
43	DQ14	-0.001149	0.089735	-29.2	2279.3
44	DQ15	-0.001149	0.073215	-29.2	1859.7
45	DQ16	-0.001149	0.056695	-29.2	1440.1
46	DNU	-0.001046	0.045484	-26.6	1155.3
47	DNU	-0.001046	0.041486	-26.6	1053.7
48	DNU	-0.001046	0.037488	-26.6	952.2
49	DNU	-0.001046	0.033490	-26.6	850.6
50	VssQ	-0.001149	0.028779	-29.2	731.0
51	Vss	0.001406	0.021418	35.7	544.0

NOTE: 1. DNU stands for "do not use"
2. Reference to center of each bond pad from center of Bond Pad #1.

DIE OUTLINE (Top View)



Wafer diameter: 150mm
Wafer thickness: 18.5 mil ±0.5 mil
Die size: 178 x 274 mil
(stepping interval)
4,521 x 6960 µm
Bond pad size: 5.3 x 5.3 mil
134 x 134 µm
Passivation Openings (typical): 4.4 x 4.4 mil
111 x 111 µm