4 194 304 x 9-Bit Dynamic RAM Module — HYM 94000S-80/-10

Advance Information

- 4 194 304 words by 9-bit organization
- Fast access and cycle time
  80 ns access time
  160 ns cycle time (HYM 94000S-80)
  100 ns access time
  190 ns cycle time (HYM 94000S-10)
- Fast page mode capability with
  45 ns cycle time (HYM 94000S-80)
  55 ns cycle time (HYM 94000S-10)
- Single + 5 V (± 10 %) supply
- Low power dissipation
  max. 4455 mW active (HYM 94000S-80)
  max. 3960 mW active (HYM 94000S-10)
  CMOS 50 mW
  TTL 100 mW
- Common $\overline{CAS}$ control for eight common data-in and data-out lines
- Separate $\overline{CAS}$ control for ninth bit
- $\overline{CAS}$-before-$\overline{RAS}$ refresh, $\overline{RAS}$-only-refresh, Hidden-refresh
- Decoupling capacitors mounted on substrate
- All inputs, outputs and clocks fully TTL-compatible
- 30 pin Single in-Line Memory Module (L-SIM-30)
- Pin configuration and outline dimensions according to JEDEC MO-64-AD
- Utilizes nine 4 M × 1 DRAMs in 350 mil wide SOJ packages
- 1024 refresh cycles/16 ms

The HYM 94000S-80/-10 is a 4 Mbyte RAM module organized as 4 194 304 words by 9-bit in a 30-pin single-in-line package comprising nine HYB 541000 DRAMs in 350 mil wide SOJ-packages mounted together with nine 0.2 µF multilayer ceramic decoupling capacitors on a PC board.

Each HYB 541000 is described in the data sheet and is fully electrical tested and processed according to SIEMENS standard quality procedure prior to module assembly. After assembly onto the board, a further set of electrical tests is performed.

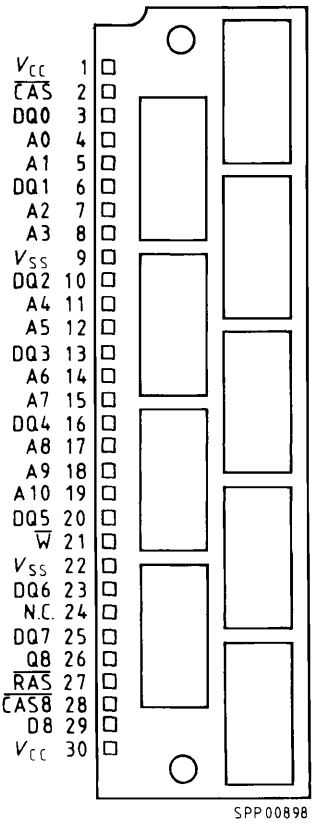
A common $\overline{CAS}$ controls for eight common data-in and data-out lines. Bit nine (D8, Q8) which is generally used for parity is controlled by $\overline{CAS8}$.

The common I/O feature on the HYM 94000S-80/-10 dictates the use of early write cycles to prevent contention on D and Q.

Ordering Information

Type	Ordering code	Package	Description
HYM 94000S-80	Q67100-Q460	L-SIM-30-950	DRAM Module (access time 80 ns)
HYM 94000S-10	Q67100-Q459	L-SIM-30-950	DRAM Module (access time 100 ns)

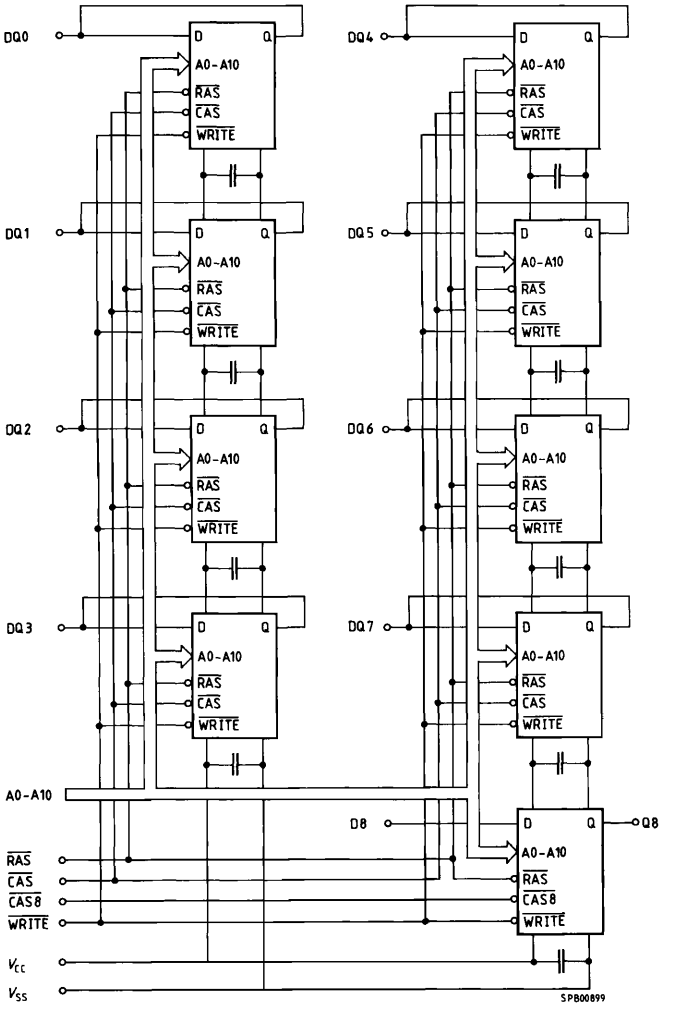
Pin Configuration



Pin Names

A0 - A10	Address Inputs
DQ0-DQ7	Data Input/Outputs
D8	Data Input
Q6	Data Output
$\overline{CAS}$	Column Address Strobe
$\overline{RAS}$	Row Address Strobe
$\overline{W}$	Read/Write Input
$\overline{CAS8}$	Column Address Strobe
V_{CC}	Power Supply (+ 5 V)
V_{SS}	Ground (0 V)
N.C.	No Connection

Block Diagram



Absolute Maximum Ratings

Operating temperature range ..... 0 to 70 °C
Storage temperature range ..... – 55 to 125 °C
Soldering temperature ..... 260 °C
Soldering time ..... 10 s
Input/output voltage ..... – 1 to + 7 V
Power supply voltage ..... – 1 to + 7 V
Power dissipation ..... 5.4 W
Data out current (short circuit) ..... 50 mA

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

T_A = 0 to 70 °C; V_{CC} = 5 V ± 10 %

Symbol	Parameter	Limit values		Unit	Test condition
		min.	max.		
V_{IH}	Input high voltage	2.4	6.5	V	1)
V_{IL}	Input low voltage	– 1.0	0.8	V	1)
V_{OH}	Output high voltage (I_{OUT} = – 5 mA)	2.4	–	V	–
V_{OL}	Output low voltage (I_{OUT} = 4.2 mA)	–	0.4	V	–
$I_{I(L)}$	Input leakage current (0 V ≤ V_{IN} ≤ 6.5 V, all other pins = 0 V)	– 20	+ 20	µA	–
$I_{O(L)}$	Output leakage current (DO is disabled, 0 V ≤ V_{OUT} ≤ 5.5 V)	– 20	+ 20	µA	–
I_{CC1}	Average V_{CC} supply current: HYM 94000S-80 HYM 94000S-10 ($\overline{RAS}$, $\overline{CAS}$, address cycling: t_{RC} = t_{RC} min.)	– –	810 720	mA mA	2) 3) 2) 3)
I_{CC2}	Standby V_{CC} supply current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	–	18	mA	–
I_{CC3}	Average V_{CC} supply current during $\overline{RAS}$-only refresh cycles: HYM 94000S-80 HYM 94000S-10 ($\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IH} = t_{RC} = t_{RC} min.)	– –	810 720	mA mA	2) 2)
I_{CC4}	Average V_{CC} supply current, during fast page mode: HYM 94000S-80 HYM 94000S-10 ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ address cycling: t_{PC} = t_{PC} min.)	– –	585 495	mA mA	2) 3) 2) 3)
I_{CC5}	Standby V_{CC} supply current: ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} – 0.2 V)	–	9	mA	–
I_{CC6}	Average V_{CC} supply current, during $\overline{CAS}$-before-$\overline{RAS}$-mode: HYM 94000S-80 HYM 94000S-10 ($\overline{RAS}$, $\overline{CAS}$ cycling: t_{RC} = t_{RC} min.)	– –	910 720	mA mA	2) 2)

Notes see page 161.

AC Characteristics [4) 5)]

T_A = 0 to 70 °C; V_{CC} = + 5 V ± 10 %; t_T = 5 ns

Symbol	Parameter	Limit values				Unit
		HYM 94000S-80		HYM 94000S-10		
		min.	max.	min.	max.	
t_{RC}	Random read or write cycle time	160	–	190	–	ns
t_{PC}	Fast page mode cycle time	45	–	55	–	ns
t_{RAC}	Access time from $\overline{RAS}$ [6) 11)]	–	80	–	100	ns
t_{CAC}	Access time from $\overline{CAS}$ [6) 11)]	–	20	–	25	ns
t_{AA}	Access time from column address [6) 12)]	–	40	–	50	ns
t_{CPA}	Access time from $\overline{CAS}$ precharge [6)]	–	40	–	50	ns
t_{CLZ}	$\overline{CAS}$ to output in low-Z [6)]	0	–	0	–	ns
t_{OFF}	Output buffer turn-off delay [7)]	0	20	0	30	ns
t_T	Transition time (rise and fall) [5)]	3	50	3	50	ns
t_{RP}	$\overline{RAS}$ precharge time	70	–	80	–	ns
t_{RAS}	$\overline{RAS}$ pulse width	80	10 000	100	10 000	ns
t_{RASP}	$\overline{RAS}$ pulse width (fast page mode)	80	200 000	100	200 000	ns
t_{RSH}	$\overline{RAS}$ hold time	20	–	25	–	ns
t_{CSH}	$\overline{CAS}$ hold time	80	–	100	–	ns
t_{CAS}	$\overline{CAS}$ pulse width	20	10 000	25	10 000	ns
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ delay time [11)]	20	60	25	75	ns
t_{RAD}	$\overline{RAS}$ to column address delay time [12)]	15	40	20	50	ns
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ precharge time	5	–	10	–	ns
t_{CP}	$\overline{CAS}$ precharge time (fast page mode)	10	–	10	–	ns
t_{ASR}	Row address setup time	0	–	0	–	ns
t_{RAH}	Row address hold time	10	–	15	–	ns
t_{ASC}	Column address setup time	0	–	0	–	ns
t_{CAH}	Column address hold time	15	–	20	–	ns
t_{AR}	Column address hold time referenced to $\overline{RAS}$	60	–	75	–	ns
t_{RAL}	Column address to $\overline{RAS}$ lead time	40	–	50	–	ns
t_{RCS}	Read command setup time	0	–	0	–	ns
t_{RCH}	Read command hold time [8)]	0	–	0	–	ns
t_{RRH}	Read command hold time referenced to $\overline{RAS}$ [8)]	0	–	0	–	ns
t_{WCH}	Write command hold time	15	–	20	–	ns

Notes see page 161.

AC Characteristics (cont'd) [4] [5]

Symbol	Parameter	Limit values				Unit
		HYM 94000S-80		HYM 94000S-10		
		min.	max.	min.	max.	
t_{WCR}	Write command hold time referenced to $\overline{RAS}$	60	–	75	–	ns
t_{WP}	Write command pulse width	15	–	20	–	ns
t_{RWL}	Write command to $\overline{RAS}$ lead time	15	–	25	–	ns
t_{CWL}	Write command to $\overline{CAS}$ lead time	15	–	25	–	ns
t_{DS}	Data setup time [9]	0	–	0	–	ns
t_{DH}	Data hold time [9]	15	–	20	–	ns
t_{DHR}	Data hold time referenced to $\overline{RAS}$	60	–	75	–	ns
t_{REF}	Refresh period	–	16	–	16	ns
t_{WCS}	Write command setup time [11]	0	–	0	–	ns
t_{CSR}	$\overline{CAS}$ setup time ($\overline{CAS}$-before-$\overline{RAS}$ cycle)	10	–	10	–	ns
t_{CHR}	$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ cycle)	30	–	30	–	ns
t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ precharge time	0	–	0	–	ns
t_{CPN}	$\overline{CAS}$ precharge time	10	–	15	–	ns
t_{WRP}	$\overline{WRITE}$ to $\overline{RAS}$ precharge time [13]	10	–	10	–	ns
t_{WRH}	$\overline{WRITE}$ hold time referenced to $\overline{RAS}$ [13]	10	–	10	–	ns

Notes see page 161.

Capacitance

T_A = 0 to 70 °C; V_{CC} = 5 V ± 10 %; f = 1 MHz

Symbol	Parameter	Limit values		Unit
		min.	max.	
C_{I1}	Input capacitance (A0 – A10, $\overline{W}$, $\overline{CAS}$, $\overline{RAS}$)	–	60	pF
C_{I2}	Input capacitance (D8, $\overline{CAS8}$)	–	10	pF
C_{IO}	I/O capacitance (DQ0 – DQ7)	–	15	pF
C_O	Output capacitance (Q8)	–	10	pF

Notes for pages 158 to 160

1) All voltages are referenced to V_{SS}.

2) I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} depend on cycle rate.

3) I_{CC1} and I_{CC4} depend on output loading. Specified values are obtained with the output open.

4) An initial pause of 200 µs is required after power-up followed by 8 $\overline{RAS}$ cycles out of which at least one cycle has to be a refresh cycle before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$-before-$\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.

5) V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring timing of input signals. Transition times are also measured between V_{IH} and V_{IL}.

6) Measured with a load equivalent to 2 TTL loads and 100 pF.

7) t_{OFF} (max.) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

8) Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

9) These parameters are referenced to $\overline{CAS}$ leading edge.

10) t_{WCS} is not a restrictive operating parameters. This is included in the data sheet as electrical characteristics only. If $t_{WCS} > t_{WCS}$ (min.), the cycle is an early write cycle and data out pin will remain open circuit (high impedance).

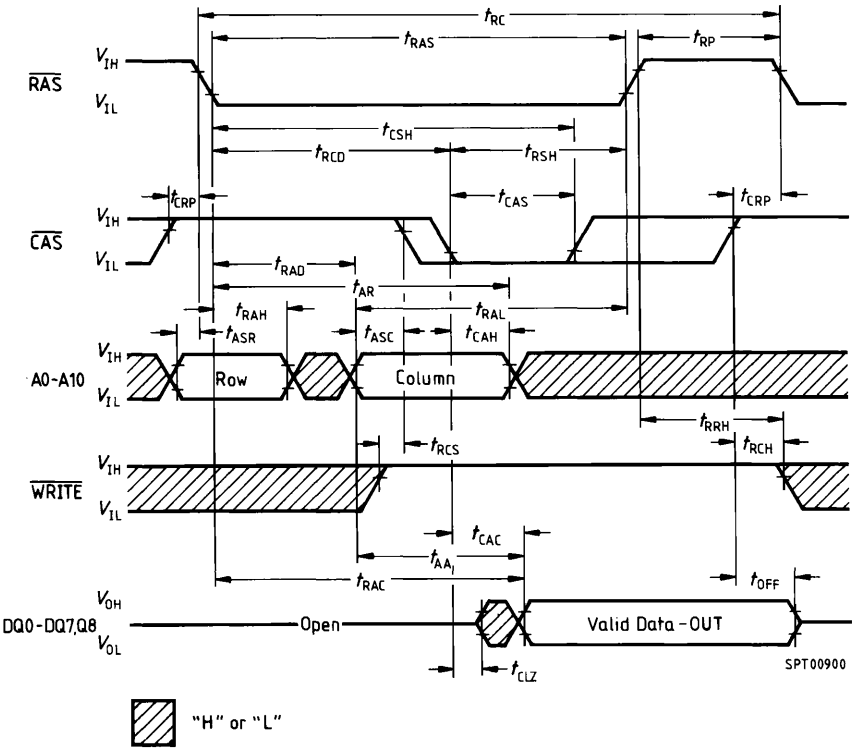
11) Operation within the t_{RCD} (max.) limit ensures that t_{RAC} (max.) can be met. t_{RCD} (max.) is specified as a reference point only: If t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled by t_{CAC}.

12) Operation within the t_{RAD} (max.) limit ensures that t_{RAC} (max.) can be met. t_{RAD} (max.) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD} (max.) limit, then access time is controlled by t_{AA}.

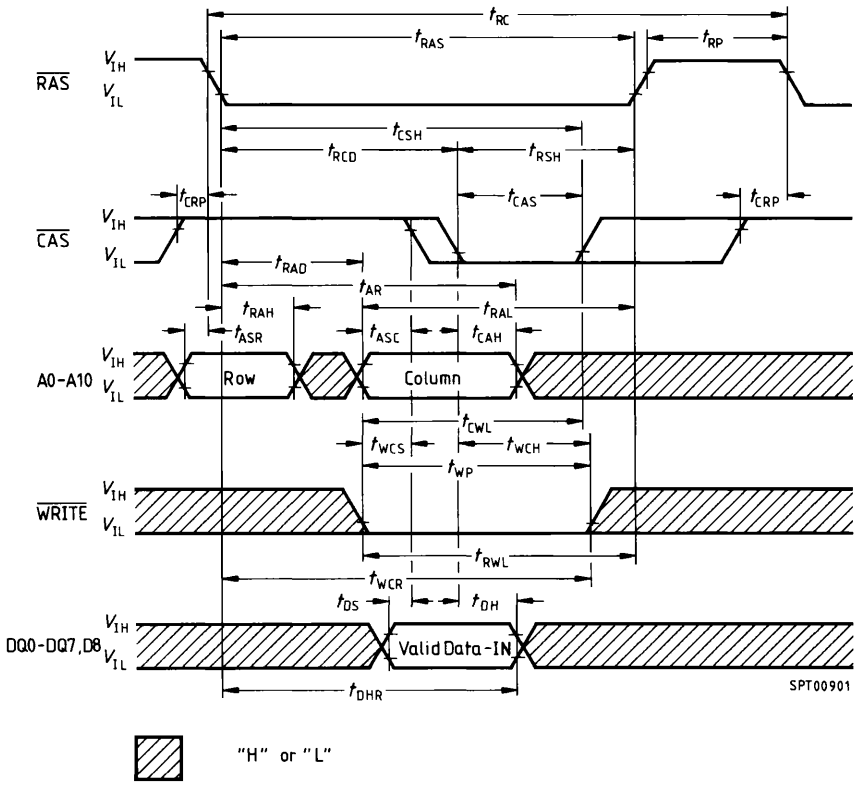
13) For $\overline{CAS}$-before-$\overline{RAS}$ cycles only.

Waveforms

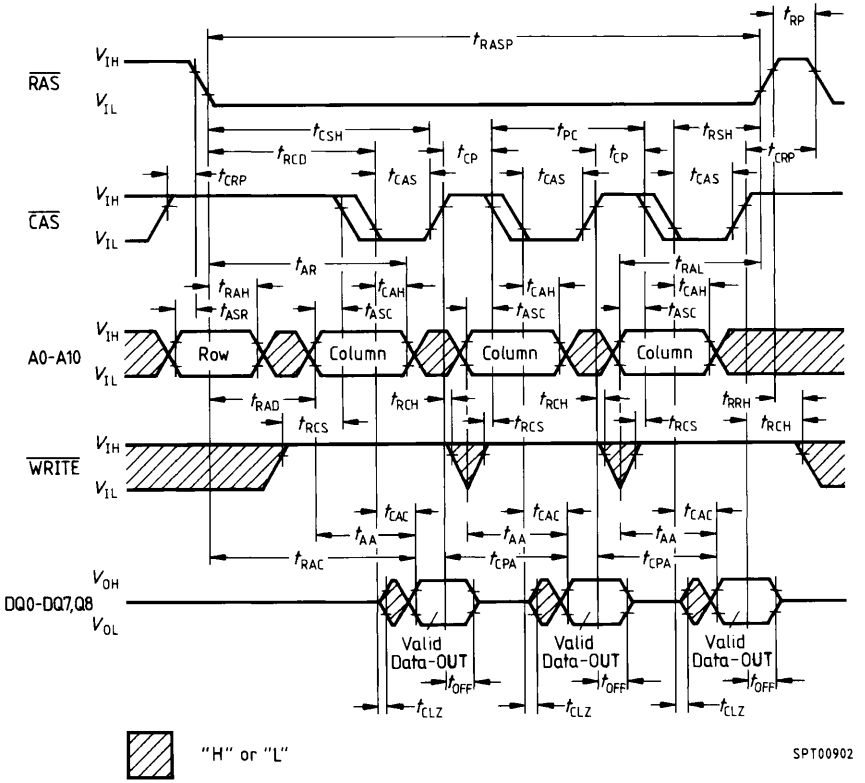
Read Cycle



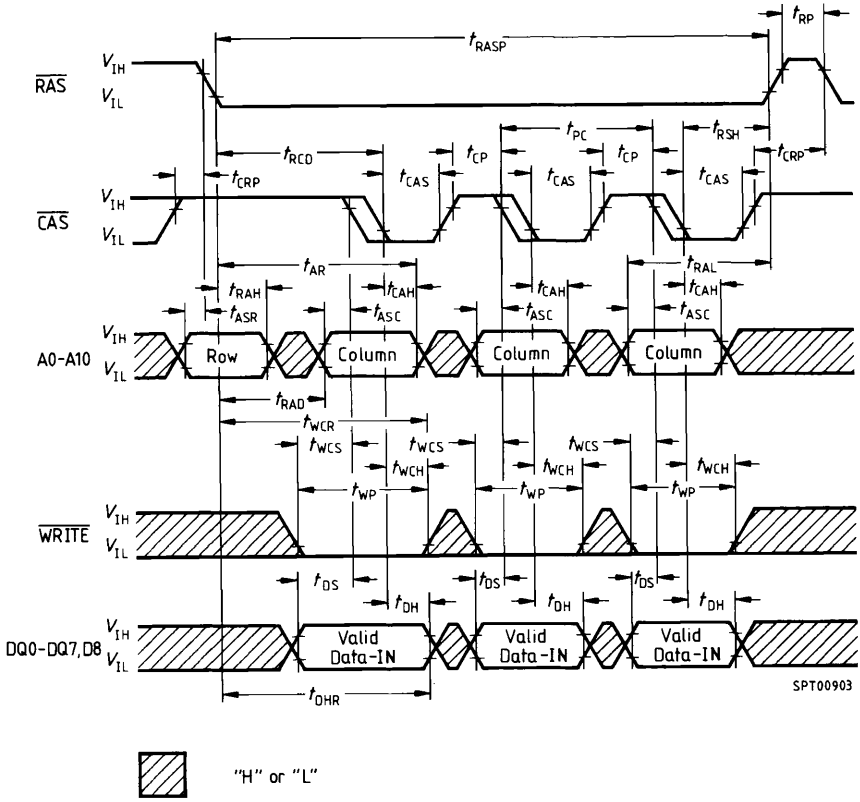
Write Cycle (early write)



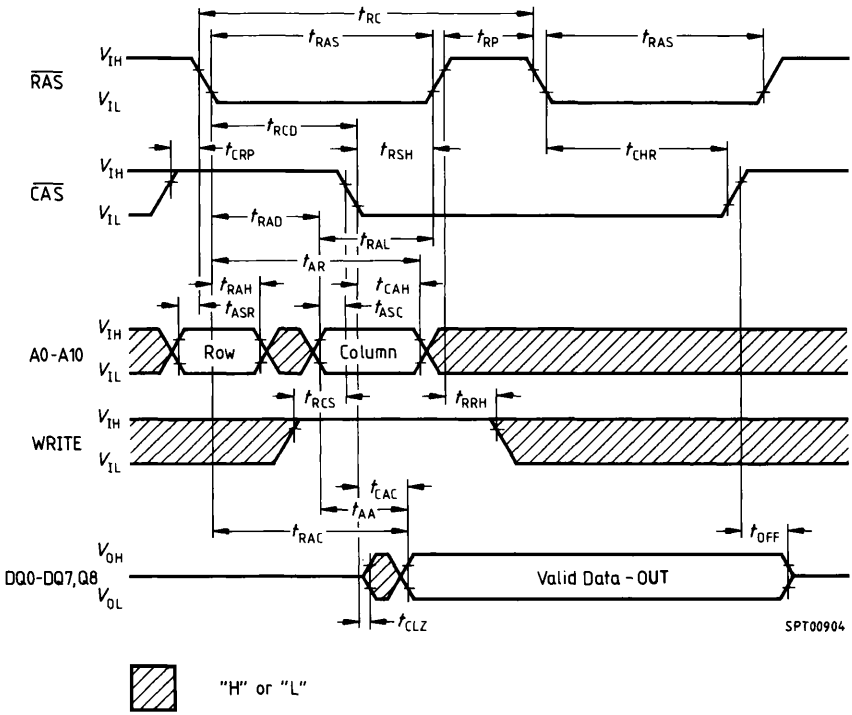
Fast Page Mode Read Cycle



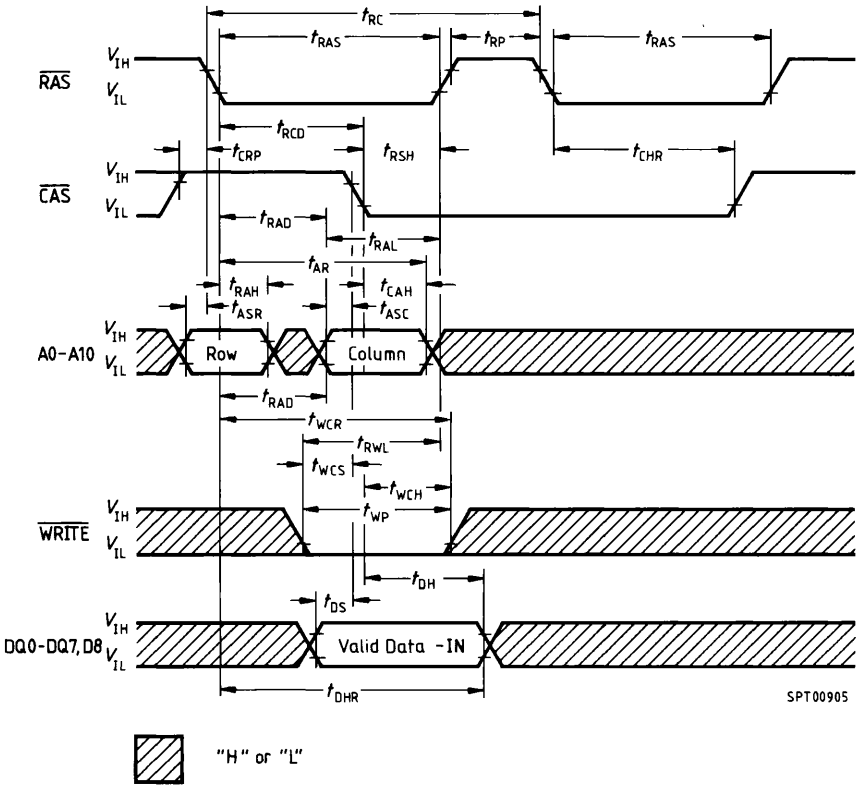
Fast Page Mode Write Cycle (early write)



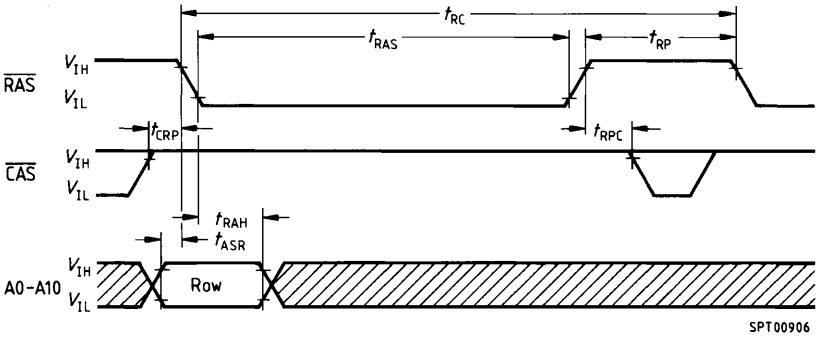
Hidden Refresh Cycle (read)



Hidden Refresh Cycle (write)

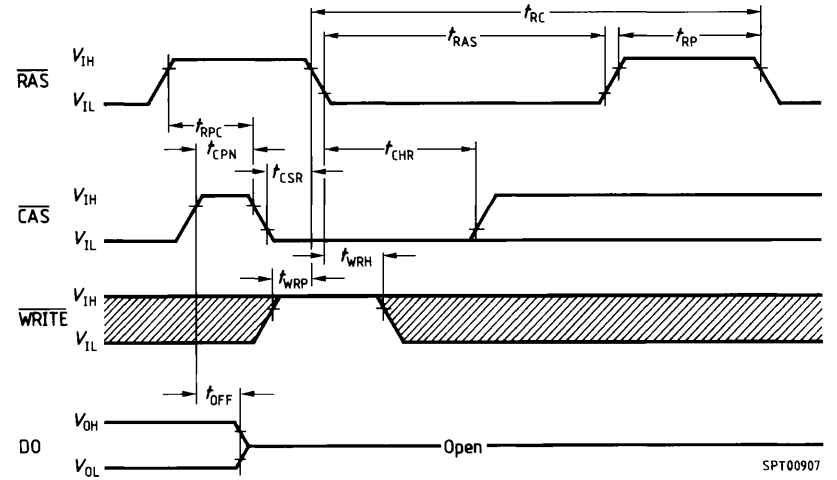


$\overline{RAS}$-Only Refresh Cycle



Note: $\overline{WRITE}$ = "H" or "L", A 10 = "H" or "L" "H" or "L"

$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Cycle



Note: A0 - A10 = Don't Care "H" or "L"