# HD153081
# Hard Disk Drive Programmable Filter/Frequency Synthesizer

HITACHI

Preliminary
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The HD153081 is a programmable filter/frequency synthesizer developed for use with magnetic disks with transfer rates of up to 40 Mbps. When used with a 1, 7 RLL code, the HD153081 built-in programmable filter is a variable cutoff frequency read channel filter that includes a pulse slimming equalizer function based on a 2-stage differentiation method combined with a low pass filter that has seventh order Bessel function characteristics. Also, the frequency synthesizer is used for write clock synthesis, and generates the clock used for writing data to the disk.

## Features

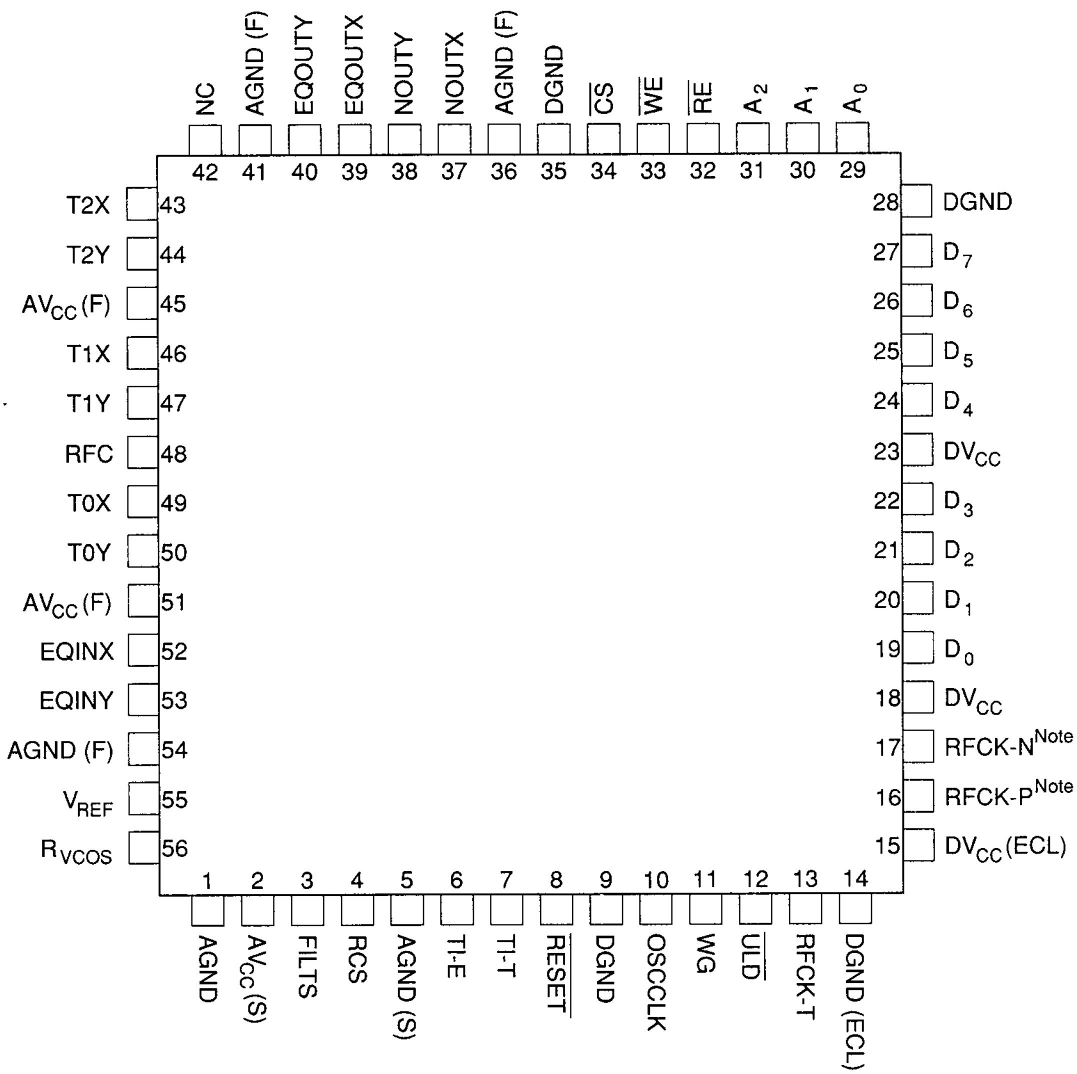
- Built-in electronic control programmable filter with seventh order Bessel characteristics
- The filter cutoff frequency can be set to any frequency in the 5 to 30 MHz range.
- Two filter output systems are provided: a low pass output and a low pass differential output. The group delay characteristics of these systems can be set to be identical.
- Pulse slimming based on a 2-stage differentiation equalizer is provided.
- The gain at the cutoff frequency can be boosted by up to 15 dB.
- The group delay characteristics when boost is used do not depend on the amount of boost.
- Built-in PLL write clock generation frequency synthesizer
- Clock frequencies of up to 60 MHz can be generated by setting the division ratios of the two dividers.
- Two output clock systems are provided: a pseudo-ECL differential output and a single-sided TTL output.
- Built-in unlock detection function for detecting PLL synchronization loss
- The unlock detection circuit can be set to one of four sensitivity levels.
- High speed and low power dissipation characteristics were realized by the adoption of a Hi-BiCMOS process.
- Standby function provided
- The QFP-56 package used is optimal for miniature surface mounting. (Resin size: 10 × 10 mm)
- Easy to handle 5 V single-voltage power supply specification

## Functional Overview

| Item | Specification |
|---|---|
| Filter characteristics | Seventh order Bessel characteristics |
| Cutoff frequency | 5 to 30 MHz (programmable) |
| Equalizer | 2-stage differentiation technique |
| Boost level | 0 to 15 dB (programmable) |
| Synthesizer output clock frequency | Up to 60 MHz (programmable) |

| Item | | Specification |
|---|---|---|
| Synthesizer PLL pull-in time | | Less than 1 ms |
| Data transfer rate (for 1, 7 code) | | 15 to 40 Mbps |
| Power dissipation | Operating | 600 mW |
| | Standby | Less than 10 mW |
| I/O | | TTL/pseudo-ECL |
| Power supply | | Unitary 5 V |
| Package | | QFP-56 (Resin size 10 x 10 mm) |

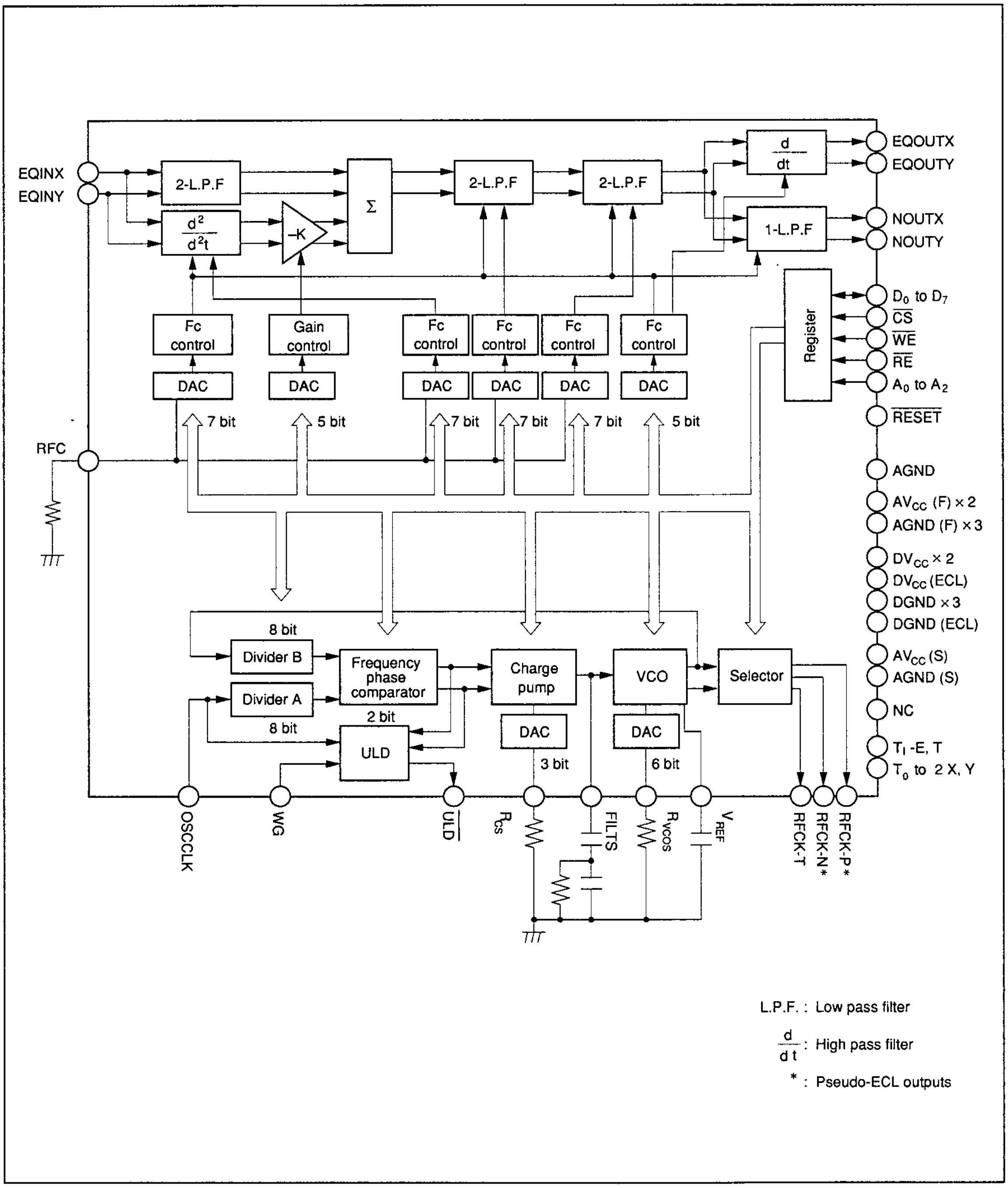
## Pin Arrangement




Note: Pseudo-ECL outputs

(Top view)

## Block Diagram



## Pin Assignments

| Pin Name | Pin Number | Type | Function |
|---|---|---|---|
| $\overline{RESET}$ | 8 | In | The internal circuits are re-initialized when this pin is set low. It should be held at a high value during normal operation. This pin must be brought low at least once following power on. |
| OSCCLK | 10 | In | The input from this pin provides the basic clock for the frequency synthesizer. The frequency synthesizer uses a PLL technique to generate the other clock frequencies based on the clock input to this pin. |
| WG | 11 | In | Set this pin high during writes.<br>This activates the frequency synthesizer PLL unlock detection circuit, and enables the $\overline{ULD}$ pin. |
| $D_0$ to $D_7$ | 19 to 22<br>24 to 27 | In/Out | These pins are connected to the register data signals, and are usually connected to the microcomputer data bus.<br>These function as input pins when $\overline{RE}$ is high, and as output pins when $\overline{RE}$ is low. |
| $A_0$ to $A_2$ | 29 to 31 | In | These pins are connected internally to the register address signals, and are usually connected externally to the microcomputer address bus. |
| $\overline{RE}$ | 32 | In | This is a register control pin. When $\overline{RE}$ is low, the contents of the register specified by the address are output to the microcomputer bus. This pin is used to check the contents of registers. Set the $\overline{CS}$ pin low during this operation. |
| $\overline{WE}$ | 33 | In | This is a register control pin. The data on the microcomputer bus is transferred to the register specified by the address on the rising edge of this signal. Set the $\overline{CS}$ pin low during this operation. |
| $\overline{CS}$ | 34 | In | This is a register control pin. When this pin is low, the register specified by the address on the microcomputer bus is selected. |
| EQINX<br>EQINY | 52<br>53 | In<br>In | The programmable filter differential input pins. Normally connected to the output of the AGC circuit through a coupling capacitance. |
| $\overline{ULD}$ | 12 | Out | The frequency synthesizer's unlock detection circuit error output pin. This pin outputs a low pulse when the frequency synthesizer's PLL circuit loses synchronization. When this occurs, the disk controller must immediately stop the write operation and restart the operation from the first data item. |
| RFCK-T | 13 | Out | Frequency synthesizer output clock pin. The output from this pin is a single-sided TTL level. It is selected by setting bit 6 ($D_6$) of register 7 to 0. |
| RFCK-P<br>RFCK-N | 16<br>17 | Out<br>Out<br>(ECL) | Frequency synthesizer output clock pins. The outputs from these pins are differential (pseudo-) ECL levels. They are selected by setting bit 6 ($D_6$) of register 7 to 1. |
| NOUTX<br>NOUTY | 37<br>38 | Out<br>Out | Programmable filter differential low-pass output pins. They are normally used to control the AGC circuit connected to the previous stage. They are connected through a coupling capacitance. |

## Pin Assignments (cont)

| Pin Name | Pin Number | Type | Function |
|---|---|---|---|
| EQOUTX<br>EQOUTY | 39<br>40 | Out<br>Out | Programmable filter differential low-pass differentiator output pins. These are normally connected to the peak detection circuit connected of the previous stage through a coupling capacitance. |
| FILTS | 3 | Component connection | Frequency synthesizer external loop filter connection. |
| $R_{CS}$ | 4 | Component connection | Resistance connection for setting the programmable filter reference voltage. |
| $R_{FC}$ | 48 | Component connection | Resistance connection for setting the programmable filter reference current. |
| $V_{REF}$ | 55 | Component connection | Connection for the frequency synthesizer VCO reference voltage stabilization capacitance. |
| $R_{VCOS}$· | 56 | Component connection | Connection for the resistance that sets the frequency synthesizer VCO center frequency. |
| $AV_{CC\ (S)}$ | 2 | Power supply | The analog circuit $V_{CC}$ pin that supplies power for the frequency synthesizer analog circuits. |
| $AV_{CC\ (F)}$ | 45<br>51 | Power supply | The analog circuit $V_{CC}$ pins that supply power to the programmable filter analog circuits. |
| $DV_{CC}$ | 18<br>23 | Power supply | The digital circuit $V_{CC}$ pin. |
| $DV_{CC}$ (ECL) | 15 | Power supply | The digital circuit $V_{CC}$ pin that supplies power for the ECL buffer circuit. |
| AGND | 1 | Power supply | The substrate ground pin that provides the ground potential for the whole substrate. |
| AGND (S) | 5 | Power supply | The analog circuit ground pin for power supply to the frequency synthesizer analog circuits. |
| AGND (F) | 36<br>41<br>54 | Power supply | The analog circuit ground pin for power supply to the programmable filter analog circuits. |
| DGND | 9<br>28<br>35 | Power supply | The digital circuit ground pin. |
| DGND (ECL) | 14 | Power supply | The digital circuit ground pin for power supply to the ECL buffer circuits. |
| TI-E<br>TI-T | 6<br>7 | In | Test input pins. Should be tied high. |
| T2X<br>T2Y<br>T1X<br>T1Y<br>T0X<br>T0Y | 43<br>44<br>46<br>47<br>49<br>50 | Out | Test output pins. Should be left open. |
| NC | 42 | NC | Unused pin. Connect to substrate $V_{CC}$ or ground for heat dissipation. |

## Functional Description

### Registers

This IC includes eight built-in 8-bit registers. These registers control the frequency synthesizer frequency, the programmable filter cutoff frequency, the programmable filter equalizer boost level, and other parameters.

| Address | | | | |
|---|---|---|---|---|
| $A_2$ | $A_1$ | $A_0$ | Name | Function |
| 0 | 0 | 0 | Register 0 | Synthesizer input clock frequency switching divider A |
| 0 | 0 | 1 | Register 1 | Synthesizer input clock frequency switching divider B |
| 0 | 1 | 0 | Register 2 | Charge pump current, unlock detection sensitivity, and VCO center frequency |
| 0 | 1 | 1 | Register 3 | Filter cutoff frequency, differential output offset |
| 1 | 0 | 0 | Register 4 | Filter cutoff frequency, differential output offset |
| 1 | 0 | 1 | Register 5 | Filter cutoff frequency, differential output offset |
| 1 | 1 | 0 | Register 6 | Filter cutoff frequency, differential output offset |
| 1 | 1 | 1 | Register 7 | Filter boost level, differential output offset, output clock level, and standby mode |

### Initial Values after Reset

| Address | | | Data | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| $A_2$ | $A_1$ | $A_0$ | $D_7$ | $D_6$ | $D_5$ | $D_4$ | $D_3$ | $D_2$ | $D_1$ | $D_0$ |
| 0 | 0 | 0 | 1 Note | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 Note | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | | MSB | | | | | | | LSB |

Note: Set to 1 after reset.

**Register 0 (divider A setting)**

| Address | | | Data | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| $A_2$ | $A_1$ | $A_0$ | $D_7$ | $D_6$ | $D_5$ | $D_4$ | $D_3$ | $D_2$ | $D_1$ | $D_0$ |
| 0 | 0 | 0 | | | | | | | | |

MSB — LSB

This register sets the divisor value $N_A$ for the synthesizer input clock switching divider A. The settings are described in the section on frequency synthesizer settings below.

00000010: $N_A = 2$ (divisor)
to
11111111: $N_A = 255$ (divisor)

**Register 1 (divider B setting)**

| Address | | | Data | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| $A_2$ | $A_1$ | $A_0$ | $D_7$ | $D_6$ | $D_5$ | $D_4$ | $D_3$ | $D_2$ | $D_1$ | $D_0$ |
| 0 | 0 | 1 | | | | | | | | |

MSB — LSB

This register sets the divisor value $N_B$ for the synthesizer input clock switching divider B. The settings are described in the section on frequency synthesizer settings below.

00000100: $N_A = 4$ (divisor)
to
11111111: $N_A = 255$ (divisor)

**Register 2 (charge pump current, unlock detection, VCO center frequency)**

| Address | | | Data | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| $A_2$ | $A_1$ | $A_0$ | $D_7$ | $D_6$ | $D_5$ | $D_4$ | $D_3$ | $D_2$ | $D_1$ | $D_0$ |
| 0 | 1 | 0 | | | | | | | | |
| | | | MSB | | | | | | | LSB |

These bits set the charge pump current ratio $N_C$. The current values that result from these settings are calculated by formula (3-4) in the item on PLL constant calculation formulas below.

000: $N_C = 0$ (Reference current times 1.0)
to
111: $N_C = 7$ (Reference current times 1.875)

The reference current is given by the expression $K_3 / R_{CS}$ in formula (3-4) below.

These bits set the unlock detection circuit detection sensitivity $N_{ULD}$.

00: $N_{ULD} = 2$ (Maximum sensitivity)
to
11: $N_{ULD} = 8$ (Minimum sensitivity)

Refer to the section on the unlock detection function below for details.

This bit is used for testing. It shorts the VCO input, and fixes the synthesizer output at the VCO center frequency.

0: Normal operation
1: VCO input short

These bits are reserved for testing, and must always be set to "00".

**Register 3 (cutoff frequency, differential output offset)**

| Address | | | Data | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| $A_2$ | $A_1$ | $A_0$ | $D_7$ | $D_6$ | $D_5$ | $D_4$ | $D_3$ | $D_2$ | $D_1$ | $D_0$ |
| 0 | 1 | 1 | | | | | | | | |

MSB (D7) … LSB (D0)

$D_6$–$D_0$: Sets the programmable filter cutoff frequency fc setting value $N_{fc}$. Refer to the section on setting the programmable filter constants below for details on this setting.

0010110: The minimum fc value (5 MHz)
to
1101010: The maximum fc value (30 MHz)

$D_7$: Sets the low pass differential offset adjustment $N_{fd}$. This bit indicates bit 0. Refer to the section on setting the programmable filter constants below for details on this setting.

**Register 4 (cutoff frequency, differential output offset)**

| Address | | | Data | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| $A_2$ | $A_1$ | $A_0$ | $D_7$ | $D_6$ | $D_5$ | $D_4$ | $D_3$ | $D_2$ | $D_1$ | $D_0$ |
| 1 | 0 | 0 | | | | | | | | |

MSB (D7) … LSB (D0)

$D_6$–$D_0$: Sets the programmable filter cutoff frequency fc setting value $N_{fc}$. Refer to the section on setting the programmable filter constants below for details on this setting.

0010110: The minimum fc value (5 MHz)
to
1101010: The maximum fc value (30 MHz)

$D_7$: Sets the low pass differential offset adjustment $N_{fd}$. This bit indicates bit 1. Refer to the section on setting the programmable filter constants below for details on this setting.

**Register 5 (cutoff frequency, differential output offset)**

| Address | | | Data | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| $A_2$ | $A_1$ | $A_0$ | $D_7$ | $D_6$ | $D_5$ | $D_4$ | $D_3$ | $D_2$ | $D_1$ | $D_0$ |
| 1 | 0 | 1 | | | | | | | | |

MSB ($D_7$) — LSB ($D_0$)

$D_6$–$D_0$: Sets the low pass differential offset adjustment $N_{fc}$. Refer to the section on setting the programmable filter constants below for details on this setting.

0010110: The minimum fc value (5 MHz)
to
1101010: The maximum fc value (30 MHz)

$D_7$: Sets the low pass differential offset adjustment $N_{fd}$. This bit indicates bit 2. Refer to the section on setting the programmable filter constants below for details on this setting.

**Register 6 (cutoff frequency, differential output offset)**

| Address | | | Data | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| $A_2$ | $A_1$ | $A_0$ | $D_7$ | $D_6$ | $D_5$ | $D_4$ | $D_3$ | $D_2$ | $D_1$ | $D_0$ |
| 1 | 1 | 0 | | | | | | | | |

MSB ($D_7$) — LSB ($D_0$)

$D_6$–$D_0$: Sets the programmable filter cutoff frequency fc setting value $N_{fc}$. Refer to the section on setting the programmable filter constants below for details on this setting.

0010110: The minimum fc value (5 MHz)
to
1101010: The maximum fc value (30 MHz)

$D_7$: Sets the low pass differential offset adjustment $N_{fd}$. This bit indicates bit 3. Refer to the section on setting the programmable filter constants below for details on this setting.

**Register 7 (boost level, differential output offset, output level, standby)**

| Address | | | Data | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| $A_2$ | $A_1$ | $A_0$ | $D_7$ | $D_6$ | $D_5$ | $D_4$ | $D_3$ | $D_2$ | $D_1$ | $D_0$ |
| 1 | 1 | 1 | | | | | | | | |

MSB ($D_7$) … LSB ($D_0$)

$D_4$–$D_0$: Sets the $N_{gb}$ setting for the programmable filter boost level gb. Refer to the section on setting the programmable filter constants below for details on this setting.

00001: The minimum gb value (0 dB)
to
10001: The maximum gb value (15 dB, fc = 5 MHz)

$D_5$: Sets the low pass differential offset adjustment $N_{fd}$. This bit indicates bit 4. Refer to the section on setting the programmable filter constants below for details on this setting.

$D_6$: Switches the synthesizer output clock level.

0: TTL
1: Pseudo-ECL

$D_7$: Sets all circuits to standby mode and reduces power dissipation.

0: Normal operating state
1: Standby state

## The Programmable Filter

The programmable filter is an electronically controlled filter whose cutoff frequency can be set to any frequency in the range 5 to 30 MHz. The filter characteristics are those of a seventh order Bessel function, and two output systems, a low pass system and a low pass differential system are provided. When both are used, the group delay characteristics of both systems can set to be identical.

The programmable filter also includes a two-stage differentiation technique based pulse slimming equalizer function, and the gain, gb, can be boosted by as much as 15 dB at the cutoff frequency. When this function is used, the group delay characteristics will be independent of the boost level.

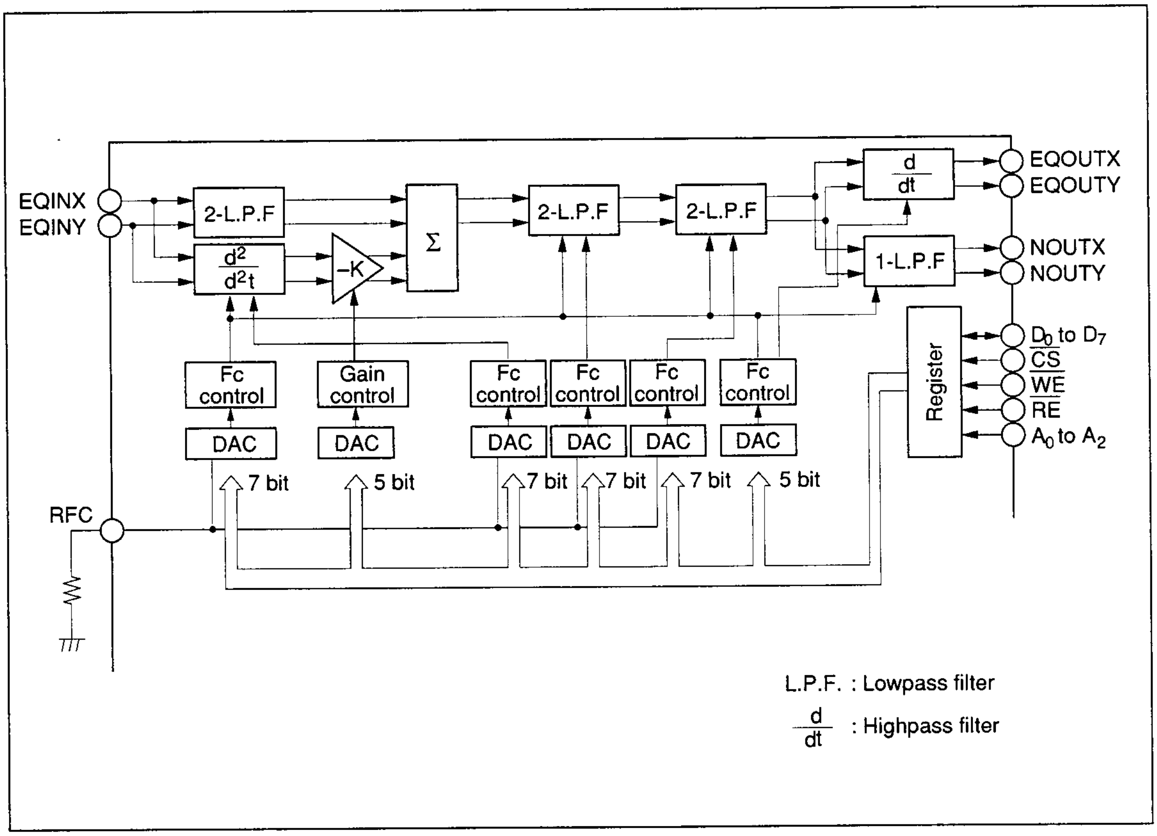
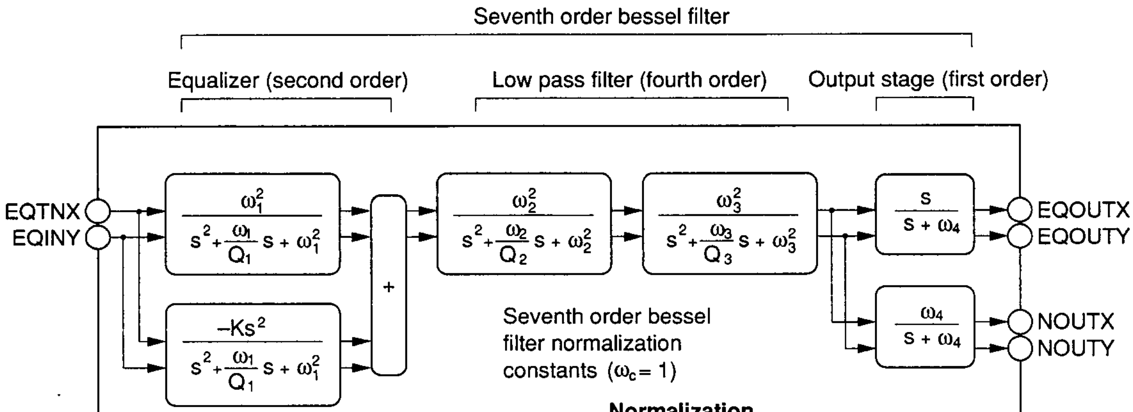



**Figure 1 Programmable Filter Block Diagram**

## Programmable Filter Transfer Characteristics




$$\frac{\omega_1^2}{s^2+\frac{\omega_1}{Q_1}s+\omega_1^2} \quad \frac{-Ks^2}{s^2+\frac{\omega_1}{Q_1}s+\omega_1^2} \quad \frac{\omega_2^2}{s^2+\frac{\omega_2}{Q_2}s+\omega_2^2} \quad \frac{\omega_3^2}{s^2+\frac{\omega_3}{Q_3}s+\omega_3^2} \quad \frac{s}{s+\omega_4} \quad \frac{\omega_4}{s+\omega_4}$$

| Item | Normalization Constant |
|---|---|
| $\omega_1^2$ | 2.94930 |
| $\omega_1/Q_1$ | 3.22597 |
| $\omega_2^2$ | 3.32507 |
| $\omega_2/Q_2$ | 2.75939 |
| $\omega_3^2$ | 4.20534 |
| $\omega_3/Q_3$ | 1.82031 |
| $\omega_4$ | 1.68536 |

**Figure 2 Programmable Filter Transfer Characteristics**

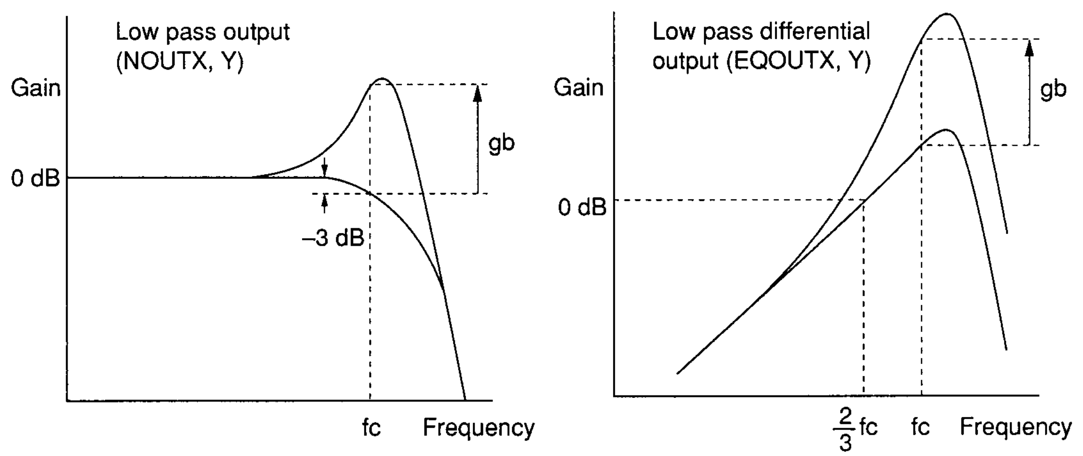



**Figure 3 Programmable Filter Transfer Characteristics Overview**

## Formulas for the Programmable Filter Settings

- The filter cutoff frequency $f_c$ (MHz) setting, $N_{fc}$

  $N_{fc} = \text{int}^{\text{Note}} [a_1 + a_2 (f_c + a_3)^2]$ ... (2-1)

  $a_1 = 135.5$
  $a2 = -0.044$
  $a3 = -55.7$

- The filter boost level $g_b$ (dB) setting, $N_{gb}$

  $N_{gb} = \text{int}^{\text{Note}} [b_1 + b_2 \times g_b]$ ... (2-2)

  $b_1 = 1.32 - 0.0176 \times f_c$
  $b_2 = 1.12 - 0.0115 \times f_c$

- The low pass differential offset adjustment value, $N_{fd}$

  $N_{fd} = \text{int}^{\text{Note}} [19.5 + \frac{fc}{5}]$ ... (2-3)

- The filter reference current generation external resistance value, $R_{fc}$

  $R_{fc} = 4.0\ k\Omega$ (fixed) ... (2-4)

Note: int[ ] is the integer value calculated by discarding the fractional part of the value.

## Setting the Programmable Filter Constants

- The filter cutoff frequency fc (MHz) setting, $N_{fc}$
  1. Determine the required cutoff frequencies for each transfer rate.*1
  2. Using formula (2-1), compute $N_{fc}$, the filter cutoff frequency constant, from the cutoff frequencies calculated in step 1, and set the values of registers 3 to 6 as shown in table 1.*2

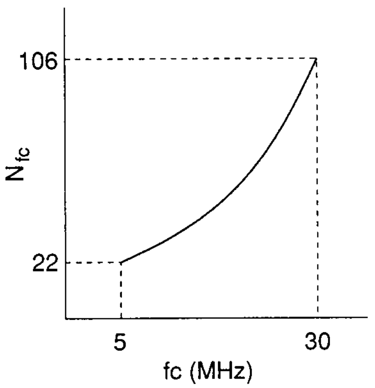
Notes: 1. Since the relationship between the transfer speed and the cutoff frequency fc will differ depending on the characteristics of the disk system (e.g., the type of heads and medium) in which the HD153081 is being used, an optimal value should be determined separately for each application system.

2. Registers 3 to 6 are all set to the same setting value, $N_{fc}$, and the cutoff frequency fc will be indicated by the seventh order Bessel characteristics of the system. Although the filter characteristics can be adjusted by changing the values of registers 4 to 6 with respect to the value in register 3, we do not recommend this for most situations.

**Table 1 Settings for Registers 3 to 6**

| | | Settings for Registers 3 to 6 | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Address | | | Data | | | | | | | |
| fc | $N_{fc}$ | $A_2$ | $A_1$ | $A_0$ | $D_7$ | $D_6$ | $D_5$ | $D_4$ | $D_3$ | $D_2$ | $D_1$ | $D_0$ |
| 5 | 22 | 0 | 1 | 1 | — | | | | | | | |
| | | to | | | — | 0 | 0 | 1 | 0 | 1 | 1 | 0 |
| | | 1 | 1 | 0 | — | | | | | | | |
| to | to | to | | | to | | | | | | | |
| 30 | 106 | 0 | 1 | 1 | — | | | | | | | |
| | | to | | | — | 1 | 1 | 0 | 1 | 0 | 1 | 0 |
| | | 1 | 1 | 0 | — | | | | | | | |

—: Don't care.



- The filter boost level gb (dB) setting, $N_{gb}$
  1. If the equalizer pulse slimming function is to be used, determine the boost level gb for the gain at the cutoff frequency fc.Note
  2. Using formula (2-2), compute the filter boost level setting value, $N_{gb}$, from the boost level gb determined in step 1, and set register 7 as shown in table 2.

Note: As was the case for the cutoff frequency fc, in determining the boost gain gb, since the characteristics of the system will vary with the structure of the disk system actually used, the optimal value should be determined separately for each application system.

- The low pass differential output offset adjustment value, $N_{fd}$
  — Using formula (2-3), compute the low pass differential output offset setting value, $N_{fd}$, and set registers 3 to 7 as shown in table 3.Note

Note: The low pass differential output adjustment value $N_{fd}$ is a value that adjusts the fc offset of the low pass differential output differentiator, and using formula (2-3) value, the group delay characteristics of the low pass differential output (the EQOUTX and Y pins) and the low pass output (the NOUTX and Y pins) can be set up to be equal. Although it is possible to set the low pass differential output adjustment value Nfd independently and thus alter only the low pass differential characteristics, we do not recommend this since it would result in group delay characteristics that differ from those of the low pass output.

**Table 2 Settings for Register 7**

Settings for Register 7

| | Address | | | Data | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| $N_{gb}$ | $A_2$ | $A_1$ | $A_0$ | $D_7$ | $D_6$ | $D_5$ | $D_4$ | $D_3$ | $D_2$ | $D_1$ | $D_0$ |
| 1 | 1 | 1 | 1 | — | — | — | 0 | 0 | 0 | 0 | 1 |
| to | 1 | 1 | 1 | | | | to | | | | |
| 17 | 1 | 1 | 1 | — | — | — | 1 | 0 | 0 | 0 | 1 |

—: Don't care.

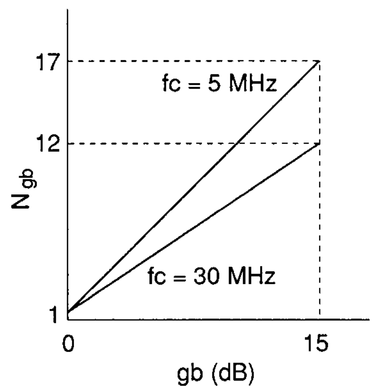
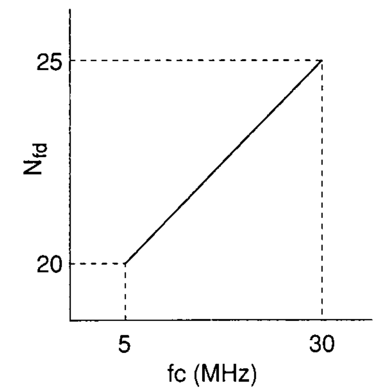



**Table 3 Settings for Registers 3 to 7**

Settings for Registers 3 to 7

| | Address | | | Data | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| $N_{fd}$ | $A_2$ | $A_1$ | $A_0$ | $D_7$ | $D_6$ | $D_5$ | $D_4$ | $D_3$ | $D_2$ | $D_1$ | $D_0$ |
| 20 | 0 | 1 | 1 | 0 | — | — | — | — | — | — | — |
| | 1 | 0 | 0 | 0 | — | — | — | — | — | — | — |
| | 1 | 0 | 1 | 1 | — | — | — | — | — | — | — |
| | 1 | 1 | 0 | 0 | — | — | — | — | — | — | — |
| | 1 | 1 | 1 | — | — | 1 | — | — | — | — | — |
| to | | | | to | | | | | | | |
| 25 | 0 | 1 | 1 | 1 | — | — | — | — | — | — | — |
| | 1 | 0 | 0 | 0 | — | — | — | — | — | — | — |
| | 1 | 0 | 1 | 0 | — | — | — | — | — | — | — |
| | 1 | 1 | 0 | 1 | — | — | — | — | — | — | — |
| | 1 | 1 | 1 | — | — | 1 | — | — | — | — | — |

—: Don't care.



## Programmable Filter Setup Example

- When the filter cutoff frequency fc is 20 MHz

  According to formula (2-1)

**Settings for Registers 3 to 6**

| | Address | | | Data | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| $N_{fc}$ | $A_2$ | $A_1$ | $A_0$ | $D_7$ | $D_6$ | $D_5$ | $D_4$ | $D_3$ | $D_2$ | $D_1$ | $D_0$ |
| 79 | 0 | 1 | 1 | — | 1 | 0 | 0 | 1 | 1 | 1 | 1 |
| | 1 | 0 | 0 | — | 1 | 0 | 0 | 1 | 1 | 1 | 1 |
| | 1 | 0 | 1 | — | 1 | 0 | 0 | 1 | 1 | 1 | 1 |
| | 1 | 1 | 0 | — | 1 | 0 | 0 | 1 | 1 | 1 | 1 |

—: Don't care.

- When the filter boost level gb is 9 dB

  According to formula (2-2)

**Setting for Register 7**

| | | | Address | | | Data | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $b_1$ | $b_2$ | $N_{gb}$ | $A_2$ | $A_1$ | $A_0$ | $D_7$ | $D_6$ | $D_5$ | $D_4$ | $D_3$ | $D_2$ | $D_1$ | $D_0$ |
| 0.97 | 0.89 | 8 | 1 | 1 | 1 | — | — | — | 0 | 1 | 0 | 0 | 0 |

- Low pass differential output offset adjustment value

  According to formula (2-3)

**Settings for Registers 3 to 7**

| | Address | | | Data | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| $N_{fd}$ | $A_2$ | $A_1$ | $A_0$ | $D_7$ | $D_6$ | $D_5$ | $D_4$ | $D_3$ | $D_2$ | $D_1$ | $D_0$ |
| 23 | 0 | 1 | 1 | 1 | — | — | — | — | — | — | — |
| | 1 | 0 | 0 | 1 | — | — | — | — | — | — | — |
| | 1 | 0 | 1 | 1 | — | — | — | — | — | — | — |
| | 1 | 1 | 0 | 0 | — | — | — | — | — | — | — |
| | 1 | 1 | 1 | — | — | 1 | — | — | — | — | — |

**The Frequency Synthesizer**

The frequency synthesizer generates the write clock using a PLL technique. By setting the two divisor ratios, a clock with a frequency of up to 60 MHz can be generated. The divisor ratios are set by writing register values, and therefore differing clock frequencies can be output under program control. There are two clock output systems: a pseudo-ECL differential output system and a single-sided TTL output system.

There is also an unlock detection function that detects when the PLL synchronization is lost. This function is used to provide write protection on errors (drive faults), and the sensitivity with respect to the reference clock (OSCCLK) can be switched between 4 levels.

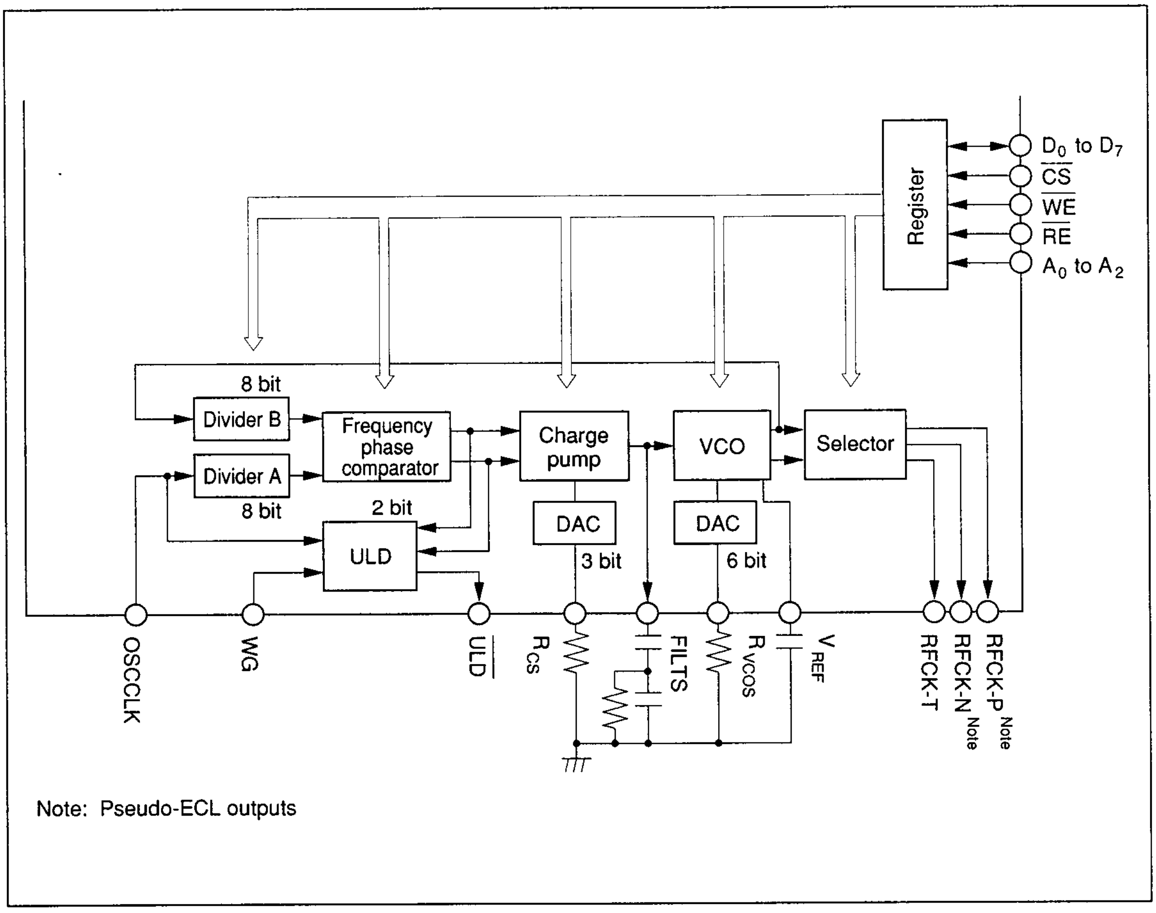



**Figure 4 Frequency Synthesizer Block Diagram**

### Unlock Detection Function

The unlock detection function is a function that detects loss of PLL synchronization, and is used to provide write protection on errors, i.e., drive faults. The unlock detection function outputs an error detection signal ($\overline{ULD}$) when the phase difference between the divider A and the divider B exceeds a certain range. This phase difference range is called the detection sensitivity, and can be selected from 4 levels with respect to the reference clock (OSCCLK) frequency. The table below shows the relationship between the detection sensitivity $N_{ULD}$ and the value set in register 2.

| Detection Sensitivity | Register 2 Setting | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | Address | | | Data | | | | | | | |
| $N_{ULD}$ | $A_2$ | $A_1$ | $A_0$ | $D_7$ | $D_6$ | $D_5$ | $D_4$ | $D_3$ | $D_2$ | $D_1$ | $D_0$ |
| 2 | 0 | 1 | 0 | — | — | — | 0 | 0 | — | — | — |
| 4 | 0 | 1 | 0 | — | — | — | 0 | 1 | — | — | — |
| 6 | 0 | 1 | 0 | — | — | — | 1 | 0 | — | — | — |
| 8 | 0 | 1 | 0 | — | — | — | 1 | 1 | — | — | — |

—: Don't care.

Here, the absolute value of the detection sensitivity phase difference is given by the formula below, which uses the period of the OSCCLK input, $T_{OSC}$.

$$N_{ULD} \times T_{OSC} \text{ (s)}$$

The ratio with respect to the PLL phase comparison period is given by the formula below using the divisor value $N_A$ of the divider A.

$$\frac{N_{ULD}}{N_A} \times 100 \text{ (\%)}$$

### Formulas for PLL Constant Derivation

- VCO center frequency $f_{VCOS}$

$$f_{VCOS} = \frac{K_1}{R_{VCOS}} \cdot \text{int}^{\text{Note}} \left[\frac{N_B}{4}\right] \text{ (Hz)} \quad \ldots (3\text{-}1)$$

$$K_1 = 28.12 \times 10^5$$

- VCO gain $K_{OS}$

$$K_{OS} = K_2 \cdot \sqrt{\frac{\text{int}^{\text{Note}}\,[N_B/4]}{R_{VCOS}}} \left(\frac{\text{rad}}{\text{s·v}}\right) \quad \ldots (3\text{-}2)$$

$$K_2 = 5.48 \times 10^5$$

- Charge pump current ratio $N_C$

$$N_C = \text{int}^{\text{Note}} [16 \cdot \sqrt{\frac{N_B}{N_{BMAX}}} - 8] \quad \ldots (3\text{-}3)$$

However, when $N_B = N_{BMAX}$, set $N_C = 7$.

- Charge pump current $I_{CS}$

$$I_{CS} = \frac{K_3}{R_{CS}} \left(1 + \frac{N_C}{8}\right) \text{ (A)} \quad \ldots (3\text{-}4)$$

$$K_3 = 5.00$$

- Characteristics frequency $\omega_{nS}$

$$\omega_{nS} = \sqrt{\frac{K_{OS} \cdot I_{CS}}{\pi \cdot N_B \cdot C_{S1}}} \left(\frac{\text{rad}}{\text{s}}\right) \quad \ldots (3\text{-}5)$$

- Attenuation ratio $\zeta_S$

$$\zeta_S = \frac{(C_{S1} + C_{S2})}{2} \cdot R_{S1} \cdot \omega_{nS} \quad \ldots (3\text{-}6)$$

Note: int [ ] is the integer value calculated by discarding the fractional part of the value.

### Setting the Frequency Synthesizer Constants

The frequency synthesizer output clock frequency $f_{OS}$ depends on the step frequency $f_{STEP}$ as follows.

$$f_{OS} = f_{STEP} \cdot N_B \text{ (Hz)} \quad \ldots (3\text{-}7)$$

$$f_{STEP} = \frac{f_{OSCCLK}}{N_A} \text{ (Hz)} \quad \ldots (3\text{-}8)$$

Here, select $N_B$ and $R_{VCOS}$ so that the VCO center frequency $f_{VCOS}$ indicated by formula (3-1) is essentially the same as $f_{OS}$. Use formula (3-9) as a guide.

$$0.95 \le \frac{f_{OS}}{f_{VCOS}} \le 1.05 \quad \ldots (3\text{-}9)$$

If the conditions of formula (3-9) are met, it will be possible to generate the required output clock frequency $f_{OS}$ by selecting appropriate values for $N_A$, $N_B$, and $R_{VCOS}$. However, the ranges of the values that can be selected are shown in table 4. Here, since the number of possible combination is large, we recommend using the method shown below for selecting these constants.

- Output clock frequency range and the step frequency determination

  Determine the output clock frequency range ($f_{OSMIN}$ to $f_{OSMAX}$) and the step frequency $f_{STEP}$ for each transfer rate so that:

  $$\frac{f_{OSMAX}}{f_{OSMIN}} \leq 4$$

- Divider A (register 0) setup

  Determine the input clock frequency for the OSCCLK pin ($f_{OSCCLK}$) and the value of the divisor $N_A$ from formula (3-8), and set divisor value $N_A$ in divider A (register 0).

- Divider B (register 1) setup

  Set the divisor value $N_B$ ($N_{BMIN}$ to $N_{BMAX}$) for divider B (register 1) to correspond to the output clock frequencies ($f_{OSMIN}$ to $f_{OSMAX}$) according to formula (3-7).

- VCO external resistance calculation

  Calculate $R_{VCOS}$ by substituting $N_B = N_{BMAX}$ and $f_{VCOS} = f_{OSMAX}$ into formula (3-1)

- VCO gain calculation

  Calculate the VCO gain for each output clock frequency using formula (3-2).

- Characteristic frequency calculation

  First determine the PLL pull-in time, Taq. Then calculate the PLL characteristic frequency $\omega_n$ using the formula below as an estimate.

  $$\omega_n \cdot Taq = 12$$

- Charge pump external resistance setup

  Set the charge pump external resistance to a value such that in formula (3-4), when $N_C = N_{CMAX}$, $I_{CS} \leq 500\ \mu A$.
  We recommend that $R_{CS}$ be 20 kΩ unless it is impossible to achieve the desired loop characteristics with that value.

- Filter capacitance calculation

  Calculate the filter capacitance $C_{S1}$ from formula (3-5). Here, when the value of $C_{S1}$ varies with the output clock frequency $f_{OS}$, we recommend using the average value.
  Taking high region jitter control and phase margin into account, we recommend setting $C_{S2}$ according to the formula below.

  $$C_{S2} = \frac{1}{45} C_{S1}$$

  (Adjust the value of $C_{S2}$ so that the multiplier is in the range 1/20 to 1/100.)

- Filter resistance calculation

  Calculate $R_{S1}$ from formula (3-6). Here, taking PLL loop stability into account, we

**Table 4**

| Constant | Range | Unit |
|---|---|---|
| $N_A$ | $2 \leq N_A \leq 255$ | Divisor (integer value) |
| $N_B$ | $4 \leq N_B \leq 255$ | Divisor (integer value) |
| $R_{VCOS}$ | $3.00 \leq R_{VCOS}$ | kΩ |

recommend setting the attenuation ratio $\zeta_S$ to be about 1.0.

- Confirmation

  Construct a Bode diagram from the open loop transfer functions, and determine whether the system is appropriate.

**Frequency Synthesizer Constants Setup Example**

- Output clock frequency range and step frequency determination

  $f_{OS}$ = 15 to 60 MHz
  $f_{STEP}$ = 0.234375 MHz

- Divider A (register 0) setup

  When $f_{OSCCLK}$ is 15 MHz,
  $N_A$ = 64.

**Register 0**

| | | Address | | | Data | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $f_{OSCCLK}$ [MHz] | $N_A$ | $A_2$ | $A_1$ | $A_0$ | $D_7$ | $D_6$ | $D_5$ | $D_4$ | $D_3$ | $D_2$ | $D_1$ | $D_0$ |
| 15.000000 | 64 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |

- Divider B (register 1) setup

**Register 1**

| | | Address | | | Data | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $f_{OS}$ [MHz] | $N_B$ | $A_2$ | $A_1$ | $A_0$ | $D_7$ | $D_6$ | $D_5$ | $D_4$ | $D_3$ | $D_2$ | $D_1$ | $D_0$ |
| 15.000000 | 64 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| 15.234375 | 65 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 |
| to | to | 0 | 0 | 1 | to | | | | | | | |
| 29.765625 | 127 | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 30.000000 | 128 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 30.234375 | 129 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| to | to | 0 | 0 | 1 | to | | | | | | | |
| 59.765625 | 255 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

- VCO external resistance calculation

  $R_{VCOS}$ = 3.0 kΩ

- VCO gain calculation

| $f_{OS}$ [MHz] | $K_{OS}$ [Mrad/sV] |
|---|---|
| 15 | 40.000 |
| to | to |
| 30 | 56.569 |
| to | to |
| 60 | 80.000 |

- Characteristic frequency calculation

  When Taq = 0.1 ms,
  $\omega_n$ = 120 krad/s

- Charge pump external resistance setup

  Set $R_{CS}$ to be 20 kΩ.

**Register 2**

| Address | | | Data | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $A_2$ | $A_1$ | $A_0$ | $D_7$ | $D_6$ | $D_5$ | $D_4$ | $D_3$ | $D_2$ | $D_1$ | $D_0$ | $N_C$ | $I_{CS}$ [mA] |
| 0 | 1 | 0 | — | — | — | — | — | 0 | 0 | 0 | 0 | 250.00 |
| 0 | 1 | 0 | to | | | | | | | | to | to |
| 0 | 1 | 0 | — | — | — | — | — | 1 | 1 | 1 | 7 | 468.75 |

—: Don't care.

- Filter capacitance calculation

| $f_{OS}$ [MHz] | $C_{S1}$ [pF] |
|---|---|
| 15 | 3454 |
| 30 | 3358 |
| 60 | 3251 |

$$C_{S1} = \frac{3454 + 3358 + 3251}{3} = 3354.3 \text{ pF} \rightarrow 3300 \text{ pF}$$

$$C_{S2} = \frac{1}{45} \times 3300 = 73.3 \text{ pF} \rightarrow 75 \text{ pF}$$

- Filter resistance calculation

  $R_{S1}$ = 4.938 kΩ → 5.1 kΩ

- Confirmation

  Bode diagram construction.

**Using register settings to change the constants**

- $f_{OSCCLK}$ vs. register 0 (when $f_{STEP}$ = 0.234375 MHz)

**Register 0**

| $f_{OSCCLK}$ [MHz] | $N_A$ | Address $A_2$ | $A_1$ | $A_0$ | Data $D_7$ | $D_6$ | $D_5$ | $D_4$ | $D_3$ | $D_2$ | $D_1$ | $D_0$ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0.468750 | 2 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| 0.703125 | 3 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| 0.937500 | 4 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| to | to | 0 | 0 | 0 | to | | | | | | | |
| 1.875000 | 8 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |
| to | to | 0 | 0 | 0 | to | | | | | | | |
| 3.750000 | 16 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |
| to | to | 0 | 0 | 0 | to | | | | | | | |
| 7.500000 | 32 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |
| to | to | 0 | 0 | 0 | to | | | | | | | |
| 15.000000 | 64 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| to | to | 0 | 0 | 0 | to | | | | | | | |
| 30.000000 | 128 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| to | to | 0 | 0 | 0 | to | | | | | | | |
| 59.53125 | 254 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 |
| 59.765625 | 255 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

- Register 1 vs. the VCO center frequency ($R_{VCOS}$ = 3.0 [kΩ])

**Register 1**

| Address $A_2$ | $A_1$ | $A_0$ | Data $D_7$ | $D_6$ | $D_5$ | $D_4$ | $D_3$ | $D_2$ | $D_1$ | $D_0$ | $N_B$ | $f_{OS}$ [MHz] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | — | — | 4 to 7 | 0.937500 |
| 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | — | — | 8 to 11 | 1.875000 |
| 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | — | — | 12 to 15 | 2.812500 |
| 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | — | — | 16 to 19 | 3.750000 |
| | | | to | | | | | | | | to | to |
| 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | — | — | 32 to 35 | 7.500000 |
| | | | to | | | | | | | | to | to |
| 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | — | — | 64 to 67 | 15.000000 |
| | | | to | | | | | | | | to | to |
| | | | 1 | 0 | 0 | 0 | 0 | 0 | — | — | 128 to 131 | 30.000000 |
| | | | to | | | | | | | | to | to |
| 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | — | — | 248 to 251 | 58.125000 |
| 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | — | — | 252 to 255 | 59.062500 |

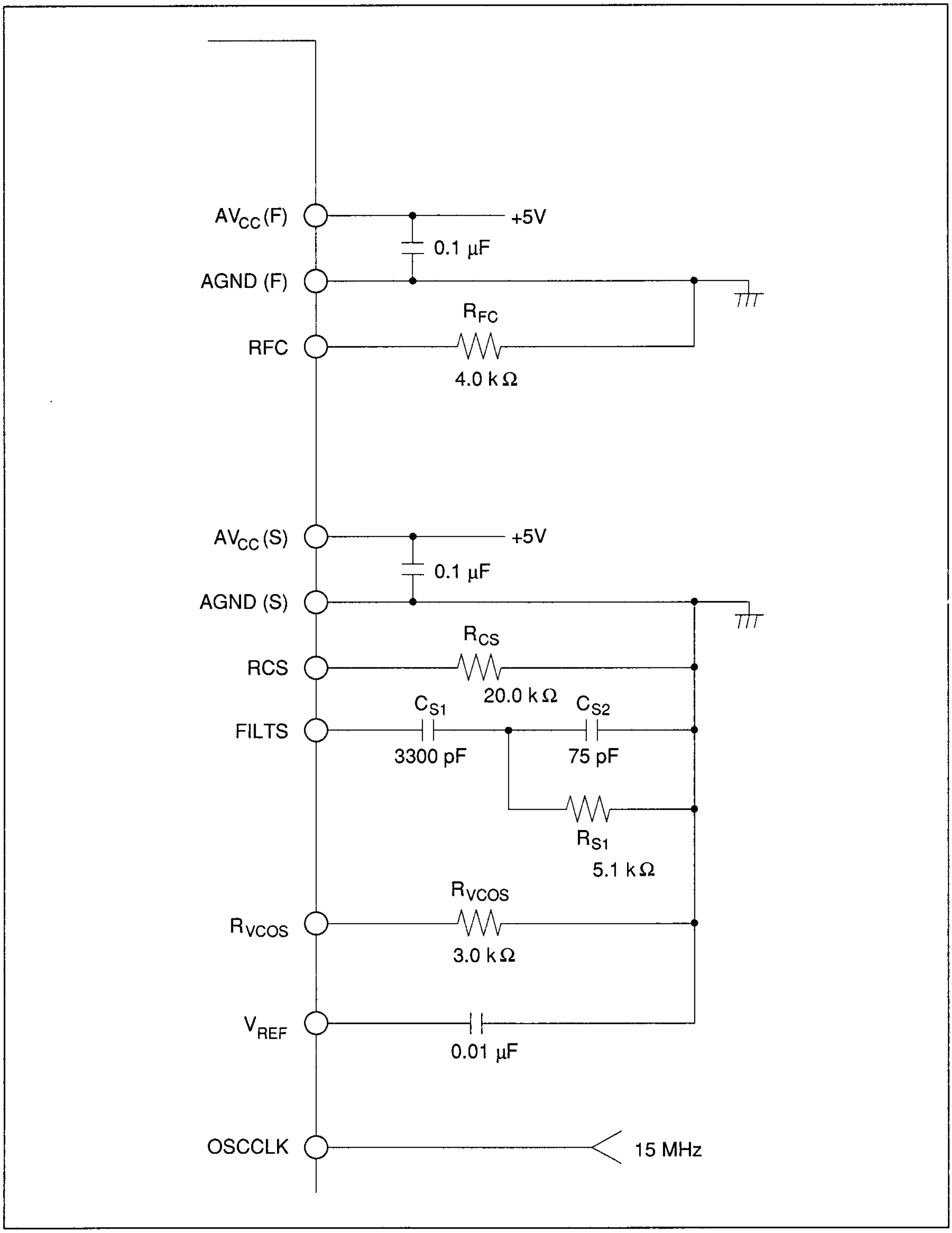
—: Don't care.

- Register 2 vs. $I_{CS}$ (when $R_{CS}$ = 20.0 [kΩ])

**Register 2**

| Address $A_2$ | $A_1$ | $A_0$ | Data $D_7$ | $D_6$ | $D_5$ | $D_4$ | $D_3$ | $D_2$ | $D_1$ | $D_0$ | $N_C$ | $I_{CS}$ [μA] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 1 | 0 | — | — | — | — | — | 0 | 0 | 0 | 0 | 250.00 |
| 0 | 1 | 0 | — | — | — | — | — | 0 | 0 | 1 | 1 | 281.25 |
| 0 | 1 | 0 | — | — | — | — | — | 0 | 1 | 0 | 2 | 312.50 |
| 0 | 1 | 0 | — | — | — | — | — | 0 | 1 | 1 | 3 | 343.75 |
| 0 | 1 | 0 | — | — | — | — | — | 1 | 0 | 0 | 4 | 375.00 |
| 0 | 1 | 0 | — | — | — | — | — | 1 | 0 | 1 | 5 | 406.25 |
| 0 | 1 | 0 | — | — | — | — | — | 1 | 1 | 0 | 6 | 437.50 |
| 0 | 1 | 0 | — | — | — | — | — | 1 | 1 | 1 | 7 | 468.75 |

## External Component Connection Example



# Sample Register Settings

## Sample Register Settings

| Address | | | Data | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| $A_2$ | $A_1$ | $A_0$ | $D_7$ | $D_6$ | $D_5$ | $D_4$ | $D_3$ | $D_2$ | $D_1$ | $D_0$ |
| 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| 0 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 1 |
| 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 1 |
| 1 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 1 |
| 1 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 1 |
| 1 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 0 |
| | | | MSB | | | | | | | LSB |

## Setting Conditions for Sample Register Settings

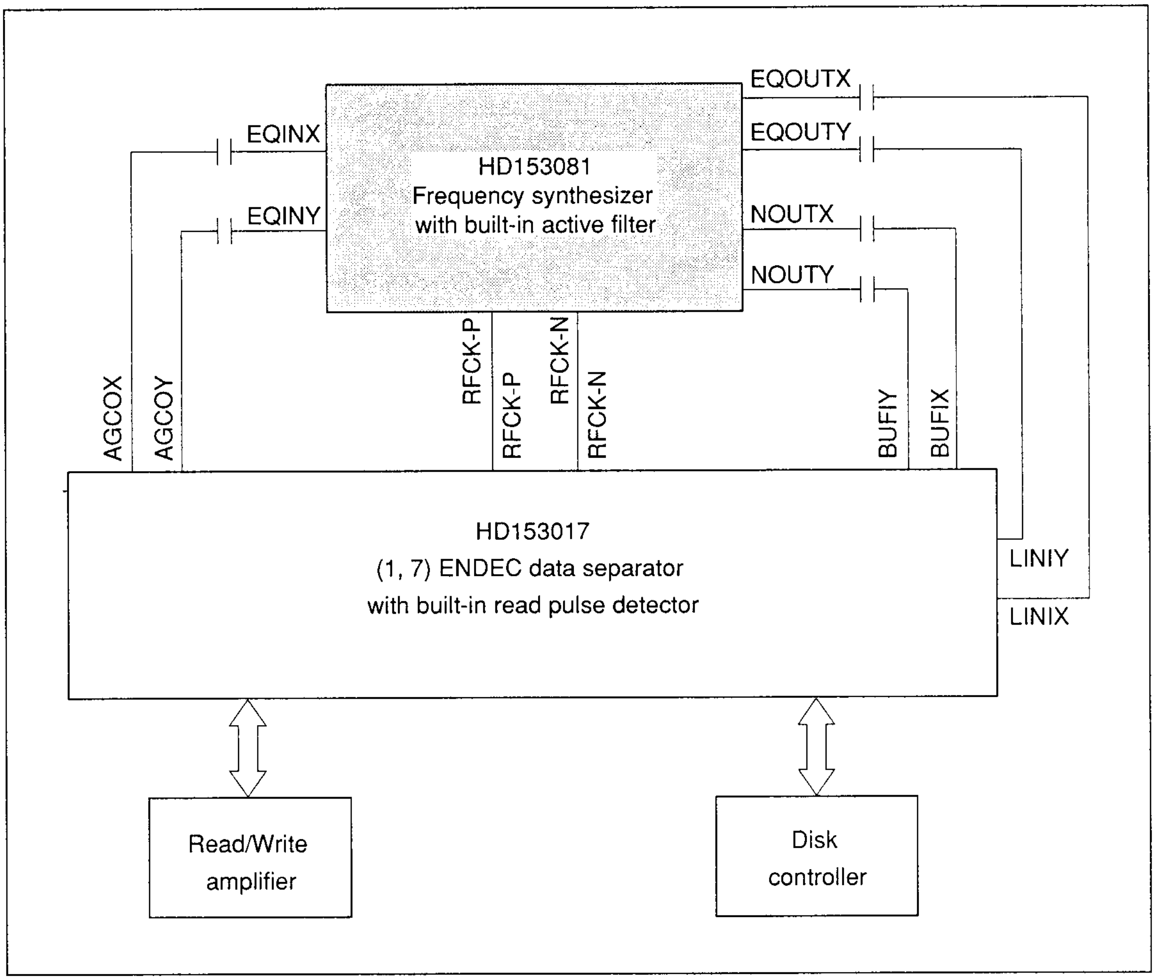
- Programmable filter

| | |
|---|---|
| Cutoff frequency, $f_C$ | 20 MHz |
| Boost level, $g_b$ | 9 dB |

- Frequency synthesizer

| | |
|---|---|
| Input clock frequency, $f_{OSCCLK}$ | 15 MHz |
| Step frequency, $f_{STEP}$ | 0.234375 MHz |
| Output clock frequency, $f_{OS}$ | 30 MHz |
| Unlock detection sensitivity $N_{ULD}$ | 2 |
| Output clock level | Pseudo-ECL |

## Application Circuit Example



## Absolute Maximum Ratings ($T_a$ = 25°C)

| Item | Symbol | Rating | Unit | Applicable Pins |
|---|---|---|---|---|
| Power supply voltage | $V_{CC}$ | 7 | V | $AV_{CC}$ (S), $AV_{CC}$ (F) $DV_{CC}$, $DV_{CC}$ (ECL) |
| Input voltage | $V_i$ | –0.3 to +5.5 | V | $\overline{RESET}$, $\overline{CS}$, $\overline{WE}$, $\overline{RE}$, $D_0$ to $D_7$, $A_0$ to $A_2$, OSCCLK, WG |
| Output voltage | $V_o$ | 5.5 | V | $D_0$ to $D_7$, $\overline{ULD}$, RFCK-T |
| Output current 1 | $I_{o1}$ | –25 | mA | RFCK-P, RFCK-N |
| Output current 2 | $I_{o2}$ | –0.5 | mA | $R_{FC}$ |
| Output current 3 | $I_{o3}$ | –0.3 | mA | $R_{CS}$ |
| Output current 4 | $I_{o4}$ | –1.5 | mA | $R_{VCOS}$ |
| Operating temperature | $T_{opr}$ | 0 to +70 | °C | |
| Storage temperature | $T_{stg}$ | –55 to +125 | °C | |
| Maximum operating junction temperature | $T_{jmax}$ | +125 | °C | |

## Electrical Characteristics

### DC Characteristics

| Item | Symbol | Min | Typ | Max | Unit | Test Conditions | Applicable Pins |
|---|---|---|---|---|---|---|---|
| Power supply voltage | $V_{CC}$ | 4.75 | 5.00 | 5.25 | V | | $AV_{CC}$ (S), $AV_{CC}$ (F) $DV_{CC}$, $DV_{CC}$ (ECL) |
| Input voltage | $V_{IH}$ | 2.2 | — | — | V | | *1 |
| | $V_{IL}$ | — | — | 0.8 | V | | *1 |
| Input current | $I_{IH}$ | — | — | 20 | µA | $V_{CC}$ = 5.25 V $V_I$ = 2.7 V | *1 |
| | $I_{IL}$ | — | — | –400 | µA | $V_{CC}$ = 5.25V $V_I$ = 0.4 V | *1 |
| Output voltage | $V_{OH}$ | 2.7/ $V_{CC}$ –1.1 | –/ $V_{CC}$ –0.8 | — | V | $V_{CC}$ = 4.75 V $I_{OH}$ = –400 µA/ $R_L$ = 510 Ω | *2/*3 |
| | $V_{OL}$ | — | –/ $V_{CC}$ –1.8 | 0.5/ $V_{CC}$ –1.5 | V | $V_{CC}$ = 4.75 V $I_{OL}$ = 8 mA/ $R_L$ = 510 Ω | *2/*3 |
| Output amplitude | $I_{SW}$ | 0.69 | 1.0 | — | V | $V_{CC}$ = 4.75 V $R_L$ = 510 Ω | *3 |
| Output shorted current | $I_{OS}$ | –2.0 | — | –120 | mA | $V_{CC}$ = 5.25 V | *2 |
| Input clamp voltage | $V_{IK}$ | — | — | –1.5 | V | $V_{CC}$ = 4.75 V $I_{OH}$ = –18 mA | *1 |
| Current dissipation | $I_{CC}$ | — | 115 | 135 | mA | $V_{CC}$ = 5.25 V*4 | $AV_{CC}$ (S), $AV_{CC}$ (F) $DV_{CC}$, $DV_{CC}$ (ECL) |
| Charge pump output current | $I_{CI}$ | — | 500 | — | µA | $V_{CC}$ = 5.0 V, $R_{SC}$ = 20 kΩ $V_{FILTS}$ = 2.5 V*5 | FILTS |
| | $I_{CD}$ | — | –500 | — | µA | $V_{CC}$ = 5.0 V, $R_{SC}$ = 20 kΩ $V_{FILTS}$ = 2.5 V*5 | FILTS |
| Standby current | $I_{SB}$ | — | — | 2 | mA | Register 7, $D_7$ = "1" | $AV_{CC}$ (S), $AV_{CC}$ (F) $DV_{CC}$, $DV_{CC}$ (ECL) |

Notes: 1. $\overline{RESET}$, $\overline{CS}$, $\overline{WE}$, $\overline{RE}$, $D_0$ to $D_7$, $A_0$ to $A_2$, OSCCLK, WG
2. $D_0$ to $D_7$, $\overline{ULD}$, RFCK-T
3. RFCK-P, RFCK-N
4. When $f_c$ is set to 30 MHz, and $f_{OS}$ to 54 MHz.
5. Register 2, $D_0$ to $D_2$ = "111"

## AC Characteristics

| Item | Symbol | Min | Typ | Max | Unit | Test Conditions | Applicable Pins |
|---|---|---|---|---|---|---|---|
| Reset time | $t_{RS}$ | 50 | — | — | ns | | $\overline{RESET}$ |
| Oscillator clock input duty | | 30 | — | 70 | % | | OSCCLK |
| Standby recovery time | | 10 | — | — | ms | | |
| Data transfer rate | | 15 | — | 40 | Mbps | When (1,7) code is used. | |

## Registers ($T_a$ = 25°C, $V_{CC}$ = 5.0 V)

| Item | Symbol | Min | Typ | Max | Unit | Test Conditions | Applicable Pins | Notes |
|---|---|---|---|---|---|---|---|---|
| Register write address setup time | $t_{ASW}$ | 0 | — | — | ns | $V_{CC}$ = 4.75 V | $A_0$ to $A_3$ | Figure 5 |
| Register write address hold time | $t_{AHW}$ | 10 | — | — | ns | $V_{CC}$ = 4.75 V | $A_0$ to $A_3$ | Figure 5 |
| Register write CS setup time | $t_{CSW}$ | 0 | — | — | ns | $V_{CC}$ = 4.75 V | $\overline{CS}$ | Figure 5 |
| Register write CS hold time | $t_{CHW}$ | 10 | — | — | ns | $V_{CC}$ = 4.75 V | $\overline{CS}$ | Figure 5 |
| Data setup time | $t_{DSW}$ | 10 | — | — | ns | $V_{CC}$ = 4.75 V | $D_0$ to $D_4$ | Figure 5 |
| Register write data hold time | $t_{DHW}$ | 10 | — | — | ns | $V_{CC}$ = 4.75 V | $D_0$ to $D_4$ | Figure 5 |
| Register write WE pulse width | $t_{WW}$ | 50 | — | — | ns | $V_{CC}$ = 4.75 V | $\overline{WE}$ | Figure 5 |
| Register read address setup time | $t_{ASR}$ | 0 | — | — | ns | $V_{CC}$ = 4.75 V | $A_0$ to $A_2$ | Figure 6 |
| Register read address hold time | $t_{AHR}$ | 10 | — | — | ns | $V_{CC}$ = 4.75 V | $A_0$ to $A_2$ | Figure 6 |
| Register read CS setup time | $t_{CSR}$ | 0 | — | — | ns | $V_{CC}$ = 4.75 V | $\overline{CS}$ | Figure 6 |
| Register read CS hold time | $t_{CHR}$ | 10 | — | — | ns | $V_{CC}$ = 4.75 V | $\overline{CS}$ | Figure 6 |
| Register read data setup time | $t_{DSR}$ | — | 5 | 40 | ns | $V_{CC}$ = 4.75 V | $D_0$ to $D_4$ | Figure 6 |
| Register read data hold time | $t_{DHR}$ | 5 | 10 | 20 | ns | $V_{CC}$ = 4.75 V | $D_0$ to $D_4$ | Figure 6 |
| Register read output on time | $t_{DBO}$ | 5 | — | — | ns | $V_{CC}$ = 4.75 V | $D_0$ to $D_4$ | Figure 6 |

**Registers ($T_a$ = 25°C, $V_{CC}$ = 5.0 V) (cont)**

| Item | Symbol | Min | Typ | Max | Unit | Test Conditions | Applicable Pins | Notes |
|---|---|---|---|---|---|---|---|---|
| Register read output off time | $t_{DBR}$ | — | — | 20 | ns | $V_{CC}$ = 4.75 V | $D_0$ to $D_4$ | Figure 6 |
| Register read RE pulse width | $t_{RW}$ | 50 | — | — | ns | $V_{CC}$ = 4.75 V | $\overline{RE}$ | Figure 6 |
| Read/Write switching time: W to R | $t_{WTR}$ | 50 | — | — | ns | $V_{CC}$ = 4.75 V | $\overline{WE}$, $\overline{RE}$ | Figure 7 |
| Read/Write switching time: R to W | $t_{RTW}$ | 50 | — | — | ns | $V_{CC}$ = 4.75 V | $\overline{WE}$, $\overline{RE}$ | Figure 7 |
| Filter cutoff frequency | fc | 5 | — | 30 | MHz | EQOUTX, Y<br>NOUTX, Y | | |
| Filter cutoff frequency accuracy | fca | –15 | — | +15 | % | EQOUTX, Y<br>NOUTX, Y | | |
| Filter cutoff frequency setting DAC step size | | — | 0.3 | — | MHz | EQOUTX, Y<br>NOUTX, Y | | |
| Filter boost level | gb | 0 | — | 15 | dB | EQOUTX, Y<br>NOUTX, Y | | |
| Filter boost level accuracy | gba | –1 | — | +1 | dB | EQOUTX, Y<br>NOUTX, Y | gb = 15 | |
| Filter boost level setting DAC step size | | — | 0.6 | — | × | EQOUTX, Y<br>NOUTX, Y | | |
| Output differential gain (normal) | DGN | 0.9 | — | 1.1 | V/V | NOUTX, Y | f = 0.2 fc,<br>gb = 0 | |
| Output differential gain (differential) | DGD | 0.9<br>DGN | — | 1.1<br>DGN | V/V | EQOUTX, Y | f = 0.67 fc,<br>gb = 0 | |
| Differential input dynamic range | $V_{in}$ | 2.5 | — | 3.5 | $V_{P-P}$ | EQINX, Y | f = 0.67 fc,<br>THD = 1% | |
| Differential output dynamic range | $V_{out}$ | 2.5 | — | 3.5 | $V_{P-P}$ | EQOUTX, Y<br>NOUTX, Y | f = 0.67 fc,<br>THD = 1% | |
| Differential input resistance | $R_{in}$ | — | 10 | — | kΩ | EQINX, Y | | |
| Output sink current | $I_o$– | — | — | 2.0 | mA | EQOUTX, Y<br>NOUTX, Y | | |

**Registers ($T_a$ = 25°C, $V_{CC}$ = 5.0 V) (cont)**

| Item | Symbol | Min | Typ | Max | Unit | Test Conditions | Applicable Pins | Notes |
|---|---|---|---|---|---|---|---|---|
| Group delay variance (gb = 0) | Gd0 | –3 | — | +3 | % | EQOUTX, Y<br>NOUTX, Y | f = 0.2 fc to fc | |
| Group delay variance (gb = 15) | Gd1 | –3 | — | +3 | % | EQOUTX, Y<br>NOUTX, Y | f = 0.2 fc to fc | |
| Output noise (normal) | Nn | — | 3 | — | mVrms | NOUTX, Y | gb = 0 | |
| Output noise (differential) | Nd | — | 6 | — | mVrms | EQOUTX, Y | gb = 0 | |
| VCO maximum oscillator frequency | | 100 | — | — | MHz | RFCK-P, -N<br>RFCK-T | $R_{VCOS}$ = 750Ω | |
| VCO center frequency | | 57 | 60 | 63 | MHz | RFCK-P, -N<br>RFCK-T | $R_{VCSO}$ = 3 kΩ | |
| VCO clamping frequency upper limit | | 68.4 | 72 | — | MHz | RFCK-P, -N<br>RFCK-T | $R_{VCSO}$ = 3 kΩ | |
| VCO clamping frequency lower limit | | — | 48 | 50.4 | MHz | RFCK-P, -N<br>RFCK-T | $R_{VCSO}$ = 3 kΩ | |
| VCO gain | | 64 | 80 | 96 | Mrad/S•V | RFCK-P, -N<br>RFCK-T | $R_{VCSO}$ = 3 kΩ<br>Register 1<br>"11111111" | |
| Synthesizer phase pull-in time | | | — | — | 1.0 | ms | | |
| Synthesizer capture range | | ±10 | — | — | % | | | |
| Synthesizer lock range | | ±10 | — | — | % | | | |

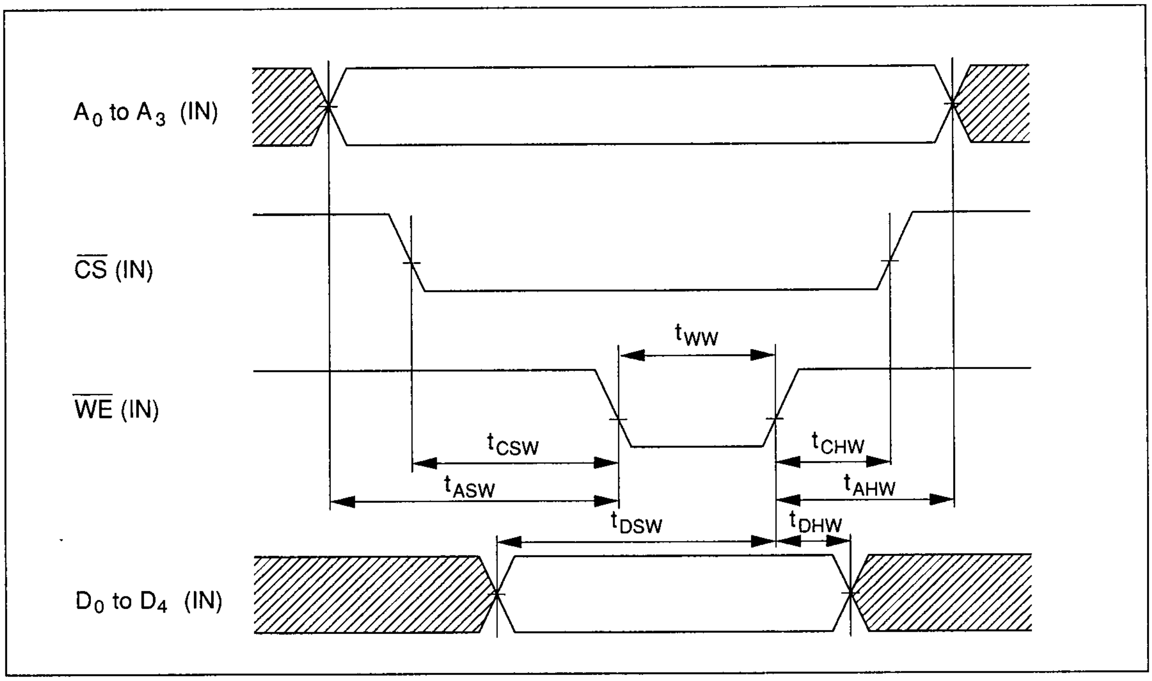



**Figure 5 Register Write Timing**

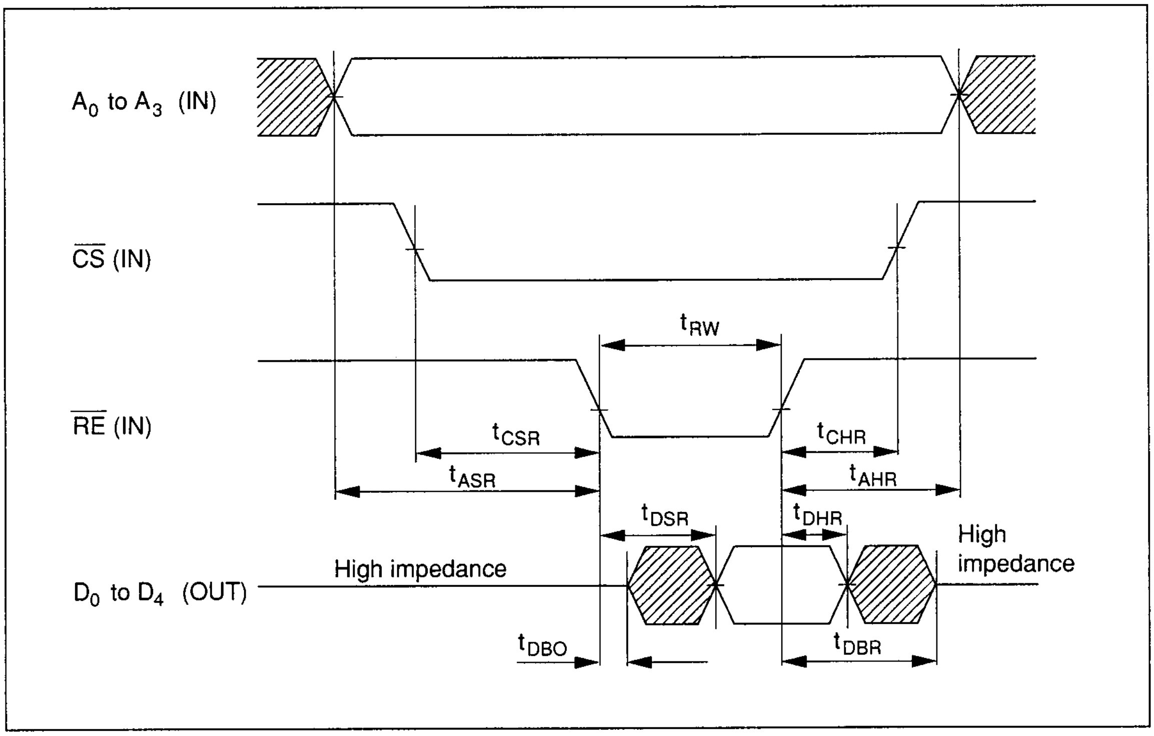



**Figure 6 Register Read Timing**

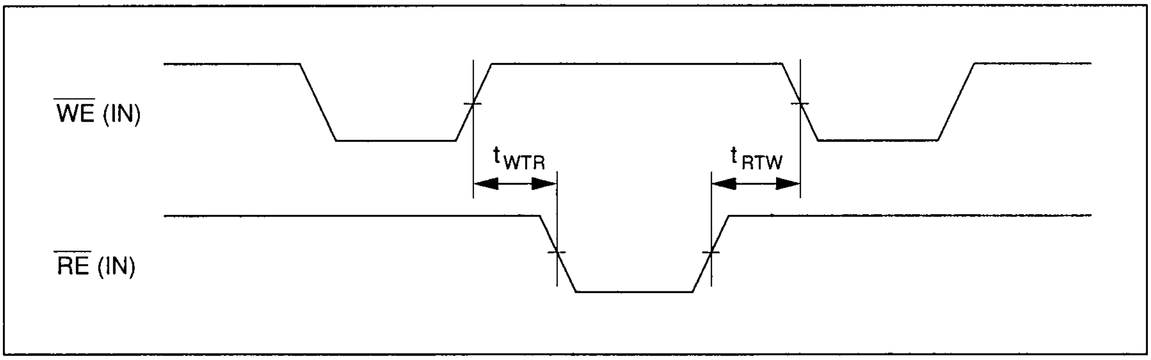
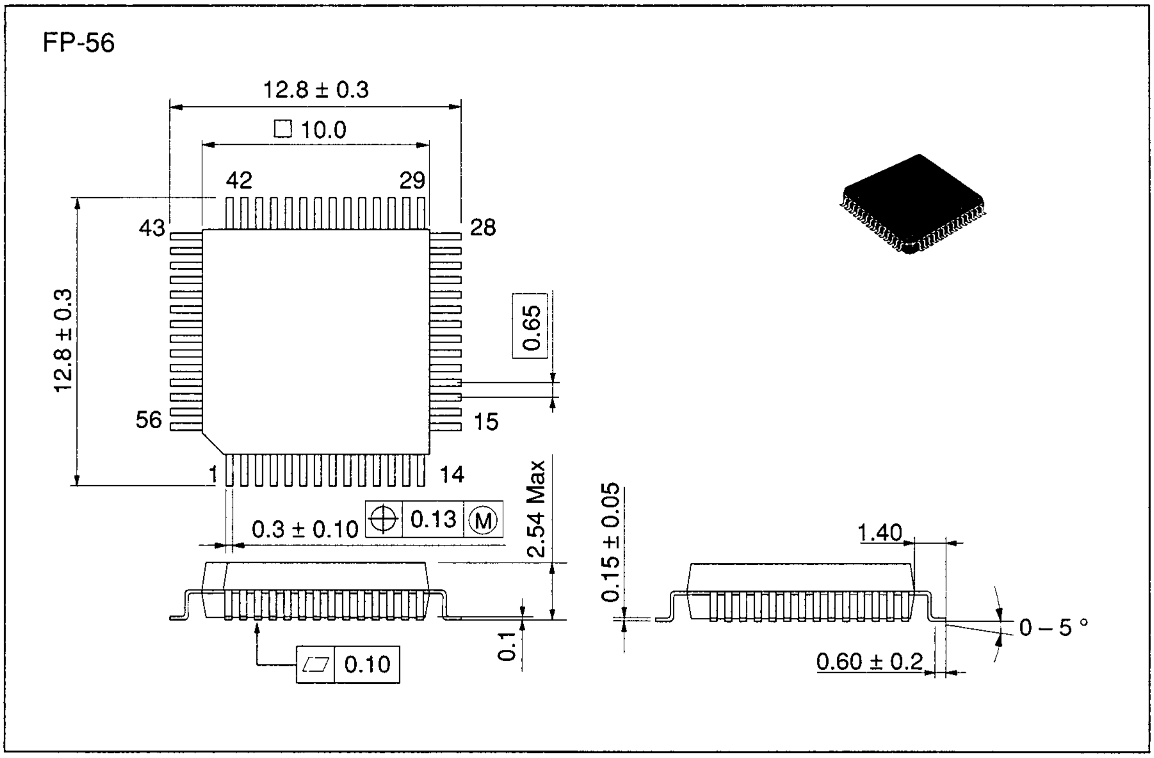



**Figure 7 Timing for Switching between Register Read and Write**

## Package Dimensions

Unit: mm



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