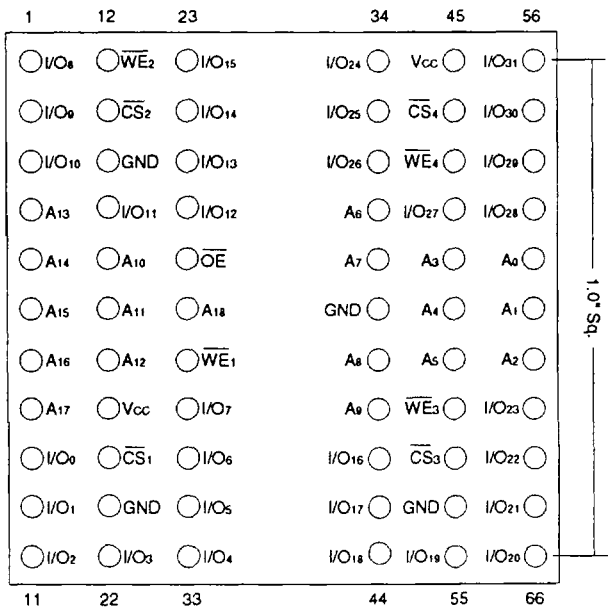

FIGURE 1 — Pin Configuration
Top View

I/O_{0-31}	Data Inputs/Outputs
A_{0-18}	Address Inputs
$\overline{WE}_{1-4}$	Write Enables
$\overline{CS}_{1-4}$	Chip Selects
$\overline{OE}$	Output Enable
V_{CC}	Power Supply
GND	Ground

Pin Description

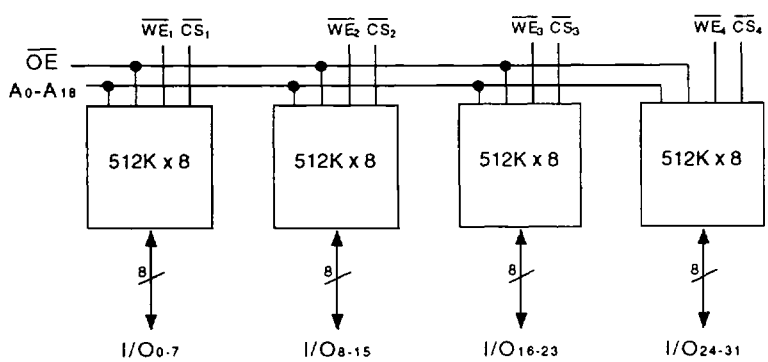

FIGURE 2 — Block Diagram

WS-512K32-XHX

ADVANCED*
16 Megabit CMOS SRAM Module

FEATURES

- **Access Times of 25nS to 120nS**
- **66-pin, PGA Type, 1.38 inch square HIP Package, Hermetic Ceramic Package**
- **User Configurable as 512Kx32, 1024Kx16 or 2Mx8**
- **Battery Back-Up Operation**
- **Commercial, Industrial and Military Temperature Ranges**
- **TTL Compatible Inputs and Outputs**
- **Low Power CMOS Fully Static Design**
- **5 Volt Power Supply**
- **Built in Decoupling Caps and Multiple Ground Pins for Low Noise Operation**

DESCRIPTION

The White Technology WS-512K32-XHX is a 16-megabit CMOS SRAM module organized as 512K words by 32 bits; 1024K x 16 or 2M x 8. The module is constructed on a multilayer ceramic substrate, hermetically sealed, with a welded metal cover, hex-in-line package (HIP) utilizing four 512K x 8 SRAM devices.

This device is part of White Technology's "WHIP" family of memory subsystems. These modules are compatible with most 66-pin HIP packaged SRAM, EEPROM and Flash memory modules.

The WS-512K32-XHX is available with access times of 25 to 120nS over the commercial and military temperature ranges.

* This data sheet describes a product under development and is subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol		Unit
Operating Temperature	T_A	-55 to +125	°C
Storage Temperature Range	T_{STG}	-65 to +150	°C
Supply Voltage	V_{CC}	-0.5 to 7.0	V
Signal Voltages Any Pin	V_G	-0.5 to 7.0	V

TRUTH TABLE

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	A0-A18	Mode	Data I/O	Device Current
H	X	X	X	Standby	High Z	Standby
L	L	H	Stable	Read	Data Out	Active
L	X	L	Stable	Write	Data In	Active
L	H	H	Stable	Out Disable	High Z	Active

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V_{CC}	4.5	5.5	V
Input High Voltage	V_{IH}	2.2	V_{CC} + 0.3	V
Input Low Voltage	V_{IL}(1)	-0.5	+0.8	V
Operating Temp. (Mil.)	T_A	-55	+125	°C

(1) V_{IL} (min.) = 3.0V for pulse width less than 20nS.

CAPACITANCE

(@ T_A = 25°C)

Parameter	Symbol	Condition	Max	Unit
* Input Capacitance	C_{IN}	V_{IN} = 0V, f = 1.0 MHz	30	pF
* I/O Capacitance	C_{OUT}	V_{OUT} = 0V, f = 1.0 MHz	10	pF

* This parameter is guaranteed by design but not tested.

DC CHARACTERISTICS - 5V

(V_{CC} = 5V, V_{SS} = 0V, T_A = -55°C TO 125°C)

Parameter	Sym	Conditions	-25 Typ	-25 Max	-35 Typ	-35 Max	-45 Typ	-45 Max	-55 Typ	-55 Max	Units
Input Leakage Current	I_{LI}	V_{CC} = Max, V_{IN} = GND or V_{CC}								10	µA
Output Leakage Current	I_{LO}	$\overline{CS}$ = V_{IH}, $\overline{OE}$ = V_{IH}, V_{OUT} = GND to V_{CC}								2	µA
Operating Supply Current x 32 Mode	I_{CC} x 32	$\overline{CS}$ = V_{IL}, $\overline{OE}$ = V_{IH}, Duty Cycle = Max							240	500	mA
Operating Supply Current x 16 Mode	I_{CC} x 16	$\overline{CS}$ = V_{IL}, $\overline{OE}$ = V_{IH}, Duty Cycle = Max							150	300	mA
Operating Supply Current x 8 Mode	I_{CC} x 8	$\overline{CS}$ = V_{IL}, $\overline{OE}$ = V_{IH}, Duty Cycle = Max							80	160	mA
Standby Current	I_{SB}	$\overline{CS}$ = V_{CC}, $\overline{OE}$ = V_{IH}, Duty Cycle = Max								500	µA
Output Low Voltage	V_{OL}	I_{OL} = 8mA, V_{CC} = Min									V
		I_{OL} = 2.1mA, V_{CC} = Min								0.4	V
Output High Voltage	V_{OH}	I_{OH} = -4.0mA, V_{CC} = Min									V
		I_{OH} = -1.0mA, V_{CC} = Min								2.4	V

Parameter	Sym	Conditions	-70 Typ	-70 Max	-85 Typ	-85 Max	-100 Typ	-100 Max	-120 Typ	-120 Max	Units
Input Leakage Current	I_{LI}	V_{CC} = Max, V_{IN} = GND or V_{CC}		10		10		10		10	µA
Output Leakage Current	I_{LO}	$\overline{CS}$ = V_{IH}, $\overline{OE}$ = V_{IH}, V_{OUT} = GND to V_{CC}		2		2		2		2	µA
Operating Supply Current x 32 Mode	I_{CC} x 32	$\overline{CS}$ = V_{IL}, $\overline{OE}$ = V_{IH}, Duty Cycle = Max	240	500	240	500	240	400	240	400	mA
Operating Supply Current x 16 Mode	I_{CC} x 16	$\overline{CS}$ = V_{IL}, $\overline{OE}$ = V_{IH}, Duty Cycle = Max	150	300	150	300	150	200	150	200	mA
Operating Supply Current x 8 Mode	I_{CC} x 8	$\overline{CS}$ = V_{IL}, $\overline{OE}$ = V_{IH}, Duty Cycle = Max	80	160	80	160	80	120	80	120	mA
Standby Current	I_{SB}	$\overline{CS}$ ≥ V_{CC} - .2V		500		500		500		500	µA
Output Low Voltage	V_{OL}	I_{OL} = 2.1mA		0.4		0.4		0.4			V
Output High Voltage	V_{OH}	I_{OH} = -1.0mA		2.4		2.4		2.4			V

DC CHARACTERISTICS - 3V

(Vcc = 5V, Vss = 0V, TA = -55°C TO 125°C)

Parameter	Sym	Conditions	-25		-35		-45		-55		Units
			Typ	Max	Typ	Max	Typ	Max	Typ	Max	
Input Leakage Current	I_{LI}	Vcc = Max, VIN = GND or Vcc								10	µA
Output Leakage Current	I_{LO}	$\overline{CS}$ = VIH, $\overline{OE}$ = VIH, VOUT = GND to Vcc								2	µA
Operating Supply Current x 32 Mode	Icc x 32	$\overline{CS}$ = VIL, $\overline{OE}$ = VIH, Duty Cycle = Max							80	200	mA
Operating Supply Current x 16 Mode	Icc x 16	$\overline{CS}$ = VIL, $\overline{OE}$ = VIH, Duty Cycle = Max							60	100	mA
Operating Supply Current x 8 Mode	Icc x 8	$\overline{CS}$ = VIL, $\overline{OE}$ = VIH, Duty Cycle = Max							40	70	mA
Standby Current	I_{SB}	$\overline{CS}$ = Vcc, $\overline{OE}$ = VIH, Duty Cycle = Max								250	µA
Output Low Voltage	V_{OL}	IOL = 8mA, Vcc = Min									V
		IOL = 2.1mA, Vcc = Min								0.4	V
Output High Voltage	V_{OH}	IOH = -4.0mA, Vcc = Min									V
		IOH = -1.0mA, Vcc = Min								2.4	V

Parameter	Sym	Conditions	-70		-85		-100		-120		Units
			Typ	Max	Typ	Max	Typ	Max	Typ	Max	
Input Leakage Current	I_{LI}	Vcc = Max, VIN = GND or Vcc		10		10		10		10	µA
Output Leakage Current	I_{LO}	$\overline{CS}$ = VIH, $\overline{OE}$ = VIH, VOUT = GND to Vcc		2		2		2		2	µA
Operating Supply Current x 32 Mode	Icc x 32	$\overline{CS}$ = VIL, $\overline{OE}$ = VIH, Duty Cycle = Max	80	200	80	200	80	150	80	150	mA
Operating Supply Current x 16 Mode	Icc x 16	$\overline{CS}$ = VIL, $\overline{OE}$ = VIH, Duty Cycle = Max	60	100	60	100	60	80	60	80	mA
Operating Supply Current x 8 Mode	Icc x 8	$\overline{CS}$ = VIL, $\overline{OE}$ = VIH, Duty Cycle = Max	40	70	40	70	40	60	40	60	mA
Standby Current	I_{SB}	$\overline{CS}$ ≥ Vcc - .2V		250		250		250		250	µA
Output Low Voltage	V_{OL}	IOL = 2.1mA		0.4		0.4		0.4			V
Output High Voltage	V_{OH}	IOH = -1.0mA		2.4		2.4		2.4			V

AC ELECTRICAL CHARACTERISTICS

(Vcc = 5.0V, Vss = 0V, TA = -55°C TO 125°C)

Parameter Read Cycle	Symbol	-25		-35		-45		-55		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}							55		nS
Address Access Time	t_{AA}								55	nS
Data Hold from Address Change	t_{OH}							10		nS
Chip Select Access	t_{ACS}								55	nS
Output Enable to Output Valid	t_{OE}								30	nS
Chip Select to Output in Low Z	t_{CLZ}[1]							10		nS
Output Enable to Output in Low Z	t_{OLZ}[1]							5		nS
Chip Deselect to Output in High Z	t_{CHZ}[1]								20	nS
Output Disable to Output in High Z	t_{OHZ}[1]								20	nS

1. This parameter is guaranteed by design but not tested.

Parameter Read Cycle	Symbol	-70		-85		-100		-120		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	70		85		100		120		nS
Address Access Time	t_{AA}		70		85		100		120	nS
Data Hold from Address Change	t_{OH}	10		10		10		10		nS
Chip Select Access	t_{ACS}		70		85		100		120	nS
Output Enable to Output Valid	t_{OE}		40		45		50		60	nS
Chip Select to Output in Low Z	t_{CLZ}[1]	10		10		10		10		nS
Output Enable to Output in Low Z	t_{OLZ}[1]	5		5		5		5		nS
Chip Deselect to Output in High Z	t_{CHZ}[1]		25		30		35		40	nS
Output Disable to Output in High Z	t_{OHZ}[1]		25		30		35		40	nS

1. This parameter is guaranteed by design but not tested.

AC ELECTRICAL CHARACTERISTICS

(Vcc = 5.0V, TA = -55°C TO 125°C)

Parameter Write Cycle	Symbol	-25		-35		-45		-55		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
Write Cycle Time	twc							55		nS
Chip Select to End of Write	tcw							50		nS
Address Valid to End of Write	taw							50		nS
Data to Write-Time Overlap	tdw							25		nS
Data Hold from Write Time	tdh							0		nS
Write Pulse Width	twp							40		nS
Address Setup Time	tas							0		nS
Write Recovery Time	twr							0		nS
Output Active from End of Write	tow							5		nS
Write to Output in High Z	twhz[1]							0	20	nS

1. This parameter is guaranteed by design but not tested.

Parameter Write Cycle	Symbol	-70		-85		-100		-120		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
Write Cycle Time	twc	70		85		100		120		nS
Chip Select to End of Write	tcw	60		70		80		100		nS
Address Valid to End of Write	taw	60		70		80		100		nS
Data to Write-Time Overlap	tdw	30		35		40		55		nS
Data Hold from Write Time	tdh	0		0		0		0		nS
Write Pulse Width	twp	50		60		70		90		nS
Address Setup Time	tas	0		0		0		0		nS
Write Recovery Time	twr	0		0		0		0		nS
Output Active from End of Write	tow	5		5		5		5		nS
Write to Output in High Z	twhz[1]		25		30		30		45	nS

1. This parameter is guaranteed by design but not tested.

DATA RETENTION CHARACTERISTICS

(TA = -55°C TO 125°C)

Parameter	Symbol	Conditions	-25			-35			-45			-55			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Data Retention Supply Voltage	VDR	CS≥ Vcc - .2V										2.0		5.5	V
DataRetention Current	ICCDR1	Vcc = 3V											10	400	µA
	ICCDR2	Vcc = 2V											8	300	µA

Parameter	Symbol	Conditions	-70			-85			-100			-120			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Data Retention Supply Voltage	VDR	CS≥ Vcc - .2V	2.0		5.5	2.0		5.5	2.0		5.5	2.0		5.5	V
DataRetention Current	ICCDR1	Vcc = 3V		.5	8		.5	8		.5	8		.5	8	µA
	ICCDR2	Vcc = 2V		8	300		8	300		8	300		8	300	µA

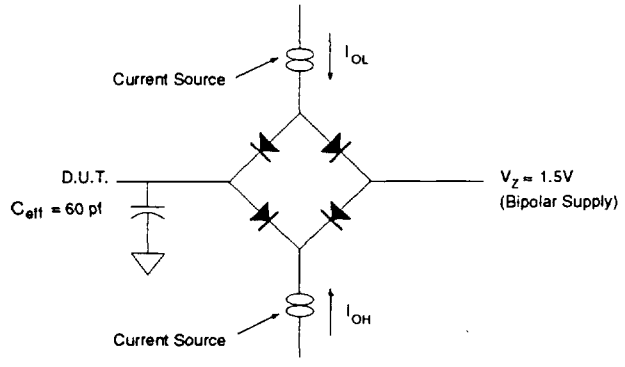

FIGURE 3 — AC Test Circuit

AC TEST CONDITIONS

Parameter	Typ.	Unit
Input Pulse Levels	V_{IL} = 0, V_{IH} = 3.0	V
Input Rise and Fall	5	nS
Input and Output Reference Level	1.5	V
Output Timing Reference Level	1.5	V

Notes:
Vz is programmable from -2V to +7V.
I_{OL} & I_{OH} programmable from 0 to 16mA.
Tester Impedance Z_O = 75 Ω.
Vz is typically the midpoint of V_{OH} and V_{OL} (i.e. (2.4 + 0.4)/2 = 1.4V).
I_{OL} & I_{OH} are adjusted to simulate a typical resistive load circuit.
ATE Tester Includes Jig Capacitance.

TIMING WAVEFORMS

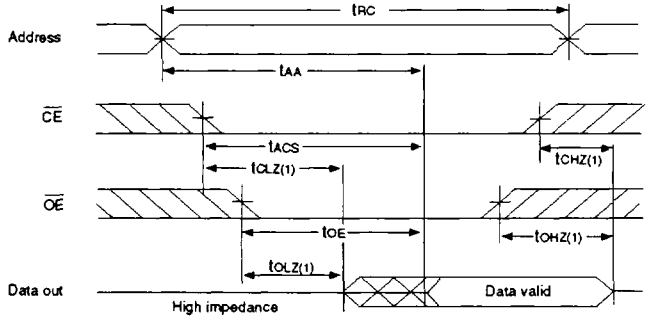

FIGURE 4 — Read Cycle Timing, $\overline{WE}$=V_{IH}

1. Measured ± 200mV steady state; guaranteed by design but not tested.

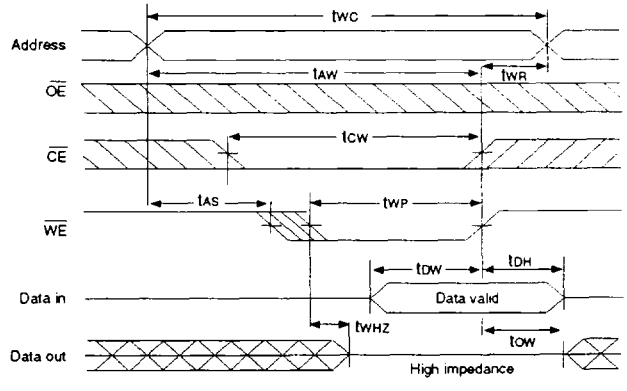

FIGURE 5 — Write Cycle Timing $\overline{WE}$ Controlled

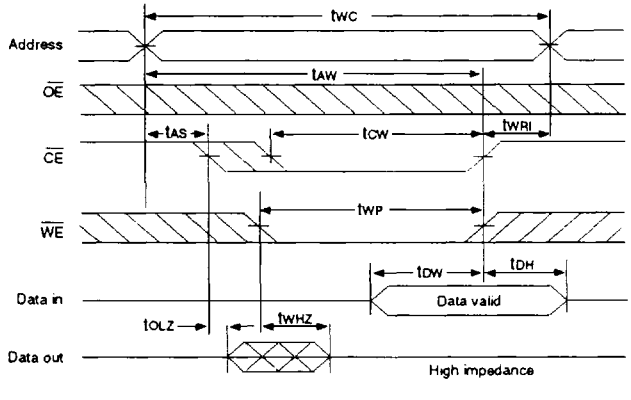

FIGURE 6 — Write Cycle Timing, CE Controlled

During I/O pins are in the output state, the data input signals of opposite phase to the utput must not be applied.

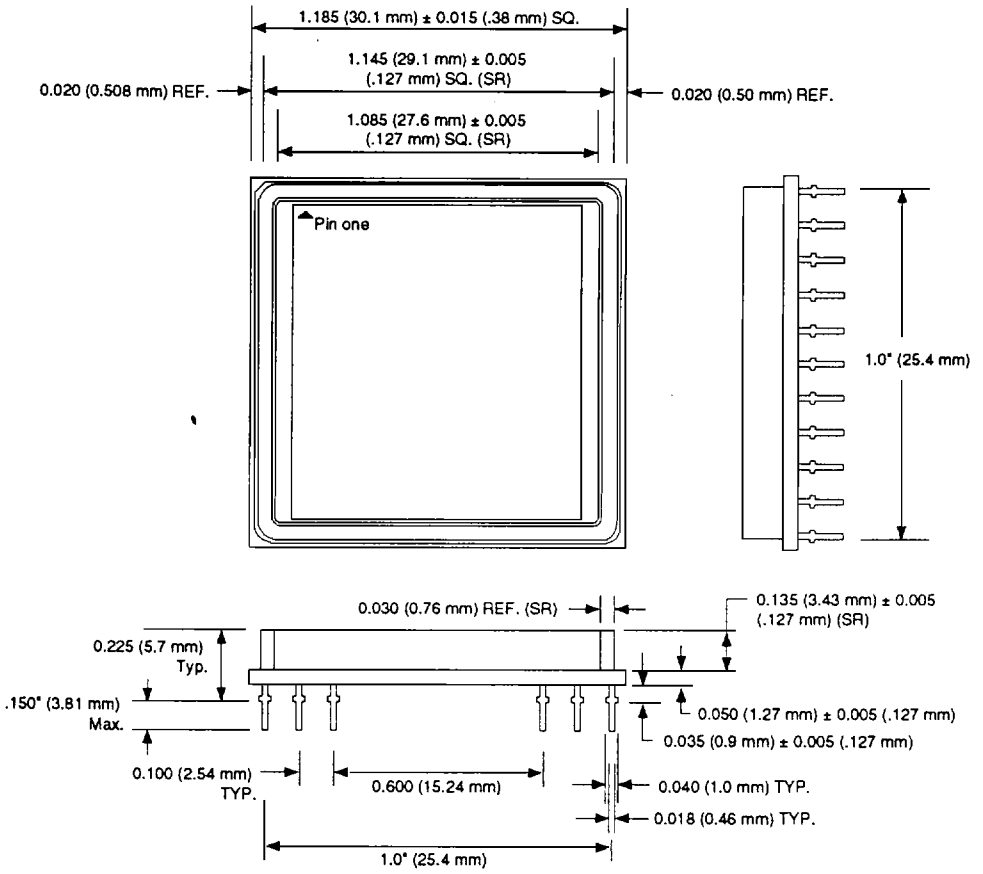

FIGURE 7 — Package Dimensions

ORDERING INFORMATION

W S - 512K32 - XXX H X

- DEVICE GRADE:
  - Q = MIL-STD-883 Compliant
  - M = Mil, -55°C to +125°C
  - I = Industrial, -40°C to 85°C
  - C = Commercial, 0 to 70°C
- PACKAGE TYPE:
  - H = Ceramic Hex in line package
- ACCESS TIME IN nS
- ORGANIZATION, 512Kx32
  - User configurable as 1024Kx16 or 2Mx8
- SRAM
- WHITE TECHNOLOGY

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