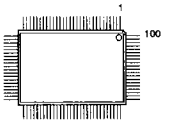
FEATURES

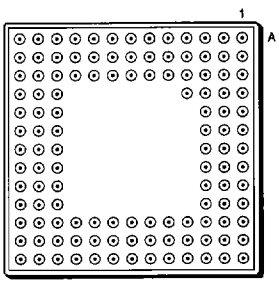
- ☐ 32 x 32 Digital crosspoint structure
- ☐ CMOS low power
- ☐ 3 ns skew, typical
- ☐ 50 MHz operation
- ☐ CMOS compatible inputs/tri-statable outputs
- ☐ Multiple package options

100-PIN QFP PACKAGE



SC11320CQ

121-PIN PGA PACKAGE (Bottom View)

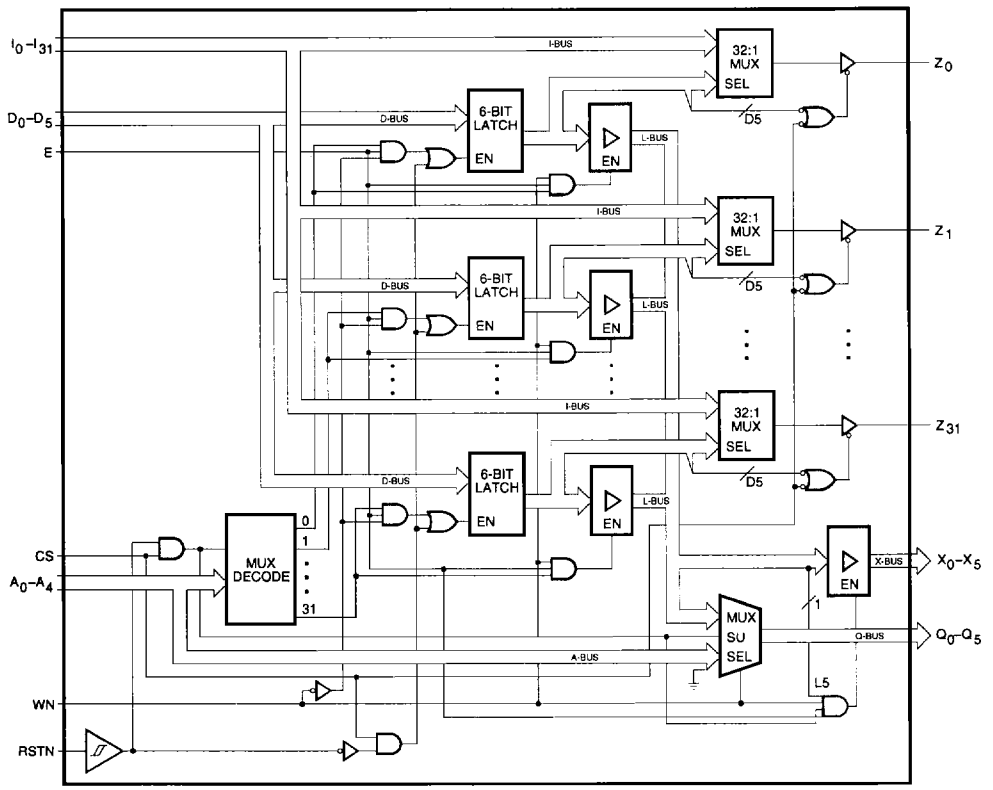


SC11320CT

GENERAL DESCRIPTION

The 32 x 32 Crosspoint Switch is a design which allows each of the 32 outputs to be independently connected to any of its 32 inputs. Thirty-two 1 of 32 muxes are employed (each with its own register which the user loads to specify the desired input for that output channel). Outputs can also be individually tri-stated by setting bit D5 low when loading these same registers. See Table 1 for pin definitions.

BLOCK DIAGRAM



-Bus: Channel input data to be switched.
)-Bus: 32:1 MUX Register input data.
\-Bus: Address of specific latch whose contents is to be read on X-bus.
(-Bus: Permits readback of state of latch addressed via A-bus (tri-state). Only the active latch enabled by L5 (most significant bit) will be read*. *Useful in multi-chip applications.

Q-Bus: Same as X-bus. Also feeds back address of latch selected. (Defaults low/not tri-state).
Z-Bus: Channel output data.

PIN DEFINITIONS Table 1

100 Pin QFP Pad #	121 Pin PGA Pin #		Name	I/O Type	Description
100	120	A1	V_{SS}	Power	Pad ring ground.
99	119	B3	N.C.		No connection.
98	118	C4	FACTORY TEST		Float (do not ground).
N.C.	117	A2	N.C.		No connection.
N.C.	116	A3	N.C.		No connection.
97	115	B4	Z28	Output	Output channel (tri-state).
96	114	C5	Z29	Output	Output channel (tri-state).
95	113	A4	Z30	Output	Output channel (tri-state).
94	112	B5	Z31	Output	Output channel (tri-state).
N.C.	111	A5	N.C.		No connection.
N.C.	110	C6	N.C.		No connection.
N.C.	109	B6	N.C.		No connection.
N.C.	108	A6	N.C.		No connection.
N.C.	107	A7	N.C.		No connection.
93	106	C7	V_{DD}	Power	Interal logic +5.0 VDC.
92	105	B7	V_{SS}	Power	Internal logic ground.
N.C.	104	A8	MZ	Output	Not supported.
91	103	B8	D0	CMOS Input	Mux register input data (write operation).
90	102	C8	D1	CMOS Input	Mux register input data (write operation).
89	101	A9	D2	CMOS Input	Mux register input data (write operation).
88	100	B9	D3	CMOS Input	Mux register input data (write operation).
87	99	A10	D4	CMOS Input	Mux register input data (write operation).
86	98	C9	D5	CMOS Input	Register data for output tri-state control.
85	97	B10	I0	CMOS Input	Channel input data.
84	96	A11	Z0	Output	Output channel (tri-state).
83	95	B11	Z1	Output	Output channel (tri-state).
82	94	C10	Z2	Output	Output channel (tri-state).
81	93	A12	Z3	Output	Output channel (tri-state).
N.C.	92	B12	N.C.		No connection.
D.B.	91	C11	V_{SS}	Power	Pad ring ground.
80	90	A13	V_{DD}	Power	Pad ring +5.0 VDC.
79	89	C12	I1	CMOS Input	Channel input data.
78	88	D11	I2	CMOS Input	Channel input data.
77	87	B13	I3	CMOS Input	Channel input data.
76	86	C13	I4	CMOS Input	Channel input data.
75	85	D12	I5	CMOS Input	Channel input data.
74	84	E11	I6	CMOS Input	Channel input data.
73	83	D13	I7	CMOS Input	Channel input data.
72	82	E12	Z4	Output	Channel output (tri-state).
71	81	E13	Z5	Output	Channel output (tri-state).
70	80	F11	Z6	Output	Channel output (tri-state).
69	79	F12	Z7	Output	Channel output (tri-state).
68	78	F13	Z8	Output	Channel output (tri-state).
D.B.	77	G13	V_{SS}	Power	Pad ring ground.
D.B.	76	G11	V_{SS}	Power	Pad ring ground.
N.C.	75	G12	V_{DD}	Power	Pad ring +5.0 VDC.
67	74	H13	Z9	Output	Channel output (tri-state).
66	73	H12	Z10	Output	Channel output (tri-state).

100 Pin QFP Pad #	120 Pin PGA Pin #		Name	I/O Type	Description
65	72	H11	Z11	Output	Channel output (tri-state).
64	71	J13	Z12	Output	Channel output (tri-state).
63	70	J12	Z13	Output	Channel output (tri-state).
62	69	K13	I8	CMOS Input	Channel input data.
61	68	J11	I9	CMOS Input	Channel input data.
60	67	K12	I10	CMOS Input	Channel input data.
59	66	L13	I11	CMOS Input	Channel input data.
58	65	L12	I12	CMOS Input	Channel input data.
57	64	K11	I13	CMOS Input	Channel input data.
56	63	M13	I14	CMOS Input	Channel input data.
55	62	M12	I15	CMOS Input	Channel input data.
	61	L11	V_{DD}	Power	Pad ring +5.0 VDC.
D.B.	60	N13	V_{SS}	Power	Pad ring ground.
54	59	M11	X5	Output	Bit 5 of L-Bus (tri-state).
53	58	L10	Z14	Output	Channel output (tri-state).
52	57	N12	Z15	Output	Channel output (tri-state).
51	56	N11	Z16	Output	Channel output (tri-state).
50	55	M10	Z17	Output	Channel output (tri-state).
49	54	L9	I16	CMOS Input	Channel input data.
48	53	N10	I17	CMOS Input	Channel input data.
47	52	M9	A0	CMOS Input	Address for channel mux selection.
46	51	N9	A1	CMOS Input	Address for channel mux selection.
45	50	L8	A2	CMOS Input	Address for channel mux selection.
44	49	M8	A3	CMOS Input	Address for channel mux selection.
43	48	N8	A4	CMOS Input	Address for channel mux selection.
42	47	N7	V_{DD}	Power	Internal logic +5.0 VDC.
41	46	L7	X0	Output	Bit 0 of L-Bus (tri-state).
D.B.	45	M7	V_{SS}	Power	Internal logic ground.
40	44	N6	E	CMOS Input	Enable. Active high enable for read and write operations.
39	43	M6	WN	CMOS Input	Write Not. Active low write strobe.
38	42	L6	RSTN	CMOS Input	Reset Not. Active low chip reset (Schmitt trigger input).
37	41	N5	CS	CMOS Input	Chip Select. Active high enable for all operations. (Z and X outputs float when CS is low.)
36	40	M5	Q0	Output	A-Bus contents (write operation). L-Bus contents (read operation).
35	39	N4	Q1	Output	
34	38	L5	Q2	Output	
33	37	M4	Q3	Output	
32	36	N3	Q4	Output	
31	35	M3	Q5	Output	Mux register output data (read operation).
30	34	L4	X1	Output	Bit 1 of L-Bus (tri-state).
29	33	N2	X2	Output	Bit 2 of L-Bus (tri-state).
28	32	M2	X3	Output	Bit 3 of L-Bus (tri-state).
27	31	L3	VSS	Power	Pad ring ground.
	30	N1	V_{DD}	Power	Pad ring +5.0 VDC.
26	29	L2	X4	Output	Bit 4 of L-Bus (tri-state).
25	28	K3	I18	CMOS Input	Channel input data.
24	27	M1	I19	CMOS Input	Channel input data.
23	26	L1	I20	CMOS Input	Channel input data.

PIN DEFINITIONS

100 Pin QFP Pad #	120 Pin PGA Pin #		Name	I/O Type	Description
22	25	K2	I21	CMOS Input	Channel input data.
21	24	J3	I22	CMOS Input	Channel input data.
20	23	K1	I23	CMOS Input	Channel input data.
19	22	J2	Z18	Output	Channel output (tri-state).
18	21	J1	Z19	Output	Channel output (tri-state).
17	20	H3	Z20	Output	Channel output (tri-state).
16	19	H2	Z21	Output	Channel output (tri-state).
15	18	H1	Z22	Output	Channel output (tri-state).
D.B.	17	G1	V_{SS}	Power	Pad ring ground.
D.B.	16	G3	V_{SS}	Power	Pad ring ground.
N.C.	15	G2	V_{DD}	Power	Pad ring +5.0 VDC.
14	14	F1	Z23	Output	Channel output (tri-state).
13	13	F2	Z24	Output	Channel output (tri-state).
12	12	F3	Z25	Output	Channel output (tri-state).
11	11	E1	Z26	Output	Channel output (tri-state).
10	10	E2	Z27	Output	Channel output (tri-state).
9	9	D1	I24	CMOS Input	Channel input data.
8	8	E3	I25	CMOS Input	Channel input data.
7	7	D2	I26	CMOS Input	Channel input data.
6	6	C1	I27	CMOS Input	Channel input data.
5	5	C2	I28	CMOS Input	Channel input data.
4	4	D3	I29	CMOS Input	Channel input data.
3	3	B1	I30	CMOS Input	Channel input data.
2	2	B2	I31	CMOS Input	Channel input data.
1	1	C3	V_{DD}	Power	Pad ring +5.0 VDC

FUNCTIONAL DESCRIPTION

Overview

As a 32 x 32 cross-point switch, this IC's primary mission is to allow a user to independently connect any of the 32 inputs to one of its 32 outputs. The circuit must also support applications where multiple switches are placed in parallel (outputs wire-ored together) to create even larger systems.

Structure

To provide the flexible switching behavior required (no inputs blocking), 32 muxes are used (one for each output). Each of these muxes is a 32:1 type as there are 32 input channels to choose from. A six bit latch is also provided for every mux to allow the user to individually load the desired input address for each output channel. Five of the six latch bits (D0–D4) are for describing the mux input while bit D5 is reserved for enabling the channel's output driver (0=tri-state, 1=driving). As the host needs to update a mux's latch without interfering with the other outputs, a decoder using five address lines as inputs is included. To enhance in-circuit testability, the outputs of all 32 six bit latches are wire-ored to form the L-bus which can be read by the host on the X-bus tri-statable outputs. Another diagnostic output bus (the Q-bus) can relay the status of both the L-bus and the A-bus (WN=0: A-bus, WN=1: L-bus), but cannot be tri-stated.

A summary of the circuit's behavior is presented in the truth table format (Table 2). A detailed discussion of the various operational modes follows.

		Read Mode	Write Mode	Idle Mode	Reset Mode	Unselect Mode
IN	CS	H	H	H	H	L
	RSTN	H	H	H	L	H
	E	H	H	L	X	X
	WN	H	L	X	X	X
Out	Q-Bus	D0–D5	A0–A5 Q5=0	L	L	L
	X-Bus	D0–D5**	Hi-Z	Hi-Z	Hi-Z	Hi-Z
	Z-Bus	Respective selected input**				Hi-Z

*Don't Care
**If D5=1, else Hi-Z.

Table 2. Truth Table

Idle Mode

As indicated in Table 2, the idle mode is encountered when both CS and RSTN are high but E is low. In this case, each mux uses the previously stored contents of its latch to choose an input to pass to its output. The Z-bus drivers are enabled (subject to D5 as discussed previously) while the Q-bus and the X-bus are inactive.

Reset Mode

In the case where RSTN=0, the reset mode begins. Here, all the mux latches are enabled at once (NOT CLEARED!). Depending on CS and the contents of the D-bus, the Z-bus outputs will either all reflect the state of the input specified (CS and D5=1) or all be floating (CS or D5=0). To clear the mux latches, the host must assure the presence of low inputs on the D-bus before and after the RSTN line is brought high. For in-circuit testing, the host can use this mode to exercise all 32 muxes simultaneously. Both the Q-bus and X-bus outputs are inactive while RSTN is low. A Schmitt trigger input is provided for RSTN to support the slow rise times seen when external capacitance is used for holding RSTN low during power-up.

Unselected Mode

As Table 2 suggests, the chip immediately enters the unselected mode when CS is taken low (regardless of the other control inputs). In this state, the Q-bus outputs go low while the Z-bus and X-bus float. The contents of the mux latches are not affected.

Write Mode

To modify the contents of a single mux's latch, the WN line must be low while CS, RSTN, and E are all high per Table 2. The latch selected by the A-bus is immediately loaded with the contents of the D-bus and this information is latched by the rising edge of the WN line. The E pulse must occur while WN is low for the Write operation to take place on the rising edge of WN. While WN is low, the Q-bus outputs the contents of the A-bus (A0–A4 on lines Q0–Q4, Q5 always low). It should be noted that only the selected mux's output can change during a write cycle. This insures that the other output channels can continue to pass their data independently of the operation.

Read Mode

Per Table 2, when all four of the control lines (CS, RSTN, E, WN) are high, the chip is in the read mode. During this

TIMING DIAGRAMS

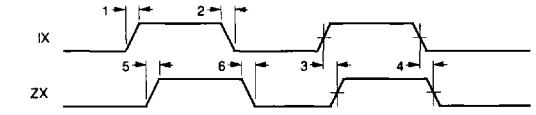


Figure 3a. Idle

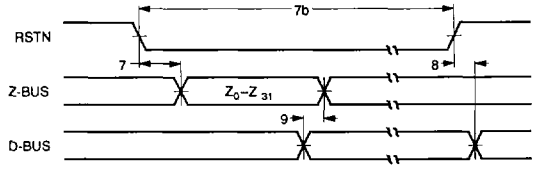


Figure 3b. Reset

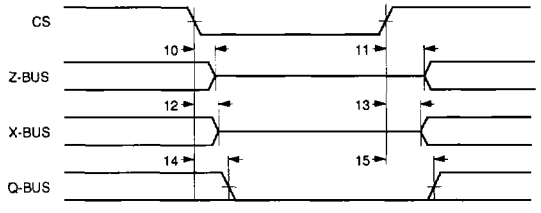


Figure 3c. Unselected

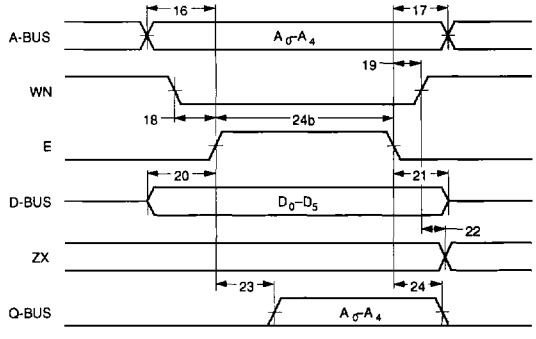


Figure 3d. Write

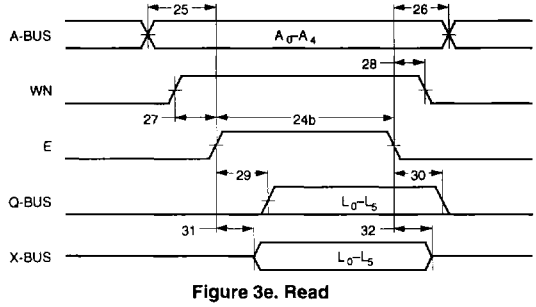


Figure 3e. Read

time, the X-bus reflects the contents of the L-bus if L5 is high, otherwise the X-bus floats. Meanwhile, the Q-bus also displays the L-bus status but without regard to L5.

Expandability for the SC11320

In order to expand the SC11320 to larger Cross-Point-Switches, it must be configured such that any input can be multiplexed to any output. Figure 4 is an example of a 64 X 64 Cross-Point-Switch. The top two SC11320's (1 & 2) correspond to the first 32 outputs and the bottom two SC11320's (3 & 4) to the last 32 outputs. The SC11320's on the left (1 & 3) correspond to the first 32 inputs, and the two SC11320's on the right (2 & 4) to the last 32 inputs. All like outputs are then joined to form the Z and Q output busses. The four SC11320's are connected in such a way that only one or none of the outputs will drive any of the 64 Z channels at a time. This will prevent contention on the Z bus.

The D5 input is still the disable input for the Z outputs. The D6 input specifies which set of I inputs to multiplex through to the Z outputs. When D6 is LOW, the first 32 I inputs are selected; and when D6 is HIGH, the second 32 I inputs are selected.

The A5 input selects between the first 32 control latches and the second 32 control latches when the device is in the READ or WRITE mode. This is done by gating A5 with the E and WN signals of each SC11320. To keep the deselected SC11320's from accidentally WRITING data into the control latches, the A5 input is gated with both the E and WN signals. This will prevent any internal race conditions between the E and WN signals.

In this example, the CSn and RSTNn signals are all separate inputs. This is not necessary for the expansion of the SC11320 and is system dependent. The In, Dn and An inputs, and the Zn and Qn outputs must stay in this format in order to maintain correct functionality of a Cross-Point-Switch.

The gating needed to perform this expansion is minimal (8 gates), and can be done on or off chip. Further expansion can be accomplished using the same technique.

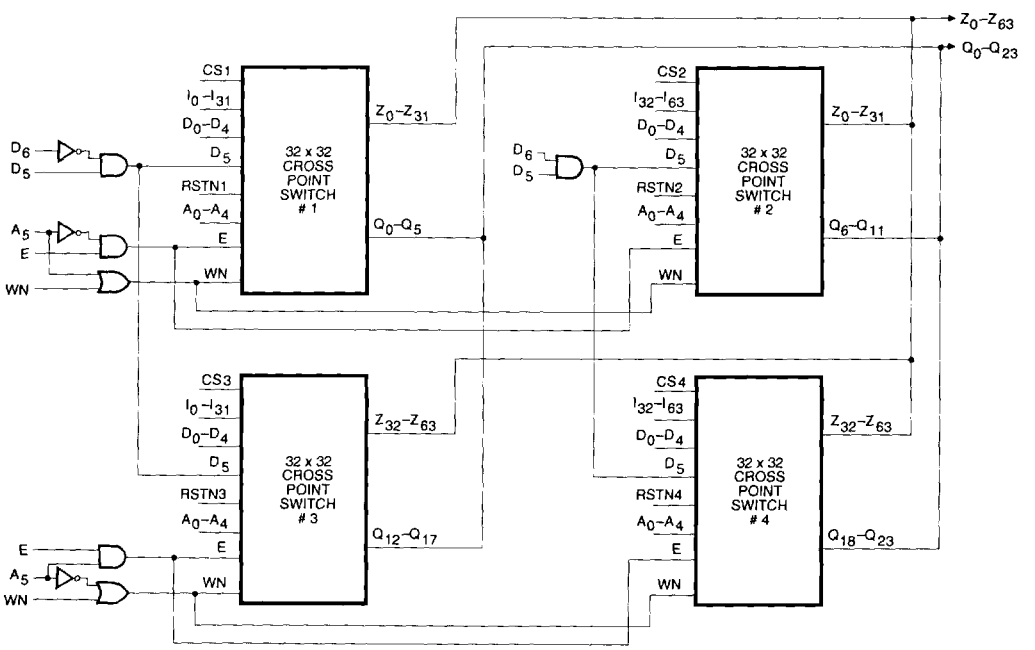


Figure 4. Expansion to 64 x 64 Crosspoint Switch

DC OPERATING CONDITIONS

Description	Min	Typ	Max	Units	Notes
Operating Ambient Air Temperature Range	0	25	70	°C	Junction Range 0 to 85
Power Supplies					
V_{DD} Supply Voltage	4.5	5.0	5.5	V	
V_{SS} Supply Voltage	0	0	0	V	
I_{DD} Supply Current		170		mA	20 MHz
Leakage Current (all inputs & tri-state outputs)	-10		+10	µA	
Input Voltages					
Logic "0" (V_{IL}) all except RSTN			1.5	V	
Logic "1" (V_{IH}) all except RSTN	3.5			V	
Logic "0" (V_{IL}) RSTN only	1.3	1.8	2.0	V	
Logic "1" (V_{IH}) RSTN only	3.0	3.5	3.8	V	
Schmitt Trigger Hysteresis	1.0	1.7	2.0	V	
Output Voltages					
Z0–Z31					
Logic "0" (V_{OL})	V_{SS}		0.8	V	I_{OL} = +8 mA
Logic "1" (V_{OH})	V_{DD}–0.8		V_{DD}	V	I_{OH} = –8 mA
X0–X5, Q0–Q5					
Logic "0" (V_{OL})	V_{SS}		0.8	V	I_{OL} = +4 mA
Logic "1" (V_{OH})	V_{DD}–0.8		V_{DD}	V	I_{OH} = –4 mA
Input Capacitance			10	pF	w/package
Output Capacitance			10	pF	w/package
Output Loading					
Q0–Q5			20	pF	
Z0–Z31			50	pF	
X0–Z5			170	pF	

AC CHARACTERISTICS

(Refer to Figures 1.1–1.5)
(@ V_{DD}=5.0 V ±10% V_{SS}=0 V, T_A=0 to 70°C. Outputs loaded and timing measured at CMOS levels.
All input rise and fall times < 10 ns, unless otherwise specified)

No	Description	Min	Typ	Max	Units	Notes
1	I-Bus Rise Time			5	ns	Figure 3.1 (symmetry: 50/50 in 45/55 out at 50 MHz)
2	I-Bus Fall Time			5	ns	
3	Propagation Time (Rising)		25	40	ns	
4	Propagation Time (Falling)		25	40	ns	
5	Z-Bus Rise Time	4		11	ns	(with 50 pF load on Z-bus)
6	Z-Bus Fall Time	4		11	ns	
	Z-Bus Skew Time		2	4	ns	
	I-Bus Frequency			50	MHz	
7	Reset Fall to Z-Bus Change			55	ns	
7b	Reset Pulse Width	100			ns	
8	D-Bus Hold From Reset Rise	20			ns	Figure 3.2
9	D-Bus to Z-Bus Delay			40	ns	
10	CS Fall to Z-Bus Float			25	ns	
11	CS Rise to Z-Bus Driven			25	ns	(If D5 = 1) Figure 3.3
12	CS Fall to X-Bus Float			30	ns	
13	CS Rise to X-Bus Driven			30	ns	(If D5 = 1)
14	CS Fall to Q-Bus Low			40	ns	
15	CS Rise to Q-Bus Enabled			50	ns	
16	A-Bus Setup Before E Rise	50			ns	
17	A-Bus Hold After E Fall	20			ns	Figure 3.4
18	WN Setup Before E Rise	50			ns	
19	WN Hold After E Fall	20			ns	
20	D-Bus Setup Before E Rise	50			ns	
21	D-Bus Hold After E Fall	20			ns	
22	WN Rise to Zx Change			85	ns	
23	E Rise to Q-Bus Active			40	ns	(A0–A4, 0)
24	E Fall to Q-Bus Low			35	ns	
24b	E Pulse Width	20			ns	
25	A-Bus Setup Before E Rise	50			ns	
26	A-Bus Hold After E Fall	50			ns	Figure 3.5
27	WN Setup Before E Rise	50			ns	
28	WN Hold After E Fall	20			ns	
29	E Rise to Q-Bus Active			55	ns	
30	E Fall to Q-Bus Low			35	ns	(L0–L5)
31	E Rise to X-Bus Active			85	ns	(L0–L5)
32	E Fall to X-Bus Float			30	ns	

MECHANICAL SPECIFICATION

Package
121 pin grid array (plastic, one locating pin)