❑ MN101E16 Series

Type	MN101E16K	MN101E16M	MN101E16Y	MN101EF16K	MN101EF16Z
Internal ROM type	Mask ROM			FLASH	
ROM (byte)	256K	384K		256K	512K
RAM (byte)	12K	20K		16K	30K
Package (Lead-free)	LQFP100-P-1414, QFP100-P-1818B	QFP100-P-1818B	QFP100-P-1818B (Under development)	LQFP100-P-1414, QFP100-P-1818B	QFP100-P-1818B
Minimum Instruction Execution Time	0.0588 µs (at 2.7 V to 3.6 V, 17 MHz, at internal 2, 4, 8 times oscillation)) 0.1 µs (at 2.7 V to 3.6 V, 20 MHz) 30.6 µs (at 2.7 V to 3.6 V, 32.768 kHz)				

■ Interrupts

RESET. Watchdog. External 0 to 5. Timer 0 to 3. Timer 6. Timer 7 (2 systems). Timer A to E.Time base. Serial 0 (2 systems). Serial 1 (2 systems). Serial 2. Serial 3 (2 systems). Serial 4 (2 systems). Automatic transfer finish (2 systems). A/D conversion finish. Key interrupt

■ Timer Counter

8-bit timer × 10

Timer 0 .....Square-wave/8-bit PWM output. Event count. Pulse width measurement. Real time output control

Timer 1 .....Square-wave output. Event count. Synchronous output event. 16-bit timer with cascade connection

Timer 2 .....Square-wave/8-bit PWM output. Event count. Synchronous output event. Pulse width measurement. Real time output control. Serial baud rate timer

Timer 3 .....Square-wave output. Event count. Serial baud rate timer

Timer 6 .....8-bit freerun timer. Time base timer

Timer A, B, C, D, E

Timer 0, 1 can be cascade-connected

Timer 0, 1, 2 can be cascade-connected

Timer 2, 3 can be cascade-connected

Timer 0, 1, 2, 3 can be cascade-connected

16-bit timer × 1

Timer 7 .....Square-wave/16-bit PWM output (cycle/duty continuous variable). Event count. Synchronous output event. Pulse width measurement. Input capture

Time base timer: One-minute count setting

Watchdog timer × 1

■ Serial interface

Synchronous type/UART (full-duplex) × 3: Serial 0, 1, 4

Synchronous type/Single-master I^2C × 1: Serial 2

Synchronous type/I^2C × 1: Serial 3

■ DMA controller

Number of channels: 2 channels

Maximum transfer cycles: 255

Starting factor: External request. Various types of interrupt. Software

Transfer mode: 1-byte transfer. Word transfer. Burst transfer

■ I/O Pins

I/O 22 : (5 V I/F port) Common use. Specified pull-up resistor available. Input/output selectable (bit unit)

62 : (3 V I/F port) Common use. Specified pull-up resistor available. Input/output selectable (bit unit)

1 : (3 V I/F port) Common use

■ A/D converter

10-bit × 8 channels (with S/H)

■ Special Ports

Buzzer output. High-current drive port

■ ROM Correction

Correcting address designation: Up to 7 addresses possible

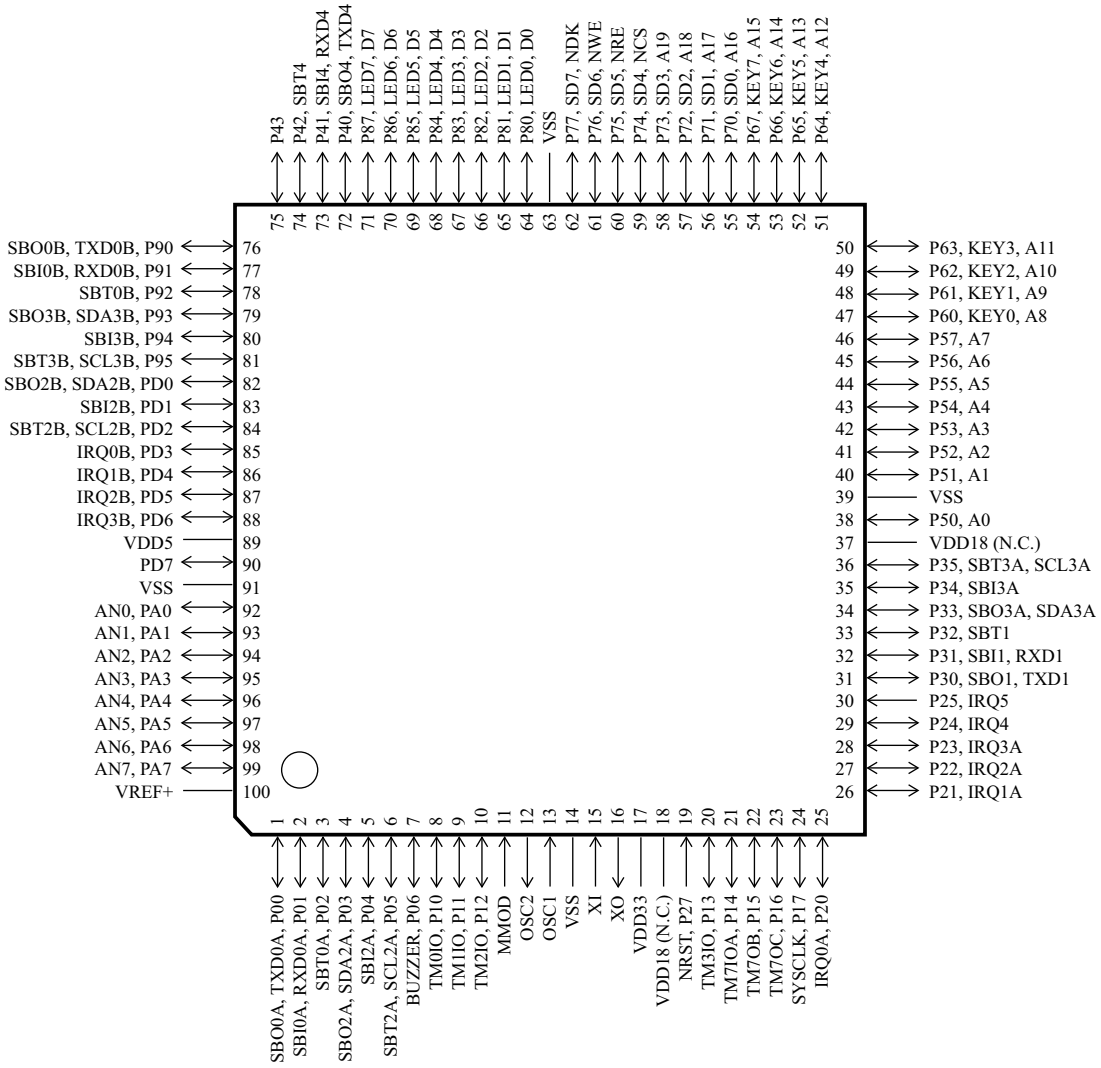
■ Development tools

In-circuit Emulator

Maintenance/Discontinued
Maintenance/Discontinued includes following four Product life cycle stages
planed maintenance type
maintenance type
planed discontinued type
discontinued type
Please visit following URL about latest information.
http://panasonic.net/sc/en

■ Pin Assignment

LQFP100-P-1414, QFP100-P-1818B



Note) ( ): MN101E16M

Pin 1 to Pin 75: VDD33 = 2.7 V to 3.6 V

Pin 76 to Pin 100: VDD5 = VDD33 to 5.5 V

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