HD-LINX™ GS1504
HDTV Adaptive Equalizer

DATA SHEET

FEATURES

- **SMPTE 292M compliant**
- **Automatic, adjustment free cable equalization for 1.485Gb/s HDTV signals**
- **Differential serial outputs capable of driving 50Ω loads**
- **Typically equalizes 100m of Belden 8281 or 150m of Belden 1694 high quality co-axial cable**
- **Cable Length Indication**
- **Output Mute**
- **Maximum Cable Length Adjust**
- **Low power**
- **Minimal external components**
- **Single +5V or -5V power supply operation**

APPLICATIONS

1.485Gb/s HDTV Serial Digital Receiver Interfaces for Routers, Distribution Amplifiers, Switchers, and other receiving equipment.

DESCRIPTION

The GS1504 is a high performance cable equalizer designed to equalize HDTV component signal conforming to SMPTE 292M. The adaptive cable equalizer is capable of equalizing up to 100m of Belden 8281 co-axial cable.

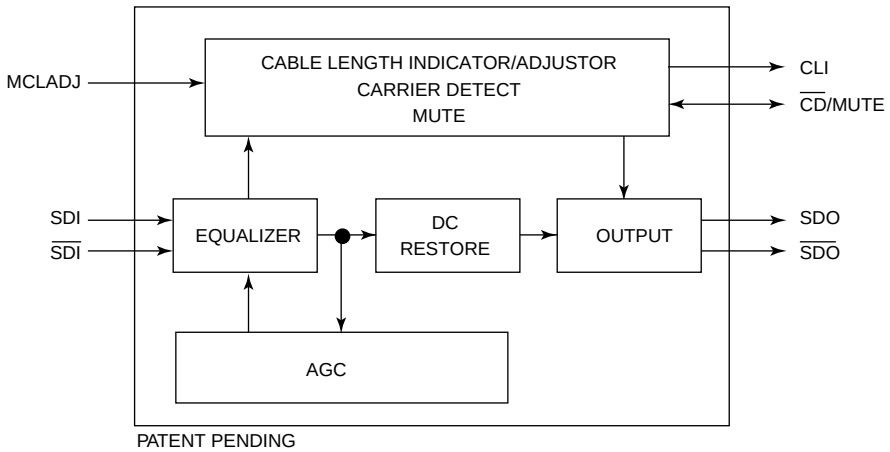
The GS1504 features DC restoration for immunity to the DC content in pathological test patterns. The device also incorporates a Cable Length Indicator signal that provides an indication of the amount of cable being equalized.

A voltage programmable mute threshold (MCLADJ) is included to allow muting of the GS1504 output when a selected cable length is reached. This feature allows the GS1504 to distinguish between low amplitude HD SDI signals and noise at the input of the device. The $\overline{CD}$/Mute pin provides an indication of the GS1504 mute status in addition to functioning as a mute control input. The output of the GS1504 may be forced to an active or a mute condition by applying a voltage to the $\overline{CD}$/Mute pin.

The GS1504 is a low power device that operates from a single 5V power supply. The GS1504 is packaged in a 16 pin narrow SOIC and does not need external pull-up resistors.

ORDERING INFORMATION

PART NUMBER	PACKAGE	TEMPERATURE
GS1504-CKD	16 pin narrow SOIC	0°C to 70°C
GS1504-CTD	16 pin Tape and Reel	0°C to 70°C



BLOCK DIAGRAM

GENNUM CORPORATION P.O. Box 489, Stn. A, Burlington, Ontario, Canada L7R 3Y3
Tel. +1 (905) 632-2996 Fax. +1 (905) 632-5946 E-mail: info@gennum.com
www.gennum.com

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C unless otherwise indicated

PARAMETER	VALUE
Supply Voltage	5.5V
Input Voltage Range (any input)	-0.3 to (V_{CC} +0.3)V
Operating Temperature Range	0°C to 70°C
Storage Temperature	-65°C to 150°C
Power Dissipation	300mW
Lead Temperature (soldering, 10 sec)	260°C
Input ESD Voltage	2000V

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5V, V_{EE} = 0V, T_A = 0°C to 70°C, Data Rate = 1.485Gb/s

PARAMETER	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNITS	TEST LEVELS
Positive Supply Voltage		V_{CC}	4.75	5.00	5.25	V	1
Power Consumption			-	250	-	mW	1
Supply Current			-	50	65.0	mA	1
Output CM Voltage			3.75	4	4.25	V	1
Input DC Voltage	Internal Bias. See Figure 2		-	2.7	-	V	1
CLI DC Voltage (0m)	CLI Output for 0m Cable		-	3.3	-	V	4
CLI DC Voltage (no signal input)			0.9	1.3	1.7	V	1
Cable Length Indicator Range	0 - Max m	CLI	-	2	-	V	2
MCLADJ DC Voltage	MCLADJ Input Voltage Required to Mute Output		2.80	3.1	3.4	V	1
MCLADJ Range	(max cable to 0m)			1		V	2
Mute DC Voltage	Output Voltage of $\overline{CD}$/Mute when Output is Active		1.5	1.8	2.1	V	1
Voltage Required to Force Outputs to Mute	Min to Mute; $V_{\overline{CD}/Mute}$			4.2		V	2
Voltage Required to Force Outputs Active	Max to Activate; $V_{\overline{CD}/Mute}$			3.8		V	2

TEST LEVELS: 1. 100% tested at 25°C. 2. Guaranteed by design. 3. Correlated Value. 4. Using EB1504

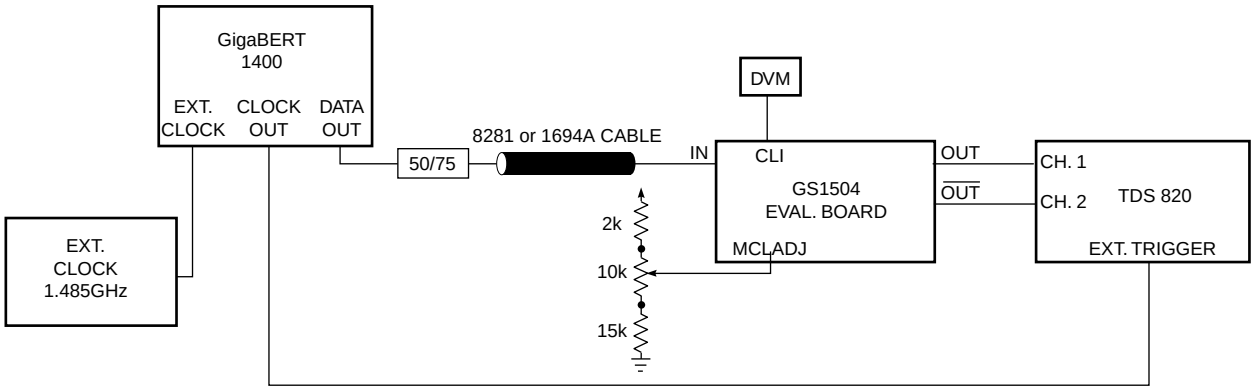


Fig. 1 Test Setup

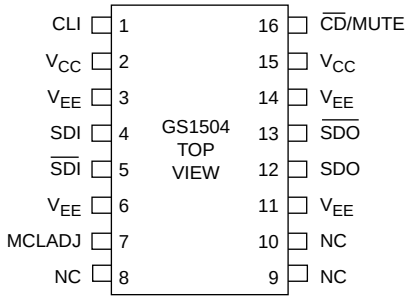
AC ELECTRICAL CHARACTERISTICS

V_{CC} = 5V, V_{EE} = 0V, T_A = 0°C to 70°C, Data Rate = 1.485Gb/s

PARAMETER	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNITS	TEST LEVEL
Jitter	100m (8281), PRN and pathological		-	80	135	ps p-p	1
Equalization	Belden 8281		-	100	-	m	1
	Belden 1694		-	150	-	m	3
Output Rise/Fall Time	20% - 80%		-	130	270	ps	1
Input Resistance	Single Ended		-	2.8	.	kΩ	2
Input Capacitance	Single Ended		-	1	-	pF	2
Output Resistance	Single Ended		-	50	-	Ω	2
Output Signal Swing SDO, $\overline{SDO}$	Into 50Ω Loads; See Figure 21.		160	200	240	mVp-p	1

TEST LEVELS: 1. 100% tested at 25°C. 2. Guaranteed by design. 3. Correlated Value. 4. Using EB1504

PIN CONNECTIONS



PIN DESCRIPTIONS

NUMBER	SYMBOL	TYPE	DESCRIPTION
1	CLI	O	Cable Length Indication. Provides a voltage output representing the amount of cable being equalized. See figures 19 and 20. The CLI voltage is an approximation of the cable length being equalized. It is intended as a guide for troubleshooting the initial design and not as an accurate indication of cable length.
2, 15	V_{CC}	I	Most positive supply voltage.
3, 6, 11, 14	V_{EE}	I	Most negative supply voltage.
4, 5	SDI, $\overline{SDI}$	I	Differential Input Pins. AC coupled termination is recommended.
7	MCLADJ	I	Adjusts the maximum amount of cable to be equalized (from 0m to the maximum cable length). The output is muted (latched to the last state) when the maximum cable length is reached. To achieve maximum cable length, this pin should be left open. See figures 10 - 12.
8, 9, 10	NC	-	No Connect. Do not connect these pins to supply or ground.
12, 13	SDO, $\overline{SDO}$	O	Differential Serial Data Output Pins, with 50Ω output resistance.
16	$\overline{CD}$/Mute	I/O	Carrier Detect/Mute Indicator/Control. When the $\overline{CD}$/Mute output is low, the carrier is present and the data output is active. When the $\overline{CD}$/Mute output is high, the carrier is not present and the data output is muted (latched to the last state). This indicates that the maximum cable length as set by MCLADJ has been reached. The above default $\overline{CD}$/Mute function can be overwritten as follows: if the $\overline{CD}$/Mute pin is tied to ground the data output will not mute and the MCLADJ setting is overwritten. If the mute pin is tied high, the data output will always mute and the MCLADJ setting is overwritten.

INPUT / OUTPUT CIRCUITS

All resistors in ohms, all capacitors in farads, unless otherwise shown.

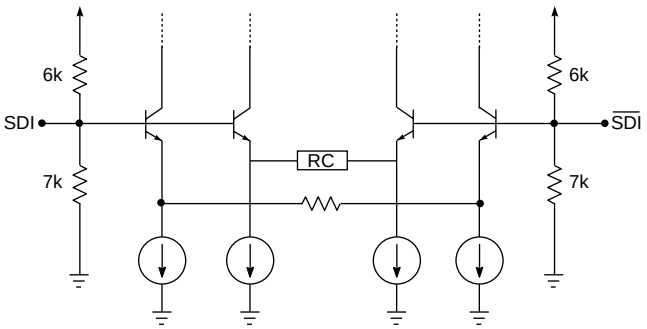


Fig. 2 Input Equivalent Circuit

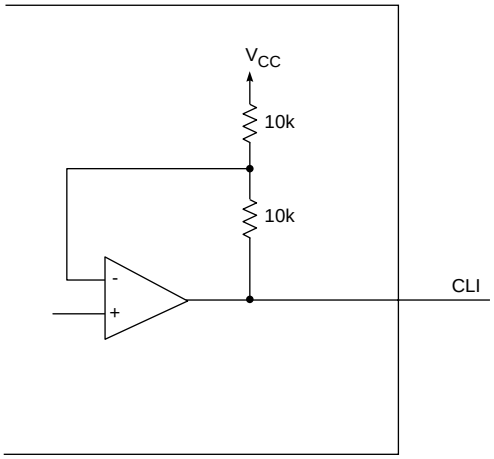


Fig. 5 CLI Output Circuit

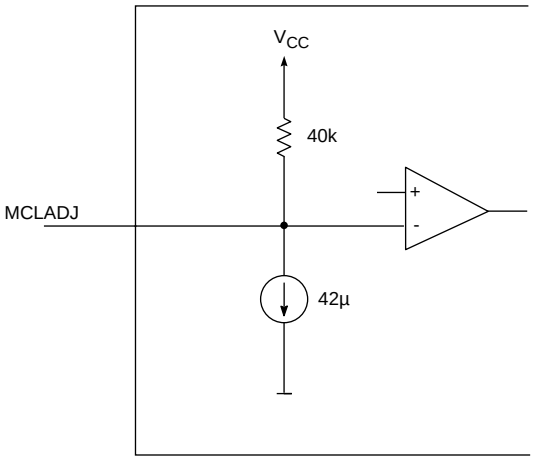


Fig. 3 MCLADJ Equivalent Circuit

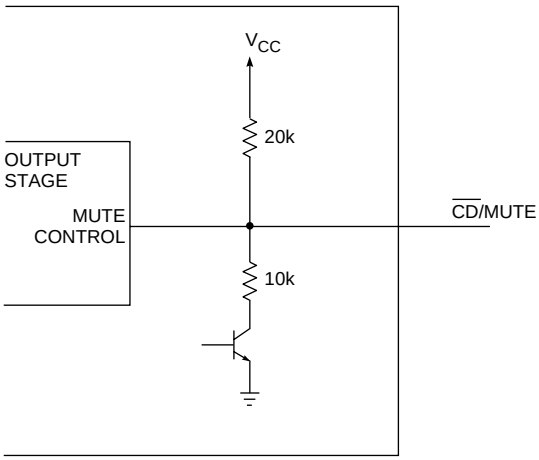


Fig. 6 $\overline{CD}$/Mute Circuit

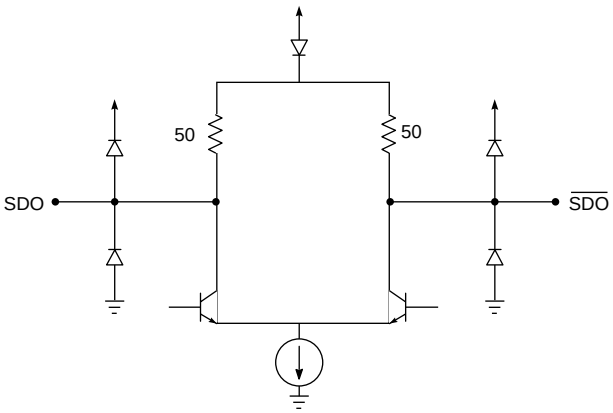


Fig. 4 Output Circuit

TYPICAL PERFORMANCE CURVES (unless otherwise shown, V_{CC} = 5V, T_A = 25°C)

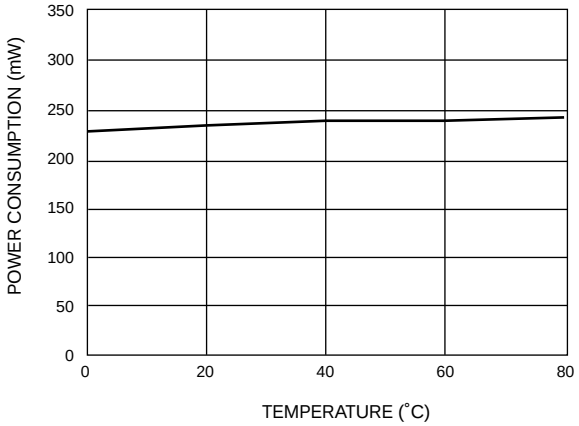


Fig. 7 Power Consumption

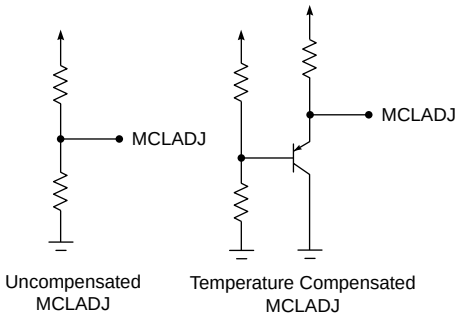


Fig. 10 Temperature Compensation of MCLADJ

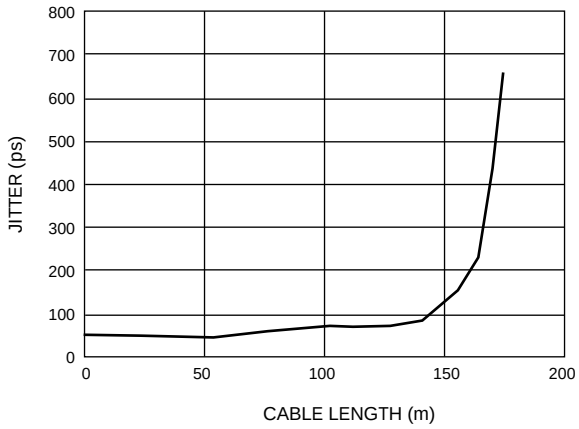


Fig. 8 Typical Peak to Peak Jitter, PRN 2^{23}-1, Belden 1694A

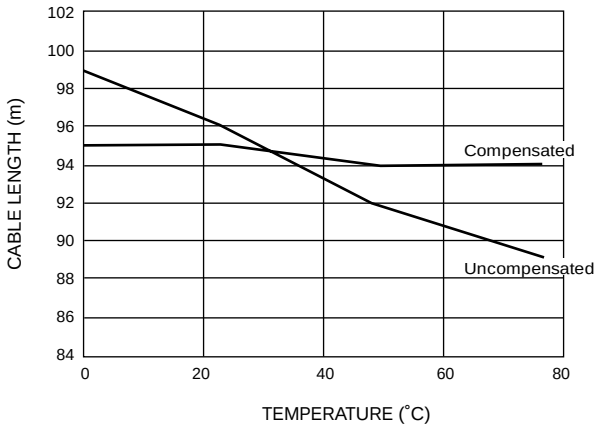


Fig. 11 Typical 1694A Cable Length vs. Temperature

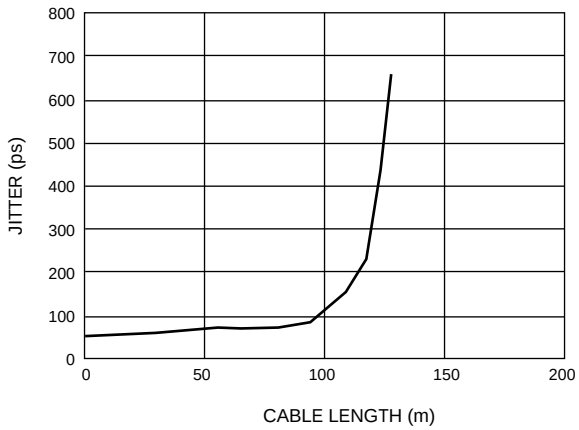


Fig. 9 Typical Peak to Peak Jitter, PRN 2^{23}-1, Belden 8281

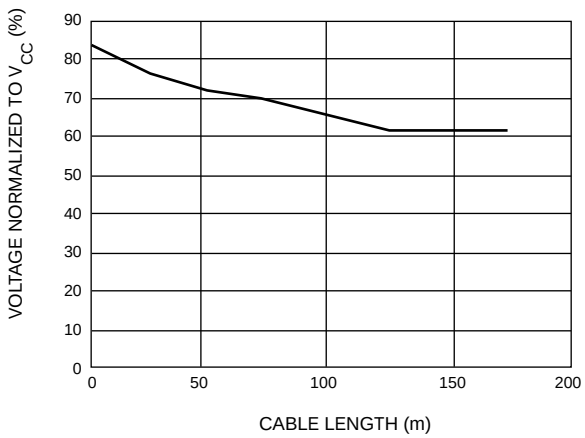


Fig. 12 MCLADJ Input Voltage vs 1694A Cable Length

TYPICAL PERFORMANCE CURVES (unless otherwise shown V_{CC} = 5V, T_A = 25°C)

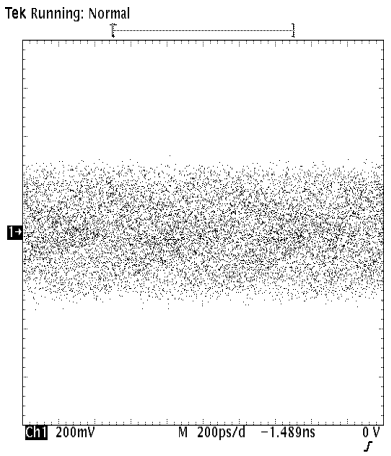


Fig. 13 Input 100m (Belden 1694A)

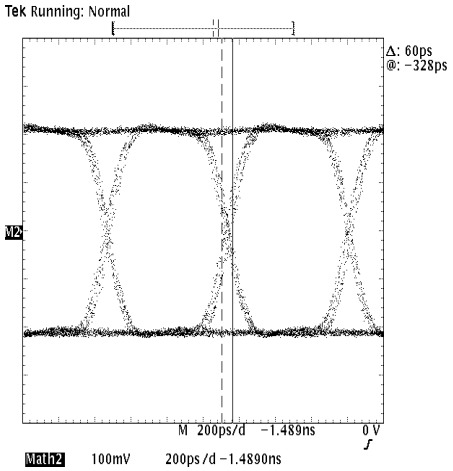


Fig. 16 Output 150m (Belden 1694A)

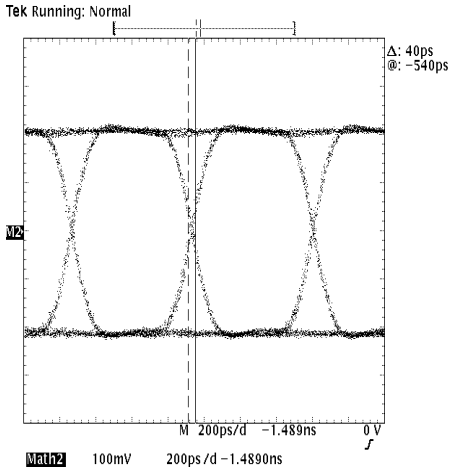


Fig. 14 Output 100m (Belden 1694A)

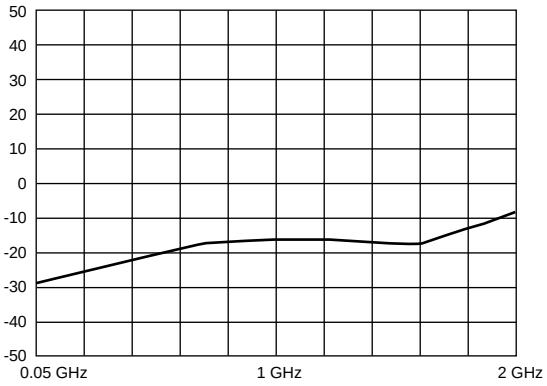


Fig. 17 Input Return Loss

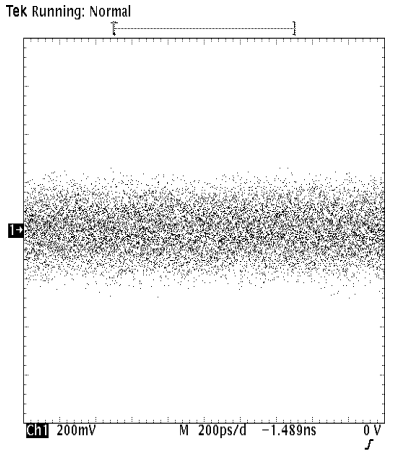


Fig. 15 Input 150m (Belden 1694A)

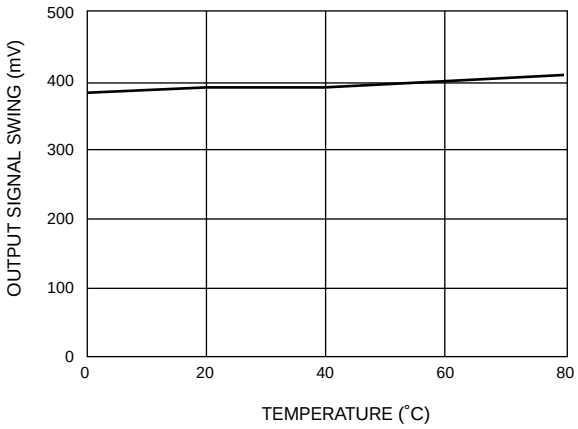


Fig. 18 Output Signal Swing, p-p, Differential

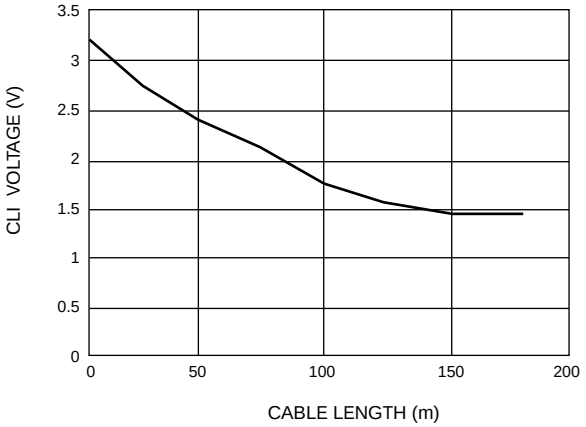


Fig. 19 CLI Voltage vs. Belden 1694A Cable Length

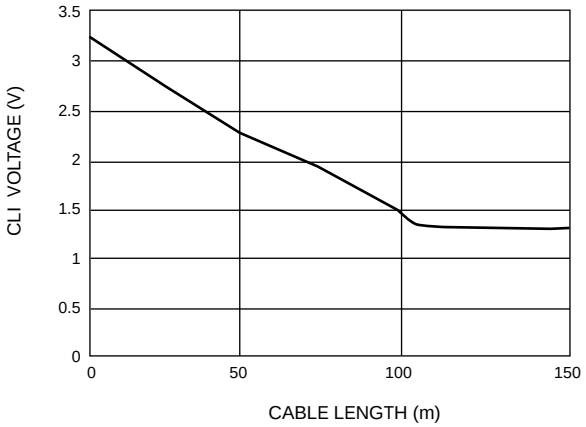


Fig. 20 CLI Voltage vs. Belden 8281 Cable Length

DETAILED DESCRIPTION

The GS1504 is a high speed bipolar IC designed to equalize HD serial digital data at a rate of 1.485Gb/s. The device can typically equalize greater than 100 meters of Belden 8281 cable or 150 meters of Belden 1694 cable. Powered from a single +5V or -5V power supply, the device consumes approximately 250mW of power

The HD serial data signal may be connected to the input pins (SDI/$\overline{\text{SDI}}$) in either a differential or single ended configuration. AC coupling of the inputs is recommended, as the SDI and $\overline{\text{SDI}}$ inputs are internally biased at approximately 2.7 volts. The input signal passes through a variable gain equalizing stage whose frequency response closely matches the inverse cable loss characteristic. In addition, the variation of the frequency response with control voltage imitates the variation of the inverse cable loss characteristic with cable length.

The edge energy of the equalized signal is monitored by a detector circuit which produces an error signal corresponding to the difference between the desired edge energy and the actual edge energy. This error signal is integrated by an internal AGC filter capacitor providing a steady control voltage for the gain stage. As the frequency response of the gain stage is automatically varied by the application of negative feedback, the edge energy of the equalized signal is kept at a constant level which is representative of the original edge energy at the transmitter. The equalized signal is also DC restored, effectively restoring the logic threshold of the equalized signal to its correct level independent of shifts due to AC coupling. The digital output signals have a nominal voltage of 400mVpp differential, or 200mVpp single ended when terminated with 50Ω as shown in Figure 21.

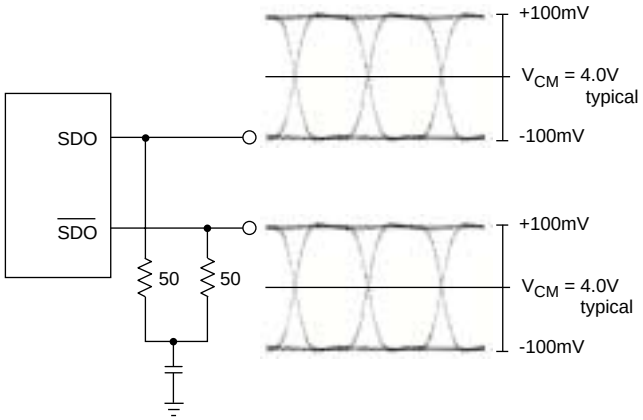


Fig. 21 Typical Output Voltage Levels

CABLE LENGTH INDICATION/CARRIER DETECT/MUTE

The GS1504 incorporates a versatile analog cable length indicator (CLI) output and a programmable threshold output mute (MCLADJ). In addition, a multi-function $\overline{\text{CD}}$/MUTE pin allows control of the GS1504 MUTE functionality.

The voltage output of CLI pin is an approximation of the amount of cable present at the GS1504 input. The CLI voltage versus cable length (signal strength) is shown in Figures 19 and 20. With 0m of cable (800mV input signal levels), the CLI output voltage is approximately 3.3V. As the cable length increases, the CLI voltage decreases providing an approximate correlation between the CLI voltage and cable length.

In applications where there are multiple input channels using the GS1504, it is advantageous to have a programmable mute output.

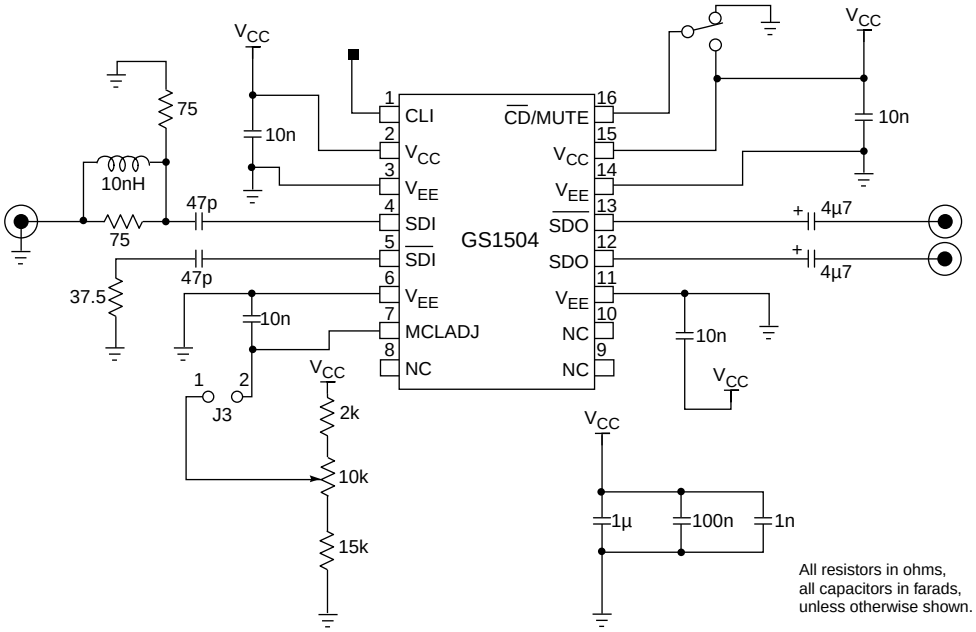
The output of the GS1504 can be muted when the input signal decreases below a preselected input level. The voltage applied to the MCLADJ pin vs input cable length is shown in Figure 12. The MCLADJ pin may be left unconnected for applications where output muting is not required. This feature has been designed for use in applications such as routers where signal crosstalk and circuit noise cause the equalizer to output erroneous data when no input signal is present. The use of a Carrier Detect function with a fixed internal reference does not solve this problem since the signal to noise ratio on the circuit board

could be significantly less than the default signal detection level set by the on chip reference.

The $\overline{CD}$/Mute pin is a multi-function bidirectional pin that provides the following functions:

- Applying a HIGH INPUT to the $\overline{CD}$/Mute pin forces the GS1504 outputs to a muted condition. See the DC electrical characteristics table for voltage level. In this condition the outputs will be latched to the last logic level present at the output.
- Applying a LOW INPUT to the $\overline{CD}$/Mute pin will force the GS1504 outputs to remain active regardless of the length of input cable and the voltage applied to the MCLADJ pin. See the DC electrical characteristics table for voltage level.
- When used as an OUTPUT, the $\overline{CD}$/Mute pin will provide an indication of the output mute status. The $\overline{CD}$/Mute pin will be logic HIGH when the output is muted, and logic LOW when the outputs are not muted.

TYPICAL APPLICATION CIRCUIT



APPLICATION INFORMATION

PCB LAYOUT

Special attention must be paid to component layout when designing serial digital interfaces for HDTV. Figures 23 through 27 show the artwork for a four layer printed circuit evaluation board for the GS1504. The schematic is shown in Figure 22. An FR-4 dielectric can be used, however, controlled impedance transmission lines are required for PCB traces longer than approximately 1cm. Note the following PCB artwork features used to optimize performance:

- PCB trace width for HD rate signals is closely matched to SMT component width to minimize reflections due to change in trace impedance.
- The PCB ground plane is removed under the GS1504 input components to minimize parasitic capacitance.
- The PCB ground plane is removed under the GS1504 output components to minimize parasitic capacitance.
- High speed traces are curved to minimize impedance changes.

A picture of the GS1504 PCB assembly is shown in Figure 28.

GS1504 EVALUATION BOARD

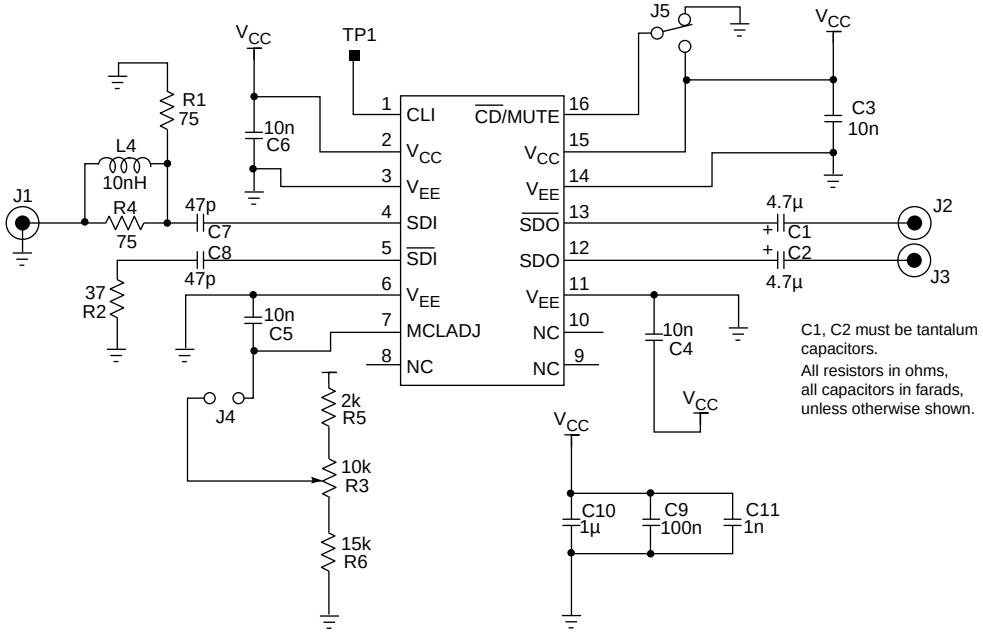


Fig. 22 GS1504 Application Schematic

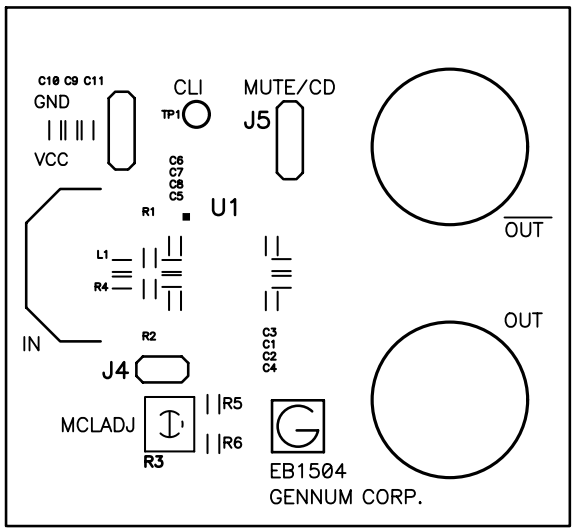


Fig. 23 Silk Screen of EB1504 PCB Layout

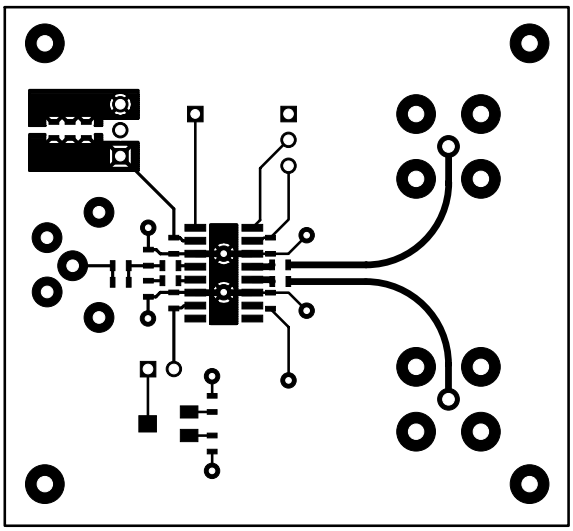


Fig. 24 Top Layer of EB1504 PCB Layout

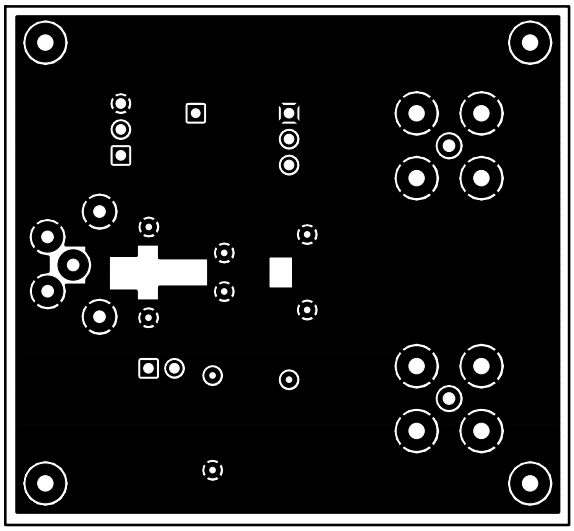


Fig. 25 Ground Layer of EB1504 PCB Layout

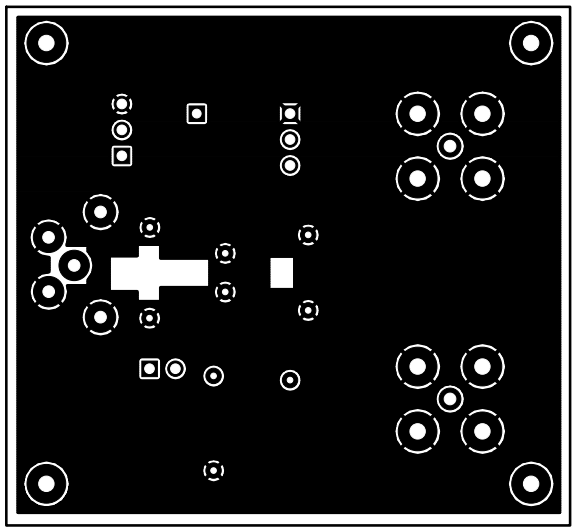


Fig. 26 Bottom Layer of EB1504 PCB Layout

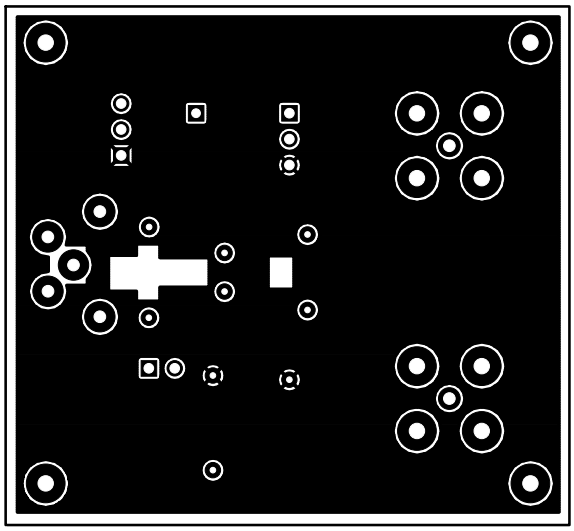


Fig. 27 Power Layer of EB1504 PCB Layout

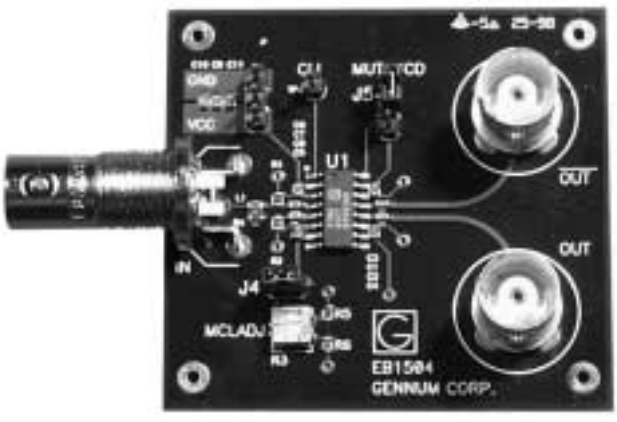


Fig. 28 Photograph of GS1504 Evaluation Board

GS1504 / GS1508 INTERFACING

Figures 30 through 34 show the artwork for a four layer printed circuit evaluation board for the GS1504. The schematic is shown in Fig 29. An FR-4 dielectric can be used, however, controlled impedance transmission lines are required for PCB traces longer than approximately 1cm. Note the following PCB artwork features used to optimize performance:

- PCB trace width for HD rate signals is closely matched to SMT component width to minimize reflections due to change in trace impedance.
- The PCB ground plane is removed under the GS1504/GS1508 input components to minimize parasitic capacitance.
- The PCB ground plane is removed under the GS1504/GS1508 output components to minimize parasitic capacitance.
- High speed traces are curved to minimize impedance changes.

A picture of the GS1504/08 PCB assembly is shown in Figure 34.

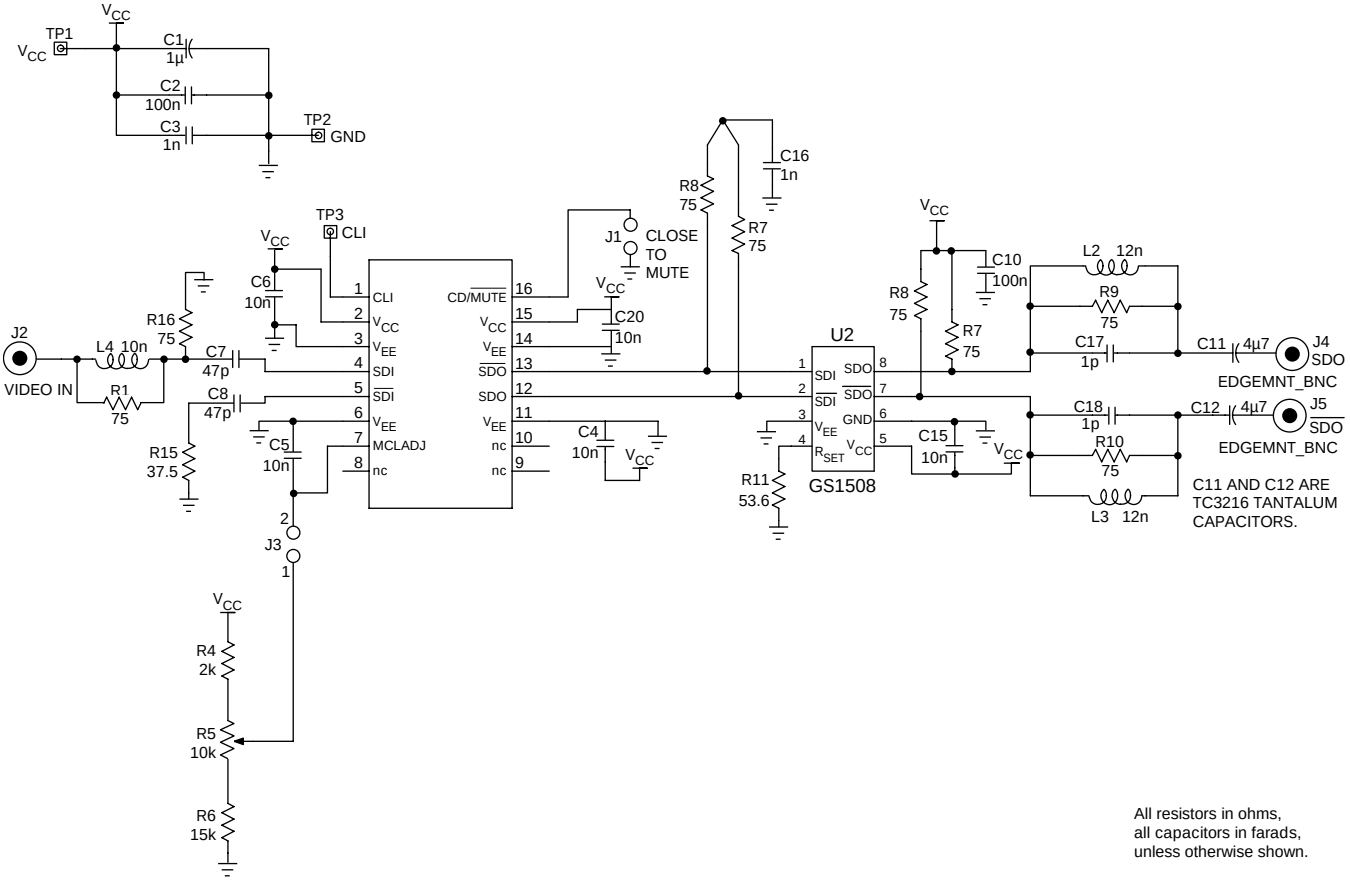


Fig. 29 GS1504/08 Evaluation Board Assembly

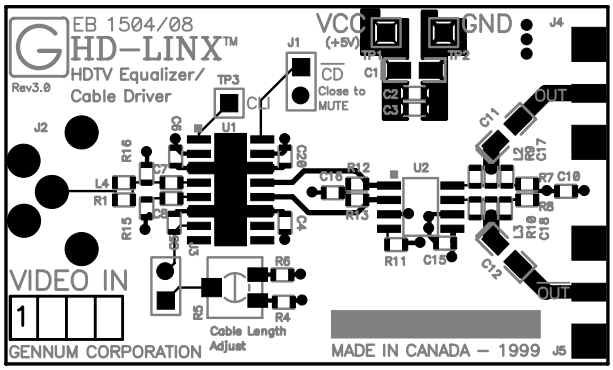


Fig. 30 Top Layer of EB1504/08 PCB Layout

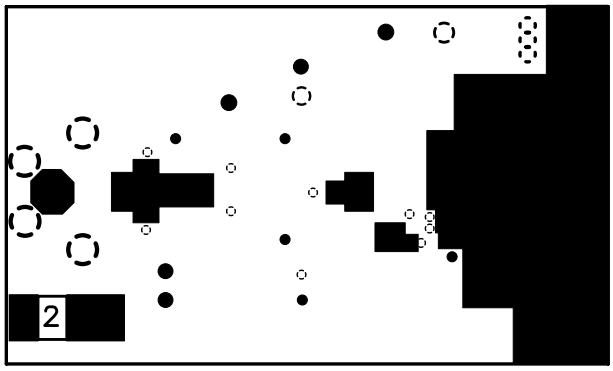


Fig. 32 Ground Layer of EB1504/08 PCB Layout

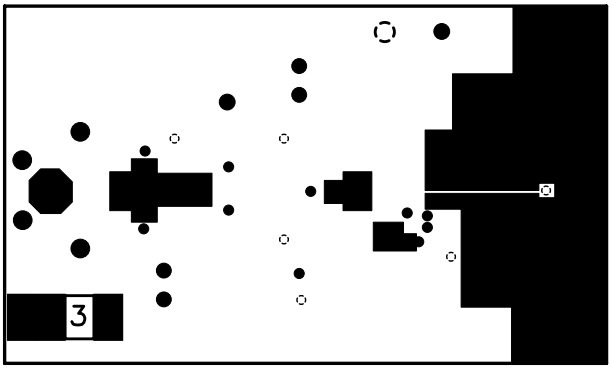


Fig. 31 Power Layer of EB1504/08 PCB Layout

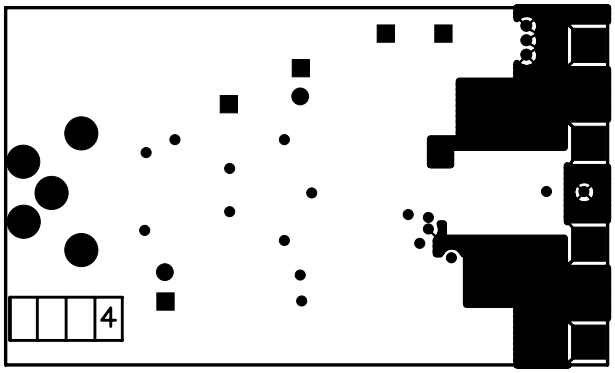


Fig. 33 Bottom Layer of EB1504/08 PCB Layout

Fig. 34 Photograph of GS1504/GS1508 Evaluation Board

CAUTION

ELECTROSTATIC
SENSITIVE DEVICES

DO NOT OPEN PACKAGES OR HANDLE
EXCEPT AT A STATIC-FREE WORKSTATION

DOCUMENT IDENTIFICATION

DATA SHEET

The product is in production. Gennum reserves the right to make changes at any time to improve reliability, function or design, in order to provide the best product possible.

REVISION NOTES:

Document type changed to data sheet.

For the latest product information, visit www.gennum.com

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