PCMCIA Flash Memory Card **1 *MEGABYTE through 10 MEGABYTE (AMD based)***

General Description

WEDC's FLC Series Flash memory cards offer medium/high density linear Flash solid state storage solutions for code and data storage, high performance disk emulation and execute in place (XIP) applications in mobile PC and dedicated (embedded) equipment.

FLC series cards conform to PCMCIA international standard.

The card's control logic provides the system interface and controls the internal Flash memories. Card can be read/written in byte-wide or word-wide mode which allows for flexible integration into various systems. Combined with file management software, such as Flash Translation Layer (FTL), FLC Flash cards provide removable high-performance disk emulation.

The FLC series cards contain separate 2kB EEPROM memory for Card Information Structure (CIS) which can be used for easy identification of card characteristics.

The WEDC FLC series is based on AMD Am29F040 Flash memories; the FLC04 is a direct equivalent of AMD's AmC0XXCFLKA, however it offers wider range of intermediate memory capacities.

Note: Standard options include attribute memory. Cards without attribute memory are available. Cards are also

Architecture Overview

vare write protect switch.

Features

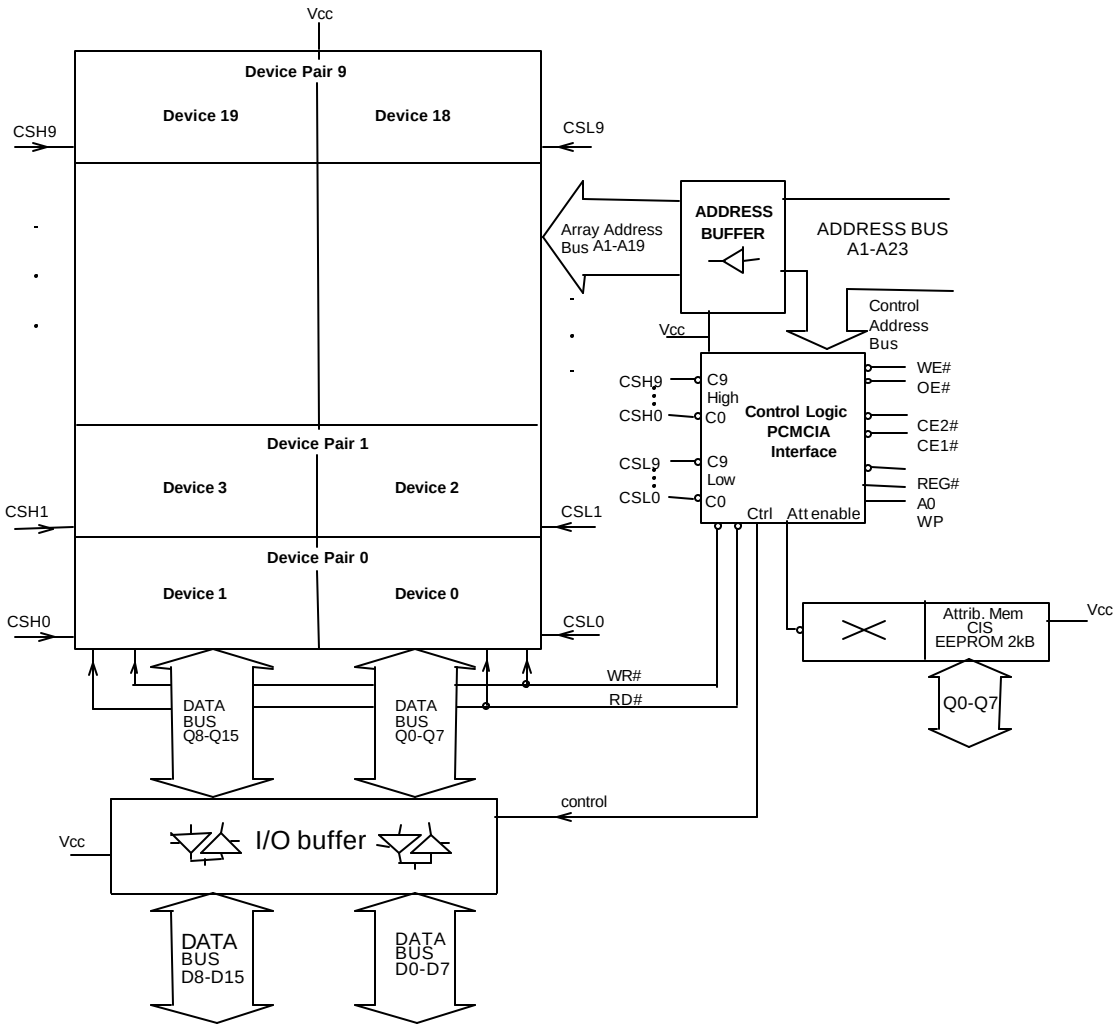
- **Low cost Medium/High Density Linear Flash Card**
- **Based on AMD Am29F040 Components (equivalent of AMD's AmC0XXCFLKA)**
- **Single supply operation, no additional programming voltage required**
  - **5 V only for write, erase and read operations**
- **Fast Read Performance**
  - **150ns Maximum Access Time**
- **PCMCIA/JEIDA 68-pin standard**
  - **x8/ x16 Data Interface**
  - **type I Form Factor**
- **Automated write and erase operations**
  - **64Kbyte memory sectors for faster automated erase speed**
  - **Typically 1.5 s per single memory sector erase**
  - **Random address writes to previously erased bytes; 16µs per byte typical**
- **100,000 Erase/Program Cycles**

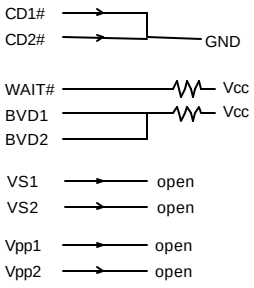
FLC Series Cards are based on the Am29F040 (4Mb) components which work with single 5V applications. Manufacture/Device code is 01h/A4h.

FLC series is designed to support from 2 to 20components, providing densities ranging from 1MB to 10MB in 1MB increments. In support of the PC Card 95 standard for word wide access devices are paired. Write, read and erase operations can be performed as either a word or byte wide operation . By multiplexing A0, CE1# and CE2#, 8-bit hosts can access all data on data lines DQ0 - DQ7. The FLC series cards conform to the PC Card Standard (PCMCIA) and JEIDA, providing electrical and physical compatibility. The PC Card form factor offers an industry standard pinout and mechanical outline, allowing density upgrades without system design changes.

WEDC's standard cards are shipped with WEDC's Logo. Cards are also available with blank housings (no Logo). The blank housings are available in both a recessed (for label) and flat housing. Please contact WEDC sales representative for further information on Custom artwork.

Block Diagram





SUPPORTED COMPONENTS (max 20 X):

Am29F040

Device type	Manuf ID	Device ID
Am29F040	$\mathbf{01}_H$	$\mathbf{A4}_H$

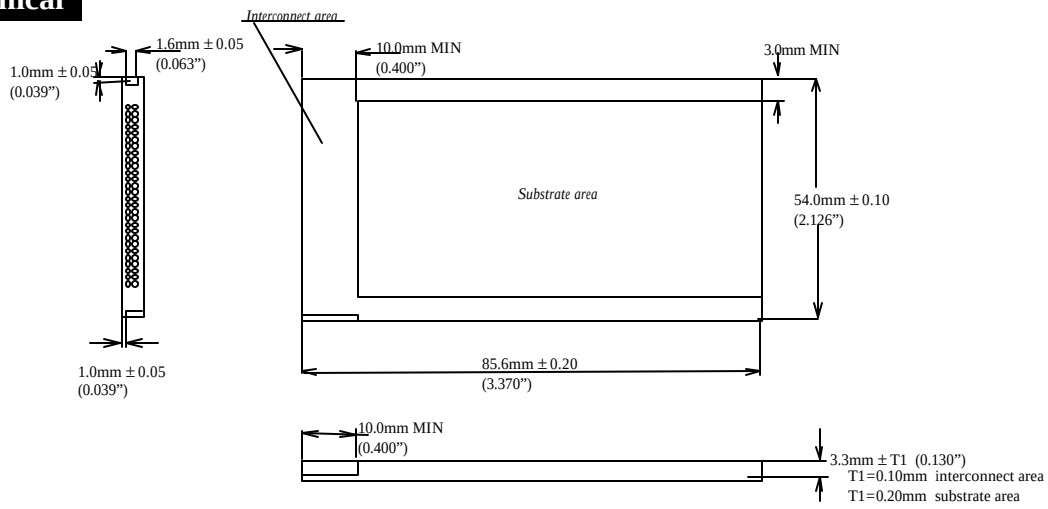
Pinout

Pin	Signal name	I/O	Function	Active
1	GND		Ground	
2	DQ3	I/O	Data bit 3	
3	DQ4	I/O	Data bit 4	
4	DQ5	I/O	Data bit 5	
5	DQ6	I/O	Data bit 6	
6	DQ7	I/O	Data bit 7	
7	CE1#	I	Card enable 1	LOW
8	A10	I	Address bit 10	
9	OE#	I	Output enable	LOW
10	A11	I	Address bit 11	
11	A9	I	Address bit 9	
12	A8	I	Address bit 8	
13	A13	I	Address bit 13	
14	A14	I	Address bit 14	
15	WE#	I	Write Enable	LOW
16	RDY/BSY#	O	Ready/Busy	N.C.
17	Vcc		Supply Voltage	
18	Vpp1		Prog. Voltage	N.C.
19	A16	I	Address bit 16	
20	A15	I	Address bit 15	
21	A12	I	Address bit 12	
22	A7	I	Address bit 7	
23	A6	I	Address bit 6	
24	A5	I	Address bit 5	
25	A4	I	Address bit 4	
26	A3	I	Address bit 3	
27	A2	I	Address bit 2	
28	A1	I	Address bit 1	
29	A0	I	Address bit 0	
30	DQ0	I/O	Data bit 0	
31	DQ1	I/O	Data bit 1	
32	DQ2	I/O	Data bit 2	
33	WP	O	Write Potect	HIGH
34	GND		Ground	

Pin	Signal name	I/O	Function	Active
35	GND		Ground	
36	CD1#	O	Card Detect 1	LOW
37	DQ11	I/O	Data bit 11	
38	DQ12	I/O	Data bit 12	
39	DQ13	I/O	Data bit 13	
40	DQ14	I/O	Data bit 14	
41	DQ15	I	Data bit 15	
42	CE2#	I	Card Enable 2	LOW
43	VS1	O	Voltage Sense 1	N.C.
44	RFU		Reserved	N.C.
45	RFU		Reserved	N.C.
46	A17	I	Address bit 17	
47	A18	I	Address bit 18	
48	A19	I	Address bit 19	1MB(2)
49	A20	I	Address bit 20	2MB(2)
50	A21	I	Address bit 21	4MB(2,3)
51	Vcc		Supply Voltage	
52	Vpp2		Prog. Voltage	N.C.
53	A22	I	Address bit 22	8MB(2,3)
54	A23	I	Address bit 23	16/10MB(2,3)
55	A24	I	Address bit 24	N.C.
56	A25	I	Address bit 25	N.C.
57	VS2	O	Voltage Sense 2	N.C.
58	RST	I	Card Reset	N.C.
59	Wait#	O	Extended Bus cycle	LOW(1)
60	RFU		Reserved	N.C.
61	REG#	I	Attrib Mem Select	LOW
62	BVD2	O	Bat. Volt. Detect 2	(1)
63	BVD1	O	Bat. Volt. Detect 1	(1)
64	DQ8	I/O	Data bit 8	
65	DQ9	I/O	Data bit 9	
66	DQ10	O	Data bit 10	
67	CD2#	O	Card Detect 2	LOW
68	GND		Ground	

Notes:
1) Wait#, BVD1 and BVD2 are driven high for compatibility
2) Shows density for which specified address bit is MSB. Higher order address bits are N.C. (i.e. 4MB A21 is MSB A22 - A25 are NC).
3) For the 3MB card the memory will wrap at the 4MB boundary, for 5MB, 6MB, and & 7MB cards the memory will wrap at the 8MB boundary, for 9MB and 10MB cards the memory will wrap at the 16MB boundary.

Mechanical



Card Signal Description

Symbol	Type	Name and Function
A0 - A25	INPUT	**ADDRESS INPUTS:** A0 through A25 enable direct addressing of up to 64MB of memory on the card. Signal A0 is not used in word access mode. The memory will wrap at the card density boundary (see PINOUT, note 3). The system should not try to access memory beyond the card density. A25 is the most significant bit. A24 – A25 are not connected.
DQ0 - DQ15	INPUT/OUTPUT	**DATA INPUT/OUTPUT:** DQ0 THROUGH DQ15 constitute the bi-directional databus. DQ0 – DQ7 constitute the lower (even) byte and DQ8 – DQ15 the upper (odd) byte. DQ15 is the MSB.
CE1#, CE2#	INPUT	**CARD ENABLE 1 AND 2:** CE1# enables even byte accesses, CE2# enables odd byte accesses. Multiplexing A0, CE1# and CE2# allows 8-bit hosts to access all data on DQ0 - DQ7.
OE#	INPUT	**OUTPUT ENABLE:** Active low signal gating read data from the memory card.
WE#	INPUT	**WRITE ENABLE:** Active low signal gating write data to the memory card.
RDY/BSY#	N.C.	**READY/BUSY OUTPUT:** Indicates status of internally timed erase or program algorithms. This signal is not connected.
CD1#, CD2#	OUTPUT	**CARD DETECT 1 and 2:** Provide card insertion detection. These signals are internally connected to ground on the card. The host shall monitor these signals to detect card insertion (pulled-up on host side).
WP	OUTPUT	**WRITE PROTECT:** Write protect reflects the status of the Write Protect switch on the memory card. WP set to high = write protected, providing internal hardware write lockout to the Flash array. If card does not include optional write protect switch, this signal will be pulled low internally indicating write protect = "off".
VPP1	N.C.	**PROGRAM/ERASE POWER SUPPLY:** Provides programming voltages 12.0V for lower byte (D0 – D7) memory components. This signal is not connected.
VPP2	N.C.	**PROGRAM/ERASE POWER SUPPLY:** Provides programming voltages 12.0V for upper byte (D8 – D15) memory components. This signal is not connected.
VCC		**CARD POWER SUPPLY:** (5.0V).
GND		**CARD GROUND**
REG#	INPUT	**ATTRIBUTE MEMORY SELECT :** Active low signal, enables access to Attribute Memory Plane, occupied by Card Information Structure and Card Registers.
RST	N.C.	**RESET:** Active high signal for placing cards in Power-on default state. This signal is not connected.
WAIT#	OUTPUT	**WAIT:** This signal is pulled high internally for compatibility. No wait states are generated.
BVD1, BVD2	OUTPUT	**BATTERY VOLTAGE DETECT:** These signals are pulled high to maintain SRAM card compatibility.
VS1, VS2	OUTPUT	**VOLTAGE SENSE:** Notifies the host socket of the card's VCC requirements. VS1 and VS2 are open to indicate a 5V card.
RFU		**RESERVED FOR FUTURE USE**
N.C.		**NO INTERNAL CONNECTION TO CARD:** pin may be driven or left floating

Functional Truth Table

READ function

						Common Memory			***Attribute Memory***		
Function Mode	/CE2	/CE1	A0	/OE	/WE	/REG	D15-D8	D7-D0	/REG	D15-D8	D7-D0
Standby Mode	H	H	X	X	X	X	High-Z	High-Z	X	High-Z	High-Z
Byte Access (8 bits)	H	L	L	L	H	H	High-Z	Even-Byte	L	High-Z	Even-Byte
	H	L	H	L	H	H	High-Z	Odd-Byte	L	High-Z	Not Valid
Word Access (16 bits)	L	L	X	L	H	H	Odd-Byte	Even-Byte	L	Not Valid	Even-Byte
Odd-Byte Only Access	L	H	X	L	H	H	Odd-Byte	High-Z	L	Not Valid	High-Z
WRITE function											
Standby Mode	H	H	X	X	X	X	X	X	X	X	X
Byte Access (8 bits)	H	L	L	H	L	H	X	Even-Byte	L	X	Even-Byte
	H	L	H	H	L	H	X	Odd-Byte	L	X	X
Word Access (16 bits)	L	L	X	H	L	H	Odd-Byte	Even-Byte	L	X	Even-Byte
Odd-Byte Only Access	L	H	X	H	L	H	Odd-Byte	X	L	X	X

Absolute Maximum Ratings (1)

Operating Temperature TA (ambient)	
Commercial	0°C to +60 °C
Industrial	-40°C to +85 °C
Storage Temperature	
Commercial	-30°C to +80 °C
Industrial	-40°C to +85 °C
Voltage on any pin relative to VSS	-0.5V to VCC+0.5V
VCC supply Voltage relative to VSS	-0.5V to +7.0V

Notes:
(1) Stress greater than those listed under "Absolute Maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC Characteristics(1)

Symbol	Parameter	Density	Notes	Typ(2)	Max	Units	Test Conditions
I_{CCR}	VCC Read Current	All			45	mA	VCC = VCCmax tcycle = 150ns,CMOS levels
I_{CCW}	VCC Program Current	All			65	mA	Programming in Progress
I_{CCE}	VCC Erase Current	All			65	mA	Erasure in Progress
I_{CCS} (CMOS)	VCC Standby Current	1MB		0.015	0.7	mA	VCC = VCCmax Control Signals = VCC CMOS levels
		2MB		0.015	0.9		
		4MB		0.015	1.3		
		10MB		0.015	2.5		

CMOS Test Conditions: VCC = 5V ± 5%, VIL = VSS ± 0.2V, VIH = VCC ± 0.2V

Notes:
1. All currents are RMS values unless otherwise specified. ICCR, ICCW and ICCE are based on Byte wide operations. For 16 bit operation values are double.
2. Typical: VCC = 5V, T = +25ºC

Symbol	Parameter	Notes	Min	Max	Units	Test Conditions
I_{LI}	Input Leakage Current	1		±20	µA	VCC = VCCMAX Vin =VCC or VSS
I_{LO}	Output Leakage Current	1		±20	µA	VCC = VCCMAX Vout =VCC or VSS
V_{IL}	Input Low Voltage	1	0	0.8	V	
V_{IH}	Input High Voltage	1	0.7VCC	VCC+0.5	V	
V_{OL}	Output Low Voltage	1		0.4	V	IOL = 3.2mA
V_{OH}	Output High Voltage	1	VCC-0.4	VCC	V	IOH = -2.0mA
V_{LKO}	VCC Erase/Program Lock Voltage	1	3.2	4.2	V	

Notes:
1) Values are the same for byte and word wide modes for all card densities.
2) Exceptions: Leakage currents on CE1#, CE2#, OE#, REG# and WE# will be < 500 µA when VIN = GND due to internal pull-up resistors.

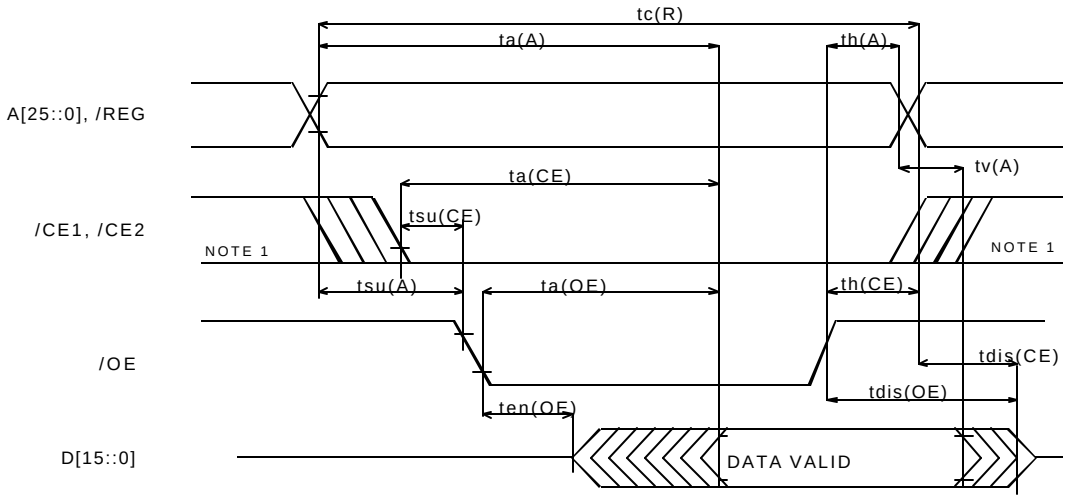
AC Characteristics

Read Timing Parameters

		150ns		
SYMBOL (PCMCIA)	**Parameter**	**Min**	**Max**	**Unit**
t_{RC}	Read Cycle Time	150		ns
t_a(A)	Address Access Time		150	ns
t_a(CE)	Card Enable Access Time		150	ns
t_a(OE)	Output Enable Access Time		75	ns
t_{su}(A)	Address Setup Time		20	ns
t_{su}(CE)	Card Enable Setup Time		0	ns
t_h(A)	Address Hold Time		20	ns
t_h(CE)	Card Enable Hold Time		20	ns
t_v(A)	Output Hold from Address Change		0	ns
t_{dis}(CE)	Output Disable Time from CE#		75	ns
t_{dis}(OE)	Output Disable Time from OE#		75	ns
t_{en}(CE)	Output Enable Time from CE#	5		ns
t_{en}(OE)	Output Enable Time from OE#	5		ns

Notes:
1. AC timing diagrams and characteristics are guaranteed to meet or exceed PCMCIA 2.1 specifications

Read Timing Diagram



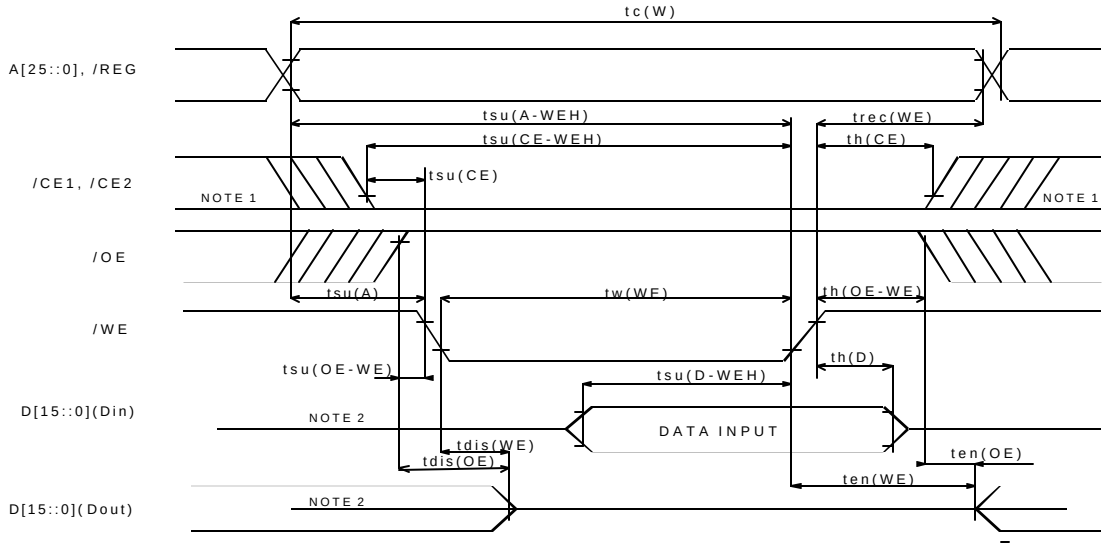
Note 1: Signal may be high or low in this area

Write Timing Parameters

		150ns		
SYMBOL (PCMCIA)	**Parameter**	**Min**	**Max**	**Unit**
t_{CW}	Write Cycle Time	150		ns
t_{w}(WE)	Write Pulse Width	80		ns
t_{su}(A)	Address Setup Time	20		ns
t_{su}(A-WEH)	Address Setup Time for WE#		100	ns
t_{su}(CE-WEH)	Card Enable Setup Time for WE#	100		ns
t_{su}(D-WEH)	Data Setup Time for WE#	50		ns
t_{h}(D)	Data Hold Time	20		ns
t_{rec}(WE)	Write Recover Time	20		ns
t_{dis}(WE)	Output Disable Time from WE#		75	ns
t_{dis}(OE)	Output Disable Time from OE#		75	ns
t_{en}(WE)	Output Enable Time from WE#	5		ns
t_{dis}(OE)	Output Enable Time from OE#	5		ns
t_{su}(OE-WE)	Output Enable Setup from WE#	10		ns
t_{h}(OE-WE)	Output Enable Hold from WE#	10		ns
t_{su}(CE)	Card Enable Setup Time from OE#	0		ns
t_{h}(CE)	Card Enable Hold Time	20		ns

Notes:
1. AC timing diagrams and characteristics are guaranteed to meet or exceed PCMCIA 2.1 specifications

Write Timing Diagram



Notes: 1)Signal may be high or low in this area
2)When the data I/O pins are in the output state, no signals shall be applied to the data pins (D15 - D0) by the host system.

Data Write and Erase Performance

VCC = 5V ± 5%, T_A = 25ºC

Parameter	Comments	Min	Typ[1]	Max	Units
Sector Erase Time	Excludes 00h programming prior to erasure		1.0	15	s
Chip Erase Time	Excludes 00h programming prior to erasure		8	120	s
Byte Programming Time	Excludes system-level overhead		7	1000[3]	µs
Chip Programming Time	Excludes system-level overhead		3.6	25[3, 4]	s

Notes:
1. Typical: Nominal voltages, T_A = 25ºC, 100,000 cycles
2. Although Embedded Algorithms allow for a longer chip program and erase time, the actual time will be considerably less since bytes program or erase significantly faster than the worst case byte.
3. Under worst case condition of 90°C, 4.5 V Vcc, 100,000 cycles.
4. The Embedded Algorithms allow for 2.5 ms byte program time. DQ5 = "1" only after a byte takes the theoretical maximum time to program. A minimal number of bytes may require significantly more programming pulses than the typical byte. The majority of the bytes will program within one or two pulses. This is demonstrated by the typical and maximum programming times.

CIS Information for FLC Series Cards

Address	Value	Description
00H	**01H**	**CISTPL_DEVICE**
02H	**03H**	TPL_LINK
04H	**53H**	FLASH = 150ns (device writable)
06H	**0DH**	Card Size:1MB
	06H	2MB
	2DH	3MB
	0EH	4MB
	4DH	5MB
	16H	6MB
	6DH	7MB
	1EH	8MB
	8DH	9MB
	26H	10MB
08H	**FFH**	END OF DEVICE
0AH	**18H**	**CISTPL_JEDEC_C**
0CH	**02H**	TPL_LINK
0EH	**01H**	AMD - ID
10H	**A4H**	Am29F040- ID
12H	**17H**	**CISTPL_DEVICE_A**
14H	**03H**	TPL_LINK
16H	**42H**	EEPROM - 200ns
18H	**01H**	Device Size = 2KBytes
1AH	**FFH**	END OF TUPLE
1CH	**1EH**	**CISTPL_DEVICEGEO**
1EH	**06H**	TPL_LINK
20H	**02H**	DGTPL_BUS
22H	**11H**	DGTPL_EBS
24H	**01H**	DGTPL_RBS
26H	**01H**	DGTPL_WBS
28H	**01H**	DGTPL_PART
2AH	**01H**	FLASH DEVICE NON-INTERLEAVED
2CH	**20H**	**CISTPL_MANFID**
2EH	**04H**	TPL_LINK(04H)
30H	**F6H**	**EDI** TPLMID_MANF: LSB
32H	**01H**	**EDI** TPLMID_MANF: MSB
34H	**00H**	*LSB: Number Not Assigned*
36H	**00H**	*MSB: Number Not Assigned*
38H	**15H**	**CISTPL_VERS1**
3AH	**47H**	TPL_LINK
3CH	**04H**	TPLLV1_MAJOR

Address	Value	Description
3EH	**01H**	TPLLV1_MINOR
40H	**45H**	E
42H	**44H**	D
44H	**49H**	I
46H	**37H**	7
48H	**50H**	P
4AH	**30H** 1)	0
4CH	**30H** 1)	0
4EH	**31H** 1)	1
50H	**46H**	F
52H	**4CH**	L
54H	**43H**	C
56H	**30H** 2)	0
58H	**32H** 2)	2
5AH	**2DH**	-
5CH	**2DH**	-
5EH	**2DH**	-
62H	**31H**	1
64H	**35H**	5
66H	**20H**	SPACE
68H	**00H**	END TEXT
6AH	**43H**	C
6CH	**4FH**	O
6EH	**50H**	P
70H	**59H**	Y
72H	**52H**	R
74H	**49H**	I
76H	**47H**	G
78H	**48H**	H
7AH	**54H**	T
7CH	**20H**	SPACE
7EH	**45H**	E
80H	**4CH**	L
82H	**45H**	E
84H	**43H**	C
86H	**54H**	T
88H	**52H**	R
8AH	**4FH**	O
8CH	**4EH**	N
8EH	**49H**	I
90H	**43H**	C

1)

Address	Value	Desc.	Value	Desc.	Value	Desc.	Value	Desc.	Value	Desc.	Value	Desc.	Value	Desc.	Value	Desc.	Value	Desc.
4AH	30H	0	30H	0	30H	0	30H	0	30H	0	30H	0	30H	0	30H	0	30H	0
4CH	30H	0	30H	0	30H	0	30H	0	30H	0	30H	0	30H	0	30H	0	31H	1
4EH	32H	2	33H	3	34H	4	35H	5	36H	6	37H	7	38H	8	39H	9	30H	0

2)

Address	Value	Description
56H	30H	0
58H	34H	4

CIS Information for FLC Series Cards - contd.

92H	**20H**	SPACE
94H	**44H**	D
96H	**45H**	E
98H	**53H**	S
9AH	**49H**	I
9CH	**47H**	G
9EH	**4EH**	N
A0H	**53H**	S
A2H	**20H**	SPACE
A4H	**49H**	I
A6H	**4EH**	N
A8H	**43H**	C
AAH	**4FH**	O
ACH	**52H**	R
AEH	**50H**	P
B0H	**4FH**	O
B2H	**52H**	R
B4H	**41H**	A
B6H	**54H**	T
B8H	**45H**	E
BAH	**44H**	D
BCH	**20H**	SPACE
BEH	**00H**	END TEXT
C0H	**31H**	1
C2H	**39H**	9
C4H	**39H**	9
C6H	**37H**	7
C8H	**00H**	END TEXT
CAH	**00H**	END OF LIST
CCH	**FFH**	**CISTPL_END**

Ordering Information

EDI 7P XXX FLC YY SS T ZZ Based on **Am29F040**

where

XXX:	**001**	**1MB**
	002	**2MB**
	003	**3MB**
	004	**4MB**
	005	**5MB**
	006	**6MB**
	007	**7MB**
	008	**8MB**
	009	**9MB**
	010	**10MB**

YY:	**01**	**No Attribute memory, no Write Protect switch**
	02	**Attribute memory, no Write Protect switch**
	03	**No Attribute memory, with Write Protect switch**
	04	**Attribute memory, with Write Protect switch**

SS:	**00**	**WEDC Silkscreen**
	01	**Blank Housing, Type I**
	02	**Blank Housing, Type I Recessed**

T:	**C**	**Commercial**
	I**	**Industrial**

ZZ:	**15**	**150ns**

NOTE: options without attribute memory and with/without hardware write protect switch are available.

White Electronic Designs, Corp

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fax: (508) 836 4850

www.whiteedc.com

WHITE ELECTRONIC DESIGNS

REVISION HISTORY		
Date of revision	**revision**	**Description**
23-Dec-98	0	Initial release
28-Jul-99	1	Logo change

** Denotes advanced information