

**Single/Dual Low Bias Current, Low Voltage, Rail-to-Rail  
Input/Output CMOS Operational Amplifiers**
**AZV831/2**
**General Description**

The AZV831/AZV832 is single/dual channels rail-to-rail input and output amplifier, which provides a wide input common-mode voltage range and output voltage swing capability for maximum signal swings in low supply voltage applications. The device is fully specified to operate from 1.6V to 5.0V single supply, or  $\pm 0.8V$  and  $\pm 2.5V$  dual supply applications. It features very low supply current dissipation  $70\mu A$  per channel, which is well suitable for today's low-voltage and/or portable systems.

The AZV831/AZV832 features optimal performance in very low bias current of  $1pA$ , which enables the IC to be used for integrators, photodiode amplifiers, and piezoelectric sensors etc. The device has typical  $0.5mV$  input offset voltage and provides  $1MHz$  bandwidth.

The AZV831/AZV832 adopts the latest packaging technology to meet the most demanding space-constraint applications. The AZV831 is available in standard SOT-23-5 and SC-70-5 packages. The AZV832 is offered in the traditional MSOP-8 and SOIC-8 packages.

**Features**

- Single Supply Voltage Range: 1.6V to 5.5V
- Ultra-low Input Bias Current:  $1pA$  (Typ.)
- Offset Voltage:  $0.5mV$  (Typ.),  $2.5mV$  (Max.)
- Rail-to-Rail Input  
 $V_{CM}$ :  $300mV$  beyond Rails @  $V_{CC}=5V$
- Rail-to-Rail Output Swing:  
 $10k\Omega$  Load:  $4mV$  from Rail  
 $1k\Omega$  Load:  $25mV$  from Rail
- Supply Current:  $70\mu A$ /Amplifier
- Unity Gain Stable  
 Gain Bandwidth Product:  $1.0MHz$
- Slew Rate:  $0.45V/\mu s$  @  $V_{CC}=5.0V$
- Operation Ambient Temperature Range:  $-40^{\circ}C$  to  $85^{\circ}C$

**Applications**

- Sensors
- Photodiode Amplification
- Battery-Powered Instrumentation
- Pulse Blood Oximeter, Glucose Meter

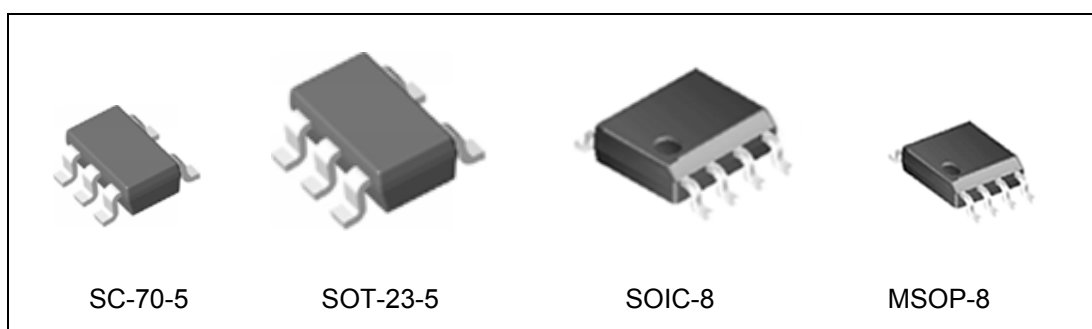
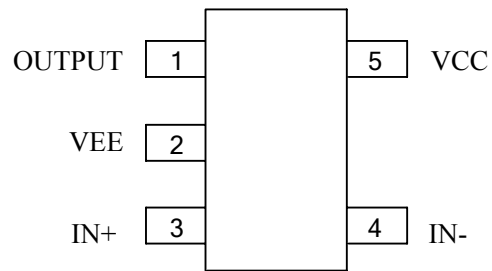
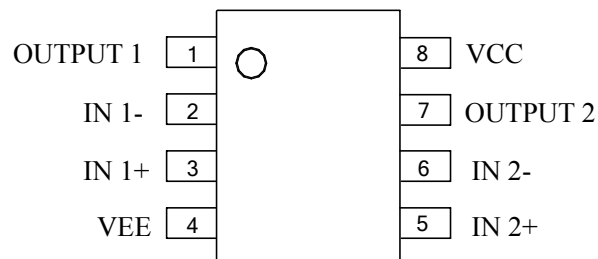


Figure 1. Package Types of AZV831/AZV832

**Single/Dual Low Bias Current, Low Voltage, Rail-to-Rail  
Input/Output CMOS Operational Amplifiers****AZV831/2****Pin Configuration**KS/K Package  
(SC-70-5/SOT-23-5)

AZV831

M/MM Package  
(SOIC-8/MSOP-8)

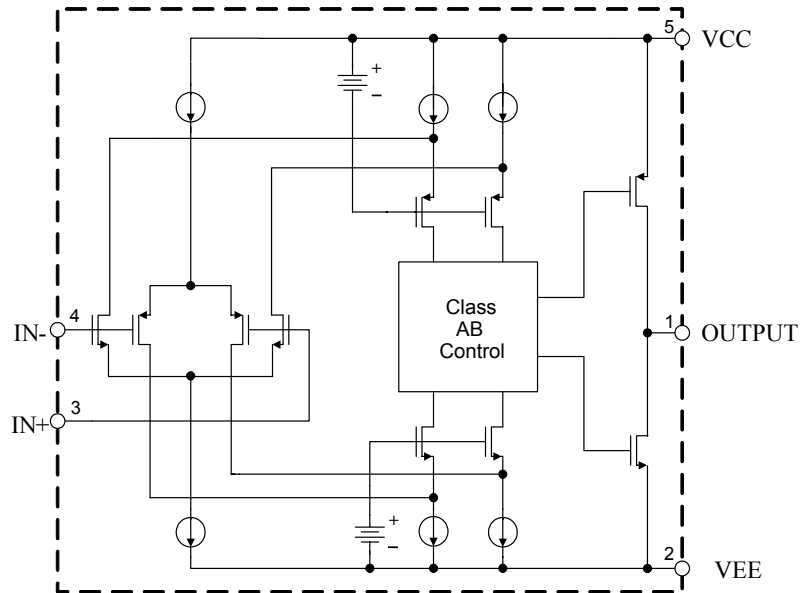
AZV832

Figure 2. Pin Configuration of AZV831/2 (Top View)

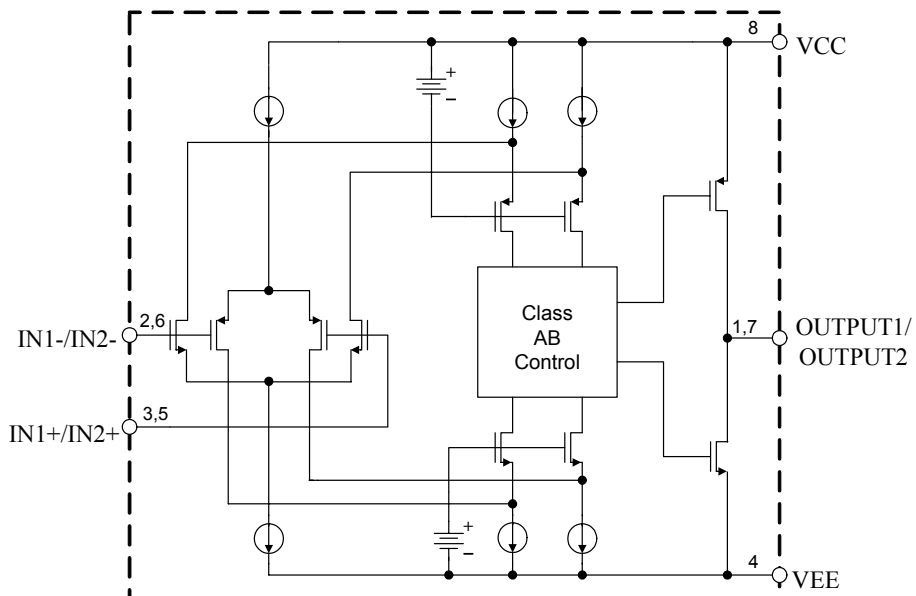
**Single/Dual Low Bias Current, Low Voltage, Rail-to-Rail  
Input/Output CMOS Operational Amplifiers**

**AZV831/2**

**Function Block Diagram**



For AZV831



For AZV832/Amplifier

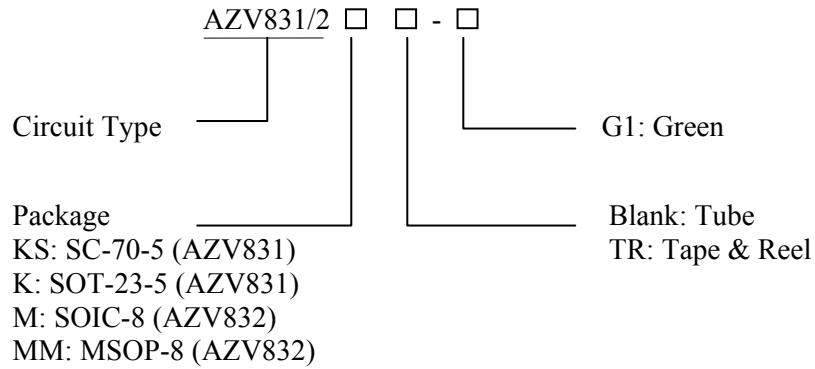
Figure 3. Functional Block Diagram of AZV831/2



**Single/Dual Low Bias Current, Low Voltage, Rail-to-Rail  
Input/Output CMOS Operational Amplifiers**

**AZV831/2**

**Ordering Information**



Package	Temperature Range	Part Number	Marking ID	Packing Type
SC-70-5	-40 to 85°C	AZV831KSTR-G1	L3	Tape & Reel
SOT-23-5	-40 to 85°C	AZV831KTR-G1	G4D	Tape & Reel
SOIC-8	-40 to 85°C	AZV832M-G1	832M-G1	Tube
		AZV832MTR-G1	832M-G1	Tape & Reel
MSOP-8	-40 to 85°C	AZV832MM-G1	832MM-G1	Tube
		AZV832MMTR-G1	832MM-G1	Tape & Reel

BCD Semiconductor's Pb-free products, as designated with "G1" suffix in the part number, are RoHS compliant and green.

**Single/Dual Low Bias Current, Low Voltage, Rail-to-Rail  
Input/Output CMOS Operational Amplifiers****AZV831/2****Absolute Maximum Ratings (Note 1)**

Parameter	Symbol	Value	Unit
Power Supply Voltage	$V_{CC}$	6.0	V
Differential Input Voltage	$V_{ID}$	6.0	V
Input Voltage	$V_{IN}$	-0.3 to $V_{CC}+0.5$	V
Operating Junction Temperature	$T_J$	150	°C
Thermal Resistance (Junction to Ambient)	$\theta_{JA}$	SC-70-5	270
		SOT-23-5	220
		SOIC-8	150
		MSOP-8	200
Storage Temperature Range	$T_{STG}$	-65 to 150	°C
Lead Temperature (Soldering,10 Seconds)	$T_{LEAD}$	260	°C
ESD (Human Body Model)		4000	V
ESD (Machine Model)		300	V

Note 1: Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “Recommended Operating Conditions” is not implied. Exposure to “Absolute Maximum Ratings” for extended periods may affect device reliability.

**Recommended Operating Conditions**

Parameter	Symbol	Min	Max	Unit
Supply Voltage	$V_{CC}$	1.6	5.5	V
Operation Ambient Temperature Range	$T_A$	-40	85	°C



**Single/Dual Low Bias Current, Low Voltage, Rail-to-Rail  
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**AZV831/2**

**1.6V DC Electrical Characteristics**

$V_{CC}=1.6V, V_{EE}=0, V_{OUT}=V_{CC}/2, V_{CM}=V_{CC}/2, T_A=25^{\circ}C$ , unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input Offset Voltage	$V_{OS}$			0.5	2.5	mV
Input Bias Current	$I_B$			1.0		pA
Input Offset Current	$I_{OS}$			1.0		pA
Input Common-mode Voltage Range	$V_{CM}$		-0.2		1.8	V
Common-mode Rejection Ratio	CMRR	$V_{CM}=-0.2V$ to $1.8V$	55	75		dB
Large Signal Voltage Gain	$G_V$	$R_L=10k\Omega$ to $V_{CC}/2$ , $V_{OUT}=0.2V$ to $1.4V$	90	110		dB
Input Offset Voltage Drift	$\Delta V_{OS}/\Delta T$			2.0		$\mu V/^{\circ}C$
Output Voltage Swing from Rail	$V_{OL}/V_{OH}$	$R_L=1k\Omega$ to $V_{CC}/2$		30	50	mV
		$R_L=10k\Omega$ to $V_{CC}/2$		3	15	
Output Current	Sink	$I_{SINK}$	$V_{OUT}=V_{CC}$	8	10	mA
	Source	$I_{SOURCE}$	$V_{OUT}=0V$	5	8.5	
Closed-loop Output Impedance	$Z_{OUT}$	$f=10kHz, A_V=1$		9		$\Omega$
Power Supply Rejection Ratio	PSRR	$V_{CC}=1.6V$ to $5.0V$	66	80		dB
Supply Current (Per Amplifier)	$I_{CC}$	$V_{OUT}=V_{CC}/2, I_{OUT}=0$		70	90	$\mu A$

**1.6V AC Electrical Characteristics**

$V_{CC}=1.6V, V_{EE}=0, V_{OUT}=V_{CC}/2, V_{CM}=V_{CC}/2, T_A=25^{\circ}C$ , unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Gain Bandwidth Product	GBP	$R_L=100k\Omega$		1.0		MHz
Slew Rate (Note 2)	SR	1V Step, $C_L=100pF, R_L=10k\Omega$		0.32		$V/\mu s$
Phase Margin	$\phi_M$	$R_L=100k\Omega$		67		Degrees
Total Harmonic Distortion+Noise	THD+N	$f=1kHz, A_V=1, V_{IN}=1V_{pp}$ $R_L=10k\Omega, C_L=100pF$		-70		dB
Voltage Noise Density	$e_n$	$f=1kHz$		27		$nV/\sqrt{Hz}$

Note 2: Number specified is the positive slew rate.



**Single/Dual Low Bias Current, Low Voltage, Rail-to-Rail  
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**1.8V DC Electrical Characteristics**

$V_{CC}=1.8V, V_{EE}=0, V_{OUT}=V_{CC}/2, V_{CM}=V_{CC}/2, T_A=25^{\circ}C$ , unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input Offset Voltage	$V_{OS}$			0.5	2.5	mV
Input Bias Current	$I_B$			1.0		pA
Input Offset Current	$I_{OS}$			1.0		pA
Input Common-mode Voltage Range	$V_{CM}$		-0.2		2.0	V
Common-mode Rejection Ratio	CMRR	$V_{CM}=-0.2V$ to $2.0V$	55	75		dB
Large Signal Voltage Gain	$G_V$	$R_L=10k\Omega$ to $V_{CC}/2$ , $V_{OUT}=0.2V$ to $1.6V$	90	112		dB
Input Offset Voltage Drift	$\Delta V_{OS}/\Delta T$			2.0		$\mu V/^{\circ}C$
Output Voltage Swing from Rail	$V_{OL}/V_{OH}$	$R_L=1k\Omega$ to $V_{CC}/2$		25	50	mV
		$R_L=10k\Omega$ to $V_{CC}/2$		3	15	
Output Current	Sink	$I_{SINK}$	$V_{OUT}=V_{CC}$	12	16	mA
	Source	$I_{SOURCE}$	$V_{OUT}=0V$	10	14	
Closed-loop Output Impedance	$Z_{OUT}$	$f=10kHz$		9		$\Omega$
Power Supply Rejection Ratio	PSRR	$V_{CC}=1.6V$ to $5.0V$	66	80		dB
Supply Current (Per Amplifier)	$I_{CC}$	$V_{OUT}=V_{CC}/2, I_{OUT}=0$		70	90	$\mu A$

**1.8V AC Electrical Characteristics**

$V_{CC}=1.8V, V_{EE}=0, V_{OUT}=V_{CC}/2, V_{CM}=V_{CC}/2, T_A=25^{\circ}C$ , unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Gain Bandwidth Product	GBP	$R_L=100k\Omega$		1.0		MHz
Slew Rate (Note 2)	SR	1V Step, $C_L=100pF, R_L=10k\Omega$		0.34		$V/\mu s$
Phase Margin	$\phi_M$	$R_L=100k\Omega$		67		Degrees
Total Harmonic Distortion+Noise	THD+N	$f=1kHz, A_V=1, V_{IN}=1V_{pp}$ $R_L=10k\Omega, C_L=100pF$		-70		dB
Voltage Noise Density	$e_n$	$f=1kHz$		27		$nV/\sqrt{Hz}$

Note 2: Number specified is the positive slew rate.



**Single/Dual Low Bias Current, Low Voltage, Rail-to-Rail  
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**3.0V DC Electrical Characteristics**

$V_{CC}=3.0V, V_{EE}=0, V_{OUT}=V_{CC}/2, V_{CM}=V_{CC}/2, T_A=25^{\circ}C$ , unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input Offset Voltage	$V_{OS}$			0.5	2.5	mV
Input Bias Current	$I_B$			1.0		pA
Input Offset Current	$I_{OS}$			1.0		pA
Input Common-mode Voltage Range	$V_{CM}$		-0.3		3.3	V
Common-mode Rejection Ratio	CMRR	$V_{CM}=-0.3V$ to 1.8V	62	80		dB
		$V_{CM}=-0.3V$ to 3.3V	58	75		
Large Signal Voltage Gain	$G_V$	$R_L=1k\Omega$ to $V_{CC}/2$ , $V_{OUT}=0.2V$ to 2.8V	90	110		dB
		$R_L=10k\Omega$ to $V_{CC}/2$ , $V_{OUT}=0.1V$ to 2.9V	95	115		
Input Offset Voltage Drift	$\Delta V_{OS}/\Delta T$			2.0		$\mu V/^{\circ}C$
Output Voltage Swing from Rail	$V_{OL}/V_{OH}$	$R_L=1k\Omega$ to $V_{CC}/2$		20	50	mV
		$R_L=10k\Omega$ to $V_{CC}/2$		3	15	
Output Current	Sink	$I_{SINK}$	$V_{OUT}=V_{CC}$	50	60	mA
	Source	$I_{SOURCE}$	$V_{OUT}=0V$	50	65	
Closed-loop Output Impedance	$Z_{OUT}$	$f=10kHz$		9		$\Omega$
Power Supply Rejection Ratio	PSRR	$V_{CC}=1.6V$ to 5.0V	66	80		dB
Supply Current (Per Amplifier)	$I_{CC}$	$V_{OUT}=V_{CC}/2, I_{OUT}=0$		70	90	$\mu A$

**3.0V AC Electrical Characteristics**

$V_{CC}=3.0V, V_{EE}=0, V_{OUT}=V_{CC}/2, V_{CM}=V_{CC}/2, T_A=25^{\circ}C$ , unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Gain Bandwidth Product	GBP	$R_L=100k\Omega$		1.0		MHz
Slew Rate (Note 2)	SR	$G=1, 2V$ Step, $C_L=100pF, R_L=10k\Omega$		0.40		V/ $\mu s$
Phase Margin	$\phi_M$	$R_L=100k\Omega$		67		Degrees
Total Harmonic Distortion+Noise	THD+N	$f=1kHz, G=1, V_{IN}=1V_{pp}$ $R_L=10k\Omega, C_L=100pF$		-70		dB
Voltage Noise Density	$e_n$	$f=1kHz$		27		$nV/\sqrt{Hz}$

Note 2: Number specified is the positive slew rate.





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**5.0V DC Electrical Characteristics**

$V_{CC}=5.0V, V_{EE}=0, V_{OUT}=V_{CC}/2, V_{CM}=V_{CC}/2, T_A=25^\circ C$ , unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input Offset Voltage	$V_{OS}$			0.5	2.5	mV
Input Bias Current	$I_B$			1.0		pA
Input Offset Current	$I_{OS}$			1.0		pA
Input Common-mode Voltage Range	$V_{CM}$		-0.3		5.3	V
Common-mode Rejection Ratio	CMRR	$V_{CM}=-0.3V$ to 3.8V	70	85		dB
		$V_{CM}=-0.3V$ to 5.3V	65	90		
Large Signal Voltage Gain	$G_V$	$R_L=1k\Omega$ to $V_{CC}/2$ , $V_{OUT}=0.2V$ to 4.8V	80	92		dB
		$R_L=10k\Omega$ to $V_{CC}/2$ , $V_{OUT}=0.05V$ to 4.95V	85	98		
Input Offset Voltage Drift	$\Delta V_{OS}/\Delta T$			2.0		$\mu V/^\circ C$
Output Voltage Swing from Rail	$V_{OL}/V_{OH}$	$R_L=1k\Omega$ to $V_{CC}/2$		25	50	mV
		$R_L=10k\Omega$ to $V_{CC}/2$		4	15	
Output Current	Sink	$I_{SINK}$	$V_{OUT}=V_{CC}$	100	150	mA
	Source	$I_{SOURCE}$	$V_{OUT}=0V$	110	185	
Closed-loop Output Impedance		$f=1kHz, A_V=1$		9		$\Omega$
Power Supply Rejection Ratio	PSRR	$V_{CC}=1.6V$ to 5.0V	66	80		dB
Supply Current (Per Amplifier)	$I_{CC}$	$V_{OUT}=V_{CC}/2, I_{OUT}=0$		70	90	$\mu A$

**5V AC Electrical Characteristics**

$V_{CC}=5.0V, V_{EE}=0, V_{OUT}=V_{CC}/2, V_{CM}=V_{CC}/2, T_A=25^\circ C$ , unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Gain Bandwidth Product	GBP	$R_L=100k\Omega$		1.0		MHz
Slew Rate (Note 2)	SR	2V Step, $C_L=100pF, R_L=10k\Omega$		0.45		V/ $\mu s$
Phase Margin	$\phi_M$	$R_L=100k\Omega$		67		Degrees
THD+N	THD+N	$f=1kHz, A_V=1, V_{IN}=1V_{PP}$ $R_L=10k\Omega, C_L=100pF$		-70		dB
Voltage Noise Density	$e_n$	$f=1kHz$		27		$nV/\sqrt{Hz}$

Note 2: Number specified is the positive slew rate.



**Single/Dual Low Bias Current, Low Voltage, Rail-to-Rail  
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**AZV831/2**

**Typical Performance Characteristics**

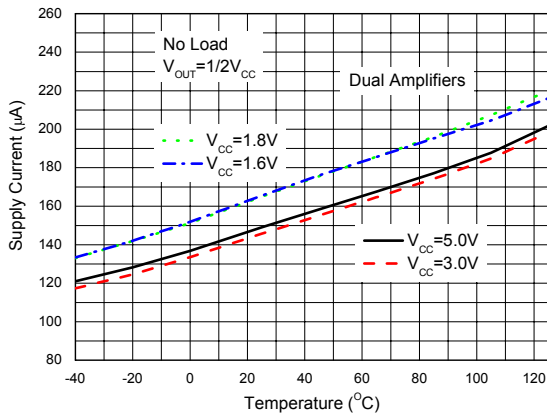


Figure 4. Supply Current vs. Temperature

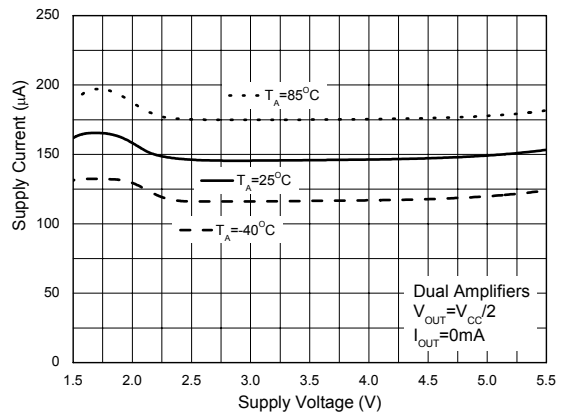


Figure 5. Supply Current vs. Supply Voltage

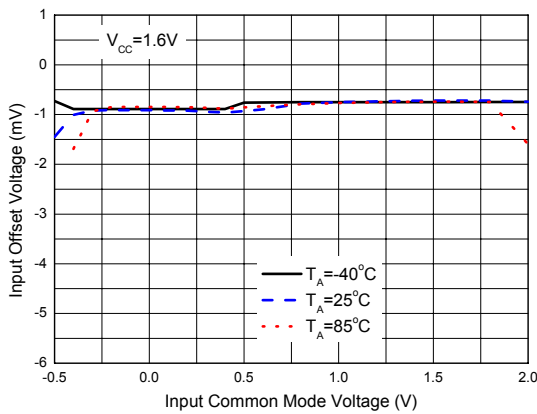


Figure 6. Input Offset Voltage vs. Input Common Mode Voltage

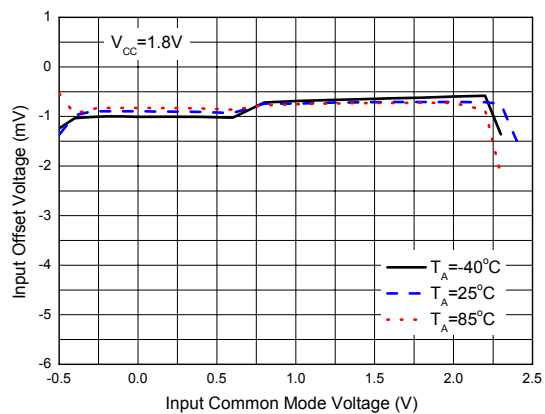


Figure 7. Input Offset Voltage vs. Input Common Mode Voltage

**Single/Dual Low Bias Current, Low Voltage, Rail-to-Rail  
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**Typical Performance Characteristics (Continued)**

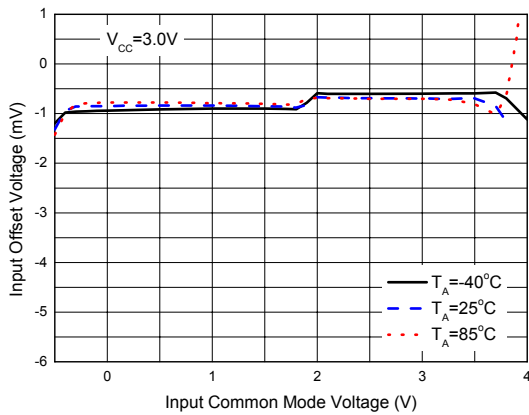


Figure 8. Input Offset Voltage vs. Input Common Mode Voltage

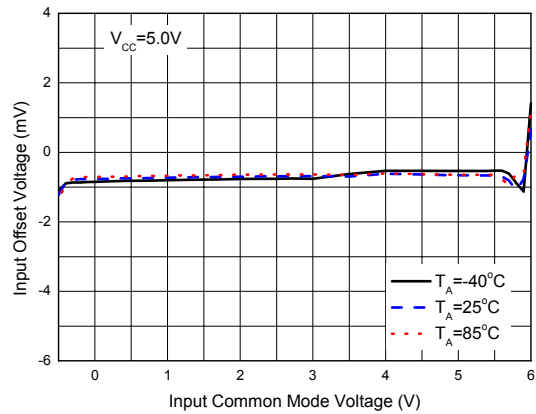


Figure 9. Input Offset Voltage vs. Input Common Mode Voltage

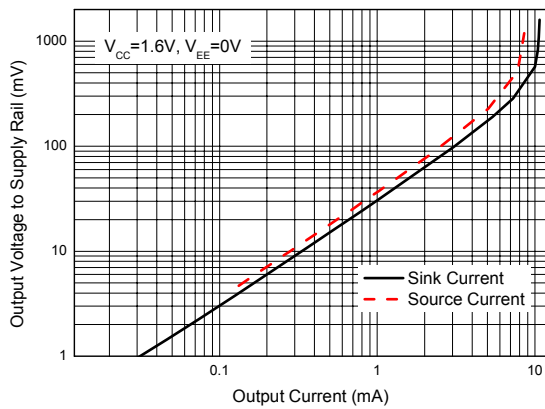


Figure 10. Output Voltage vs. Output Current

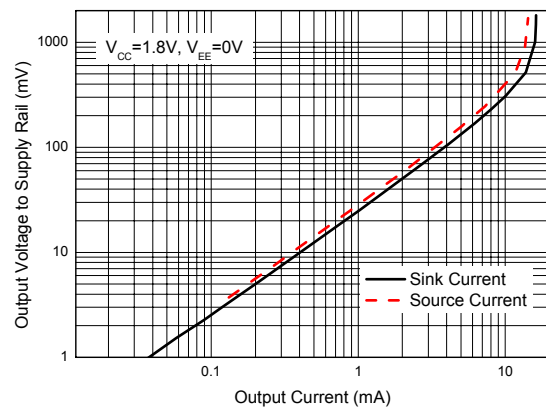


Figure 11. Output Voltage vs. Output Current



**Single/Dual Low Bias Current, Low Voltage, Rail-to-Rail  
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**Typical Performance Characteristics (Continued)**

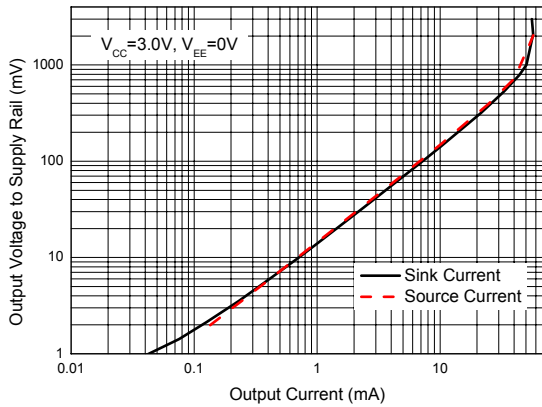


Figure 12. Output Voltage vs. Output Current

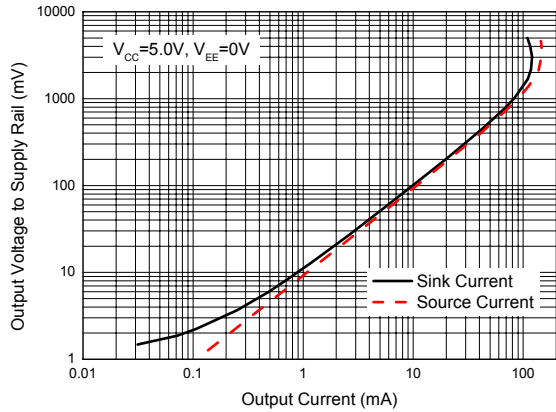


Figure 13. Output Voltage vs. Output Current

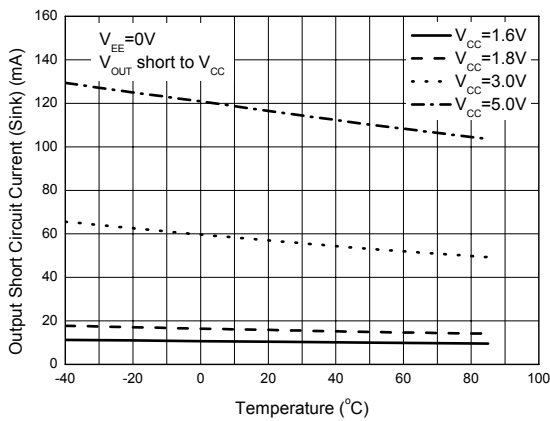


Figure 14. Output Short Circuit Current vs. Temperature

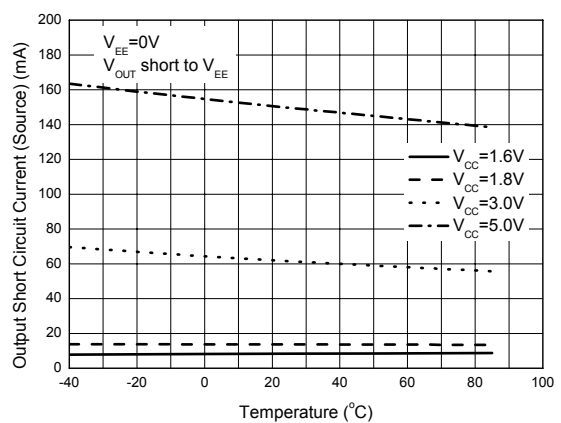


Figure 15. Output Short Circuit Current vs. Temperature

**Single/Dual Low Bias Current, Low Voltage, Rail-to-Rail  
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**Typical Performance Characteristics (Continued)**

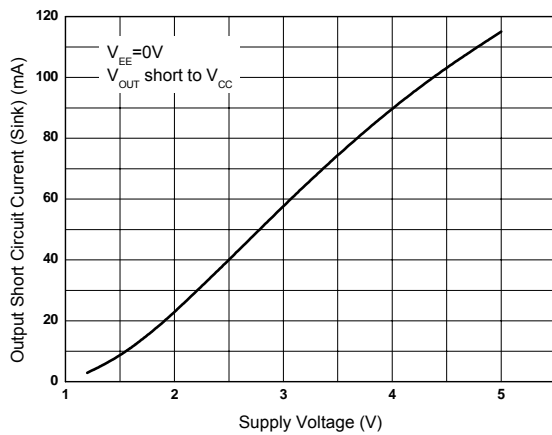


Figure 16. Output Short Circuit Current vs. Supply Voltage

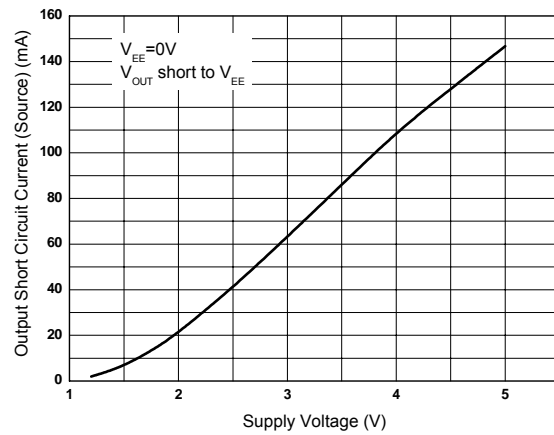


Figure 17. Output Short Circuit Current vs. Supply Voltage

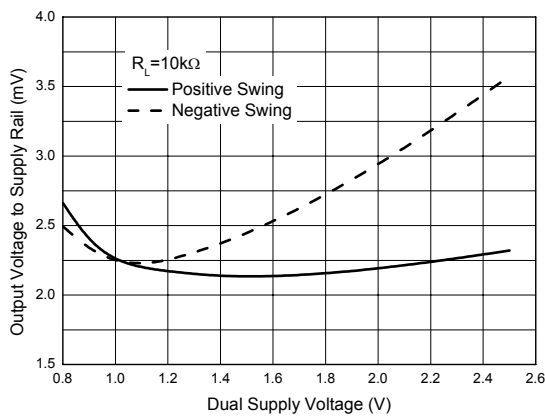


Figure 18. Output Voltage Swing vs. Supply Voltage

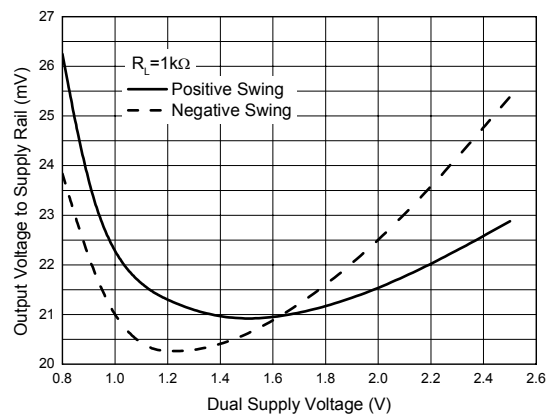


Figure 19. Output Voltage Swing vs. Supply Voltage

**Single/Dual Low Bias Current, Low Voltage, Rail-to-Rail  
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**Typical Performance Characteristics (Continued)**

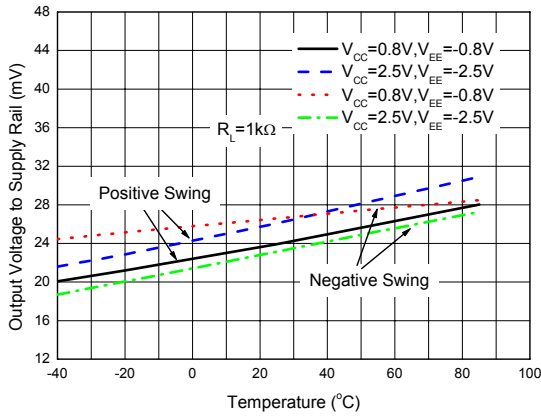


Figure 20. Output Voltage Swing vs. Temperature

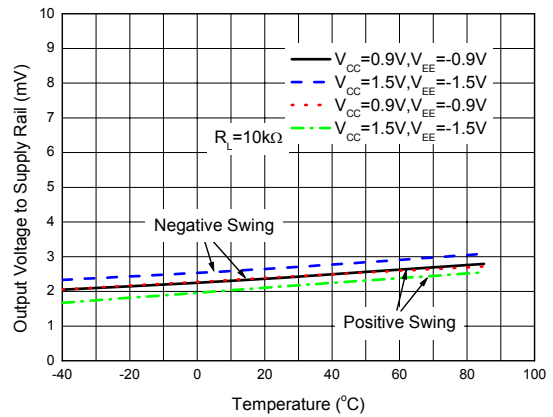


Figure 21. Output Voltage Swing vs. Temperature

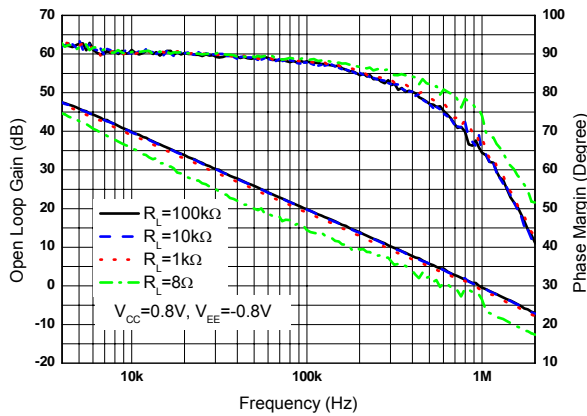


Figure 22. Gain and Phase vs. Frequency with Resistive Load

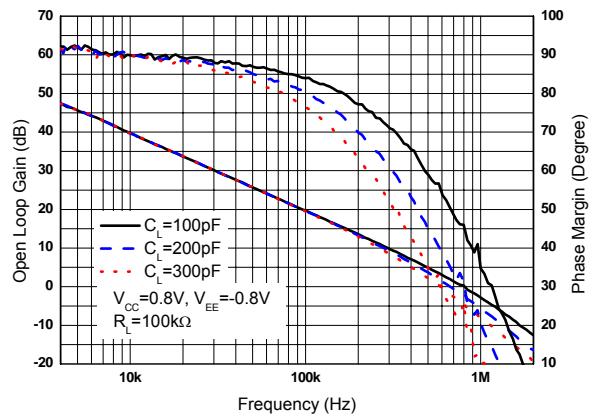


Figure 23. Gain and Phase vs. Frequency with Capacitive Load



Single/Dual Low Bias Current, Low Voltage, Rail-to-Rail  
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Typical Performance Characteristics (Continued)

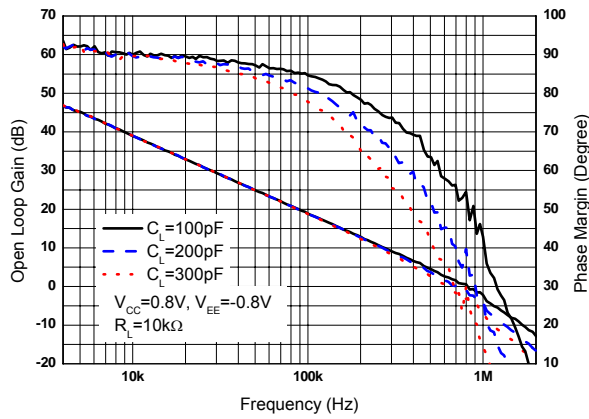


Figure 24. Gain and Phase vs. Frequency with Capacitive Load

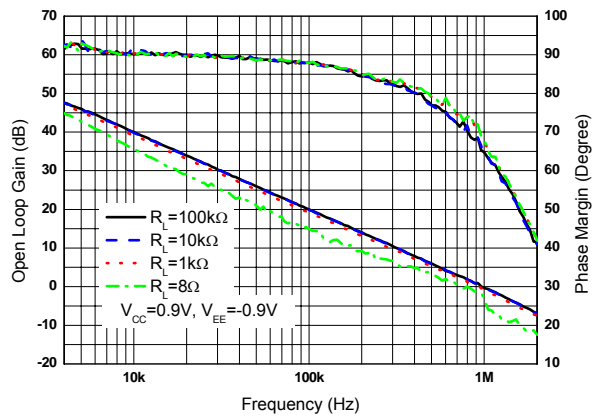


Figure 25. Gain and Phase vs. Frequency with Resistive Load

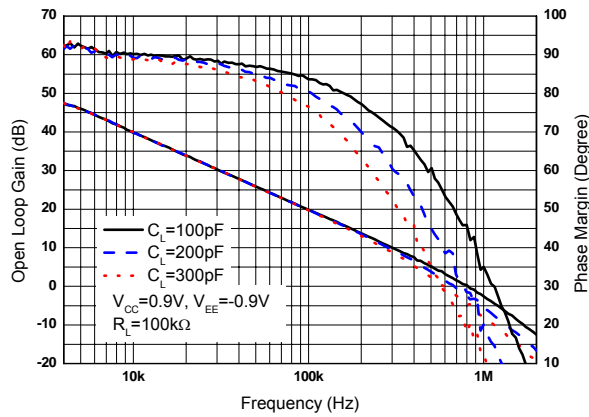


Figure 26. Gain and Phase vs. Frequency with Capacitive Load

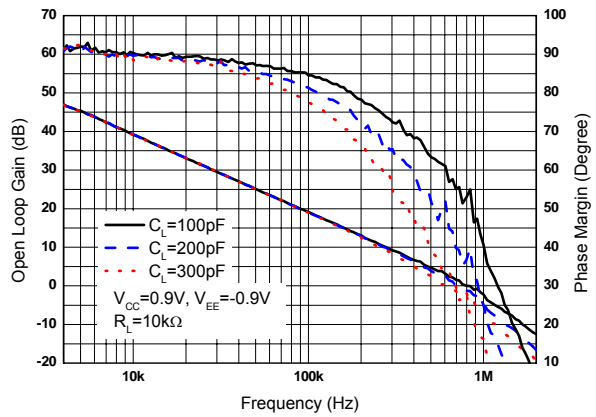


Figure 27. Gain and Phase vs. Frequency with Capacitive Load

**Single/Dual Low Bias Current, Low Voltage, Rail-to-Rail  
Input/Output CMOS Operational Amplifiers**

**AZV831/2**

**Typical Performance Characteristics (Continued)**

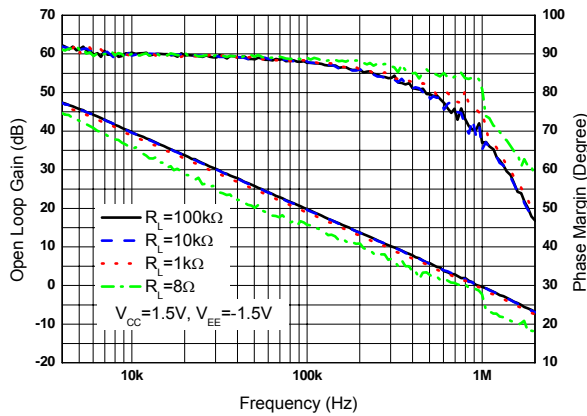


Figure 28. Gain and Phase vs. Frequency with Resistive Load

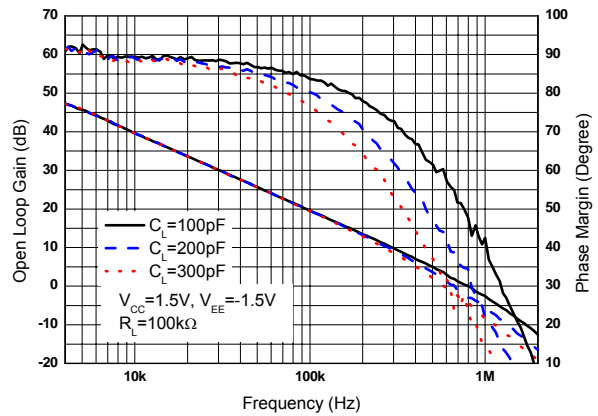


Figure 29. Gain and Phase vs. Frequency with Capacitive Load

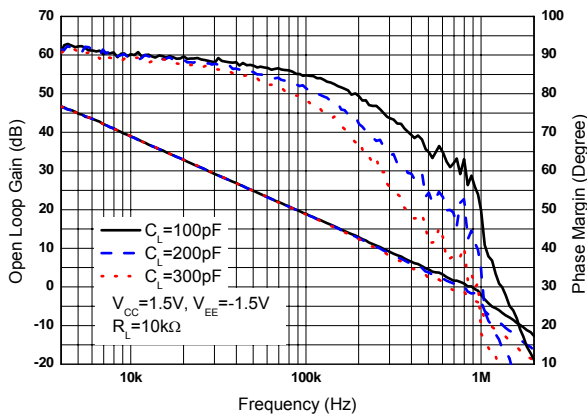


Figure 30. Gain and Phase vs. Frequency with Capacitive Load

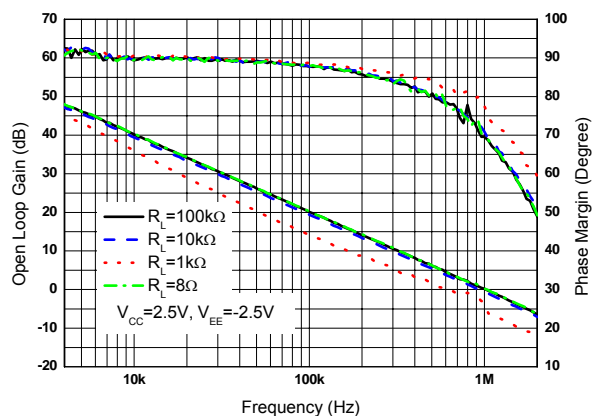


Figure 31. Gain and Phase vs. Frequency with Resistive Load





Single/Dual Low Bias Current, Low Voltage, Rail-to-Rail  
Input/Output CMOS Operational Amplifiers

AZV831/2

Typical Performance Characteristics (Continued)

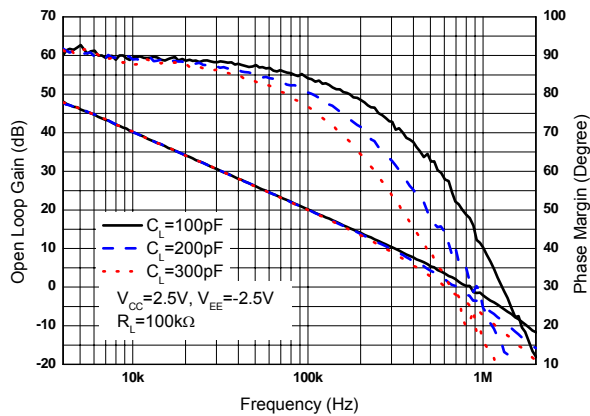


Figure 32. Gain and Phase vs. Frequency with Capacitive Load

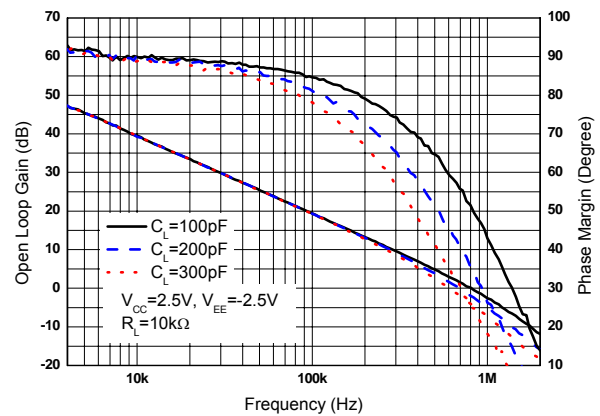


Figure 33. Gain and Phase vs. Frequency with Capacitive Load

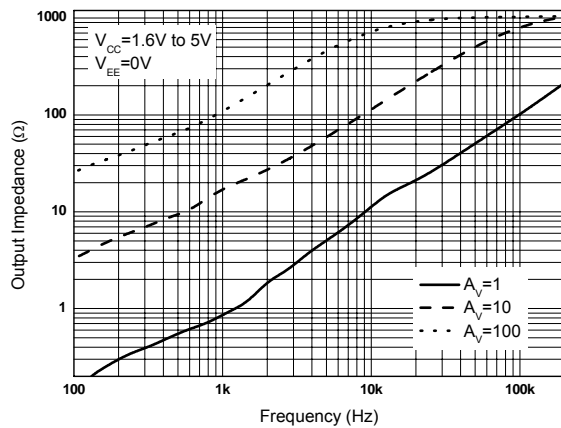


Figure 34. Output Impedance vs. Frequency

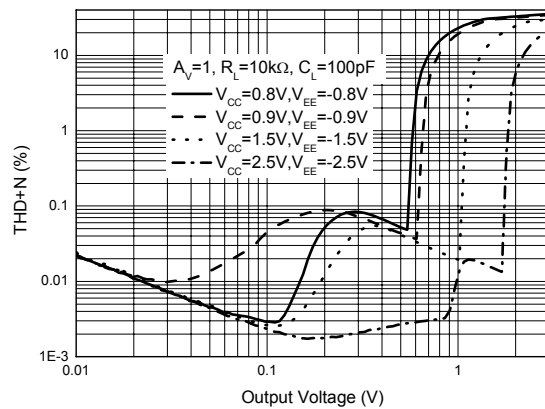


Figure 35. THD+N vs. Output Voltage

**Single/Dual Low Bias Current, Low Voltage, Rail-to-Rail  
Input/Output CMOS Operational Amplifiers**

**AZV831/2**

**Typical Performance Characteristics (Continued)**

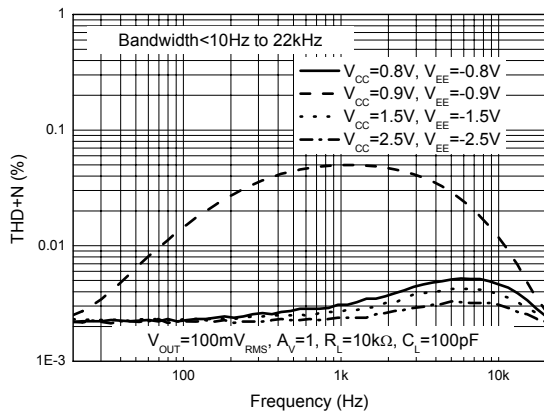


Figure 36. THD+N vs. Frequency

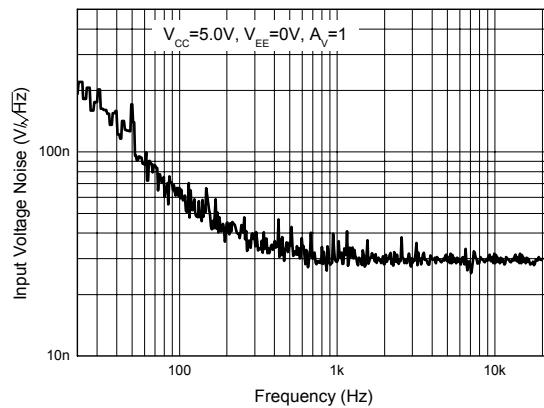
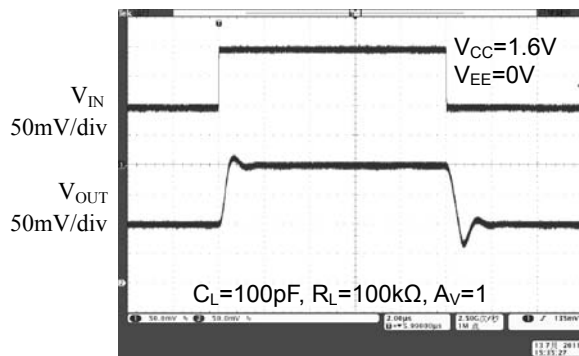
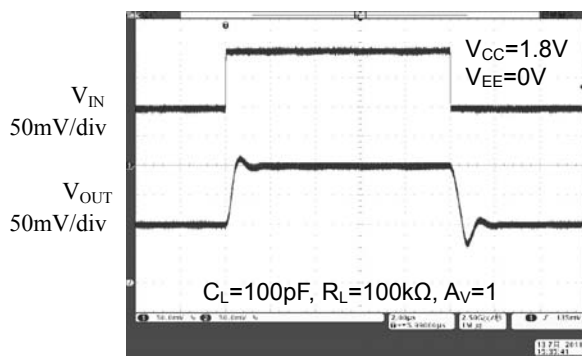


Figure 37. Input Voltage Noise Density



Time (2μs/div)

Figure 38. Small Signal Pulse Response



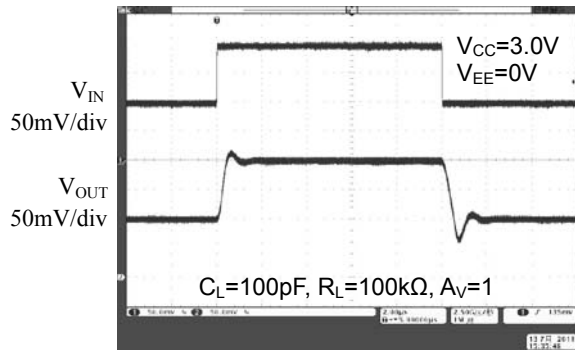
Time (2μs/div)

Figure 39. Small Signal Pulse Response

**Single/Dual Low Bias Current, Low Voltage, Rail-to-Rail  
Input/Output CMOS Operational Amplifiers**

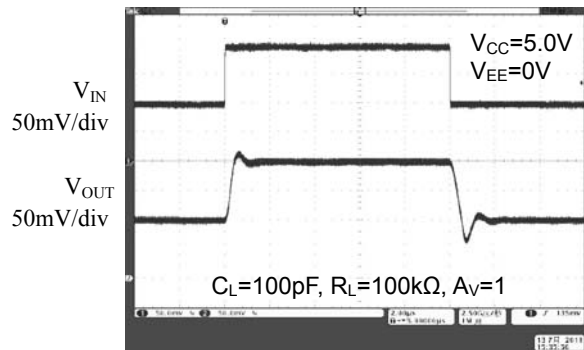
**AZV831/2**

**Typical Performance Characteristics (Continued)**



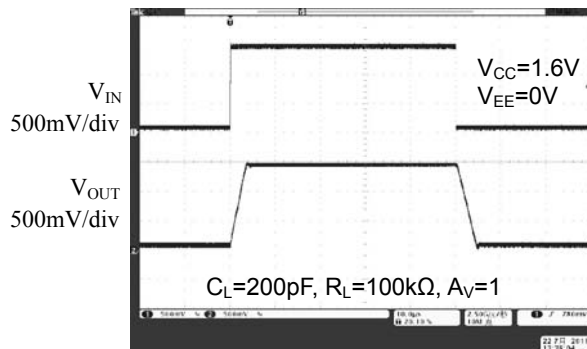
Time (2µs/div)

Figure 40. Small Signal Pulse Response



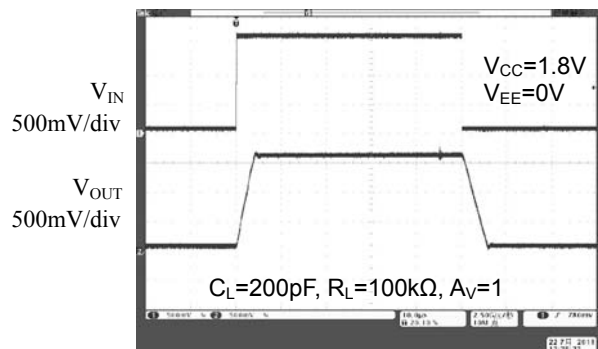
Time (2µs/div)

Figure 41. Small Signal Pulse Response



Time (10µs/div)

Figure 42. Large Signal Pulse Response



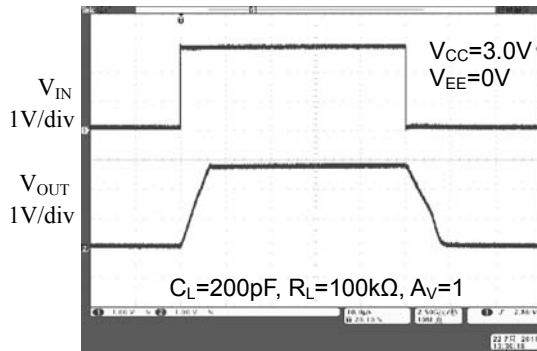
Time (10µs/div)

Figure 43. Large Signal Pulse Response

**Single/Dual Low Bias Current, Low Voltage, Rail-to-Rail  
Input/Output CMOS Operational Amplifiers**

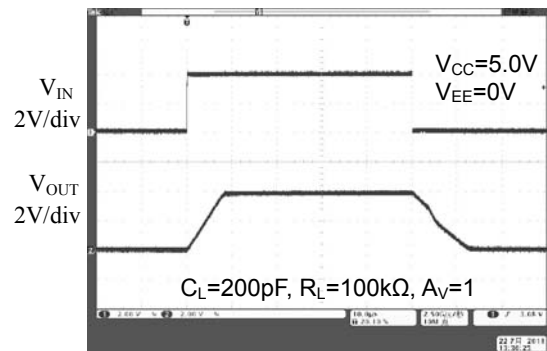
**AZV831/2**

**Typical Performance Characteristics (Continued)**



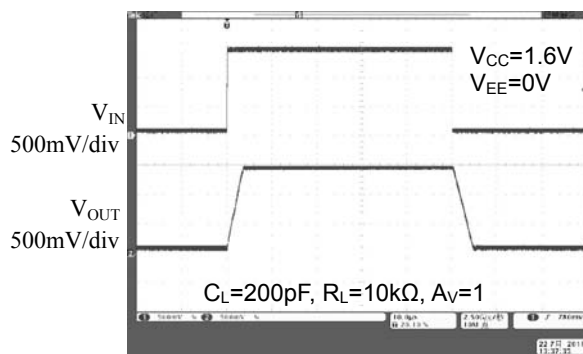
Time (10μs/div)

Figure 44. Large Signal Pulse Response



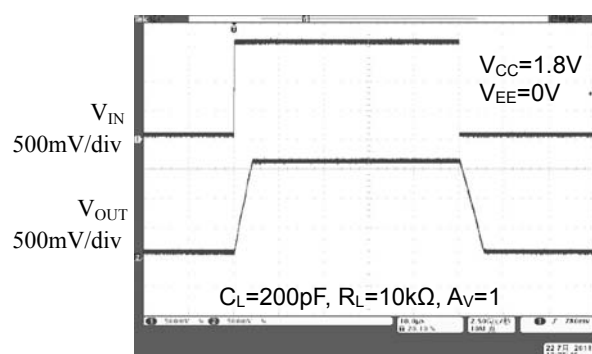
Time (10μs/div)

Figure 45. Large Signal Pulse Response



Time (10μs/div)

Figure 46. Large Signal Pulse Response



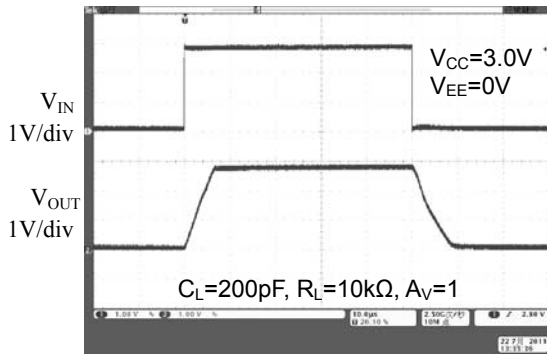
Time (10μs/div)

Figure 47. Large Signal Pulse Response

**Single/Dual Low Bias Current, Low Voltage, Rail-to-Rail  
Input/Output CMOS Operational Amplifiers**

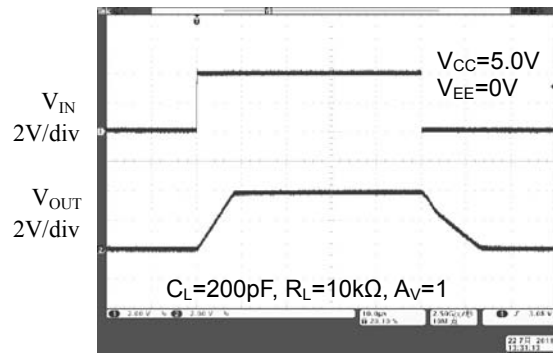
**AZV831/2**

**Typical Performance Characteristics (Continued)**



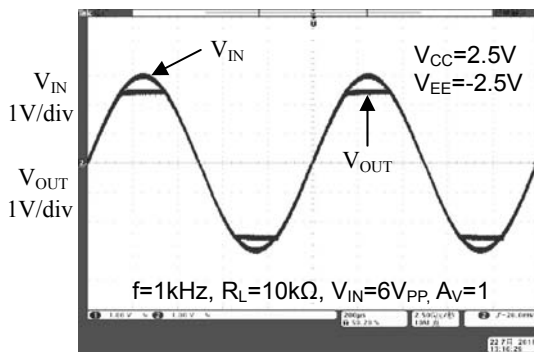
Time (10µs/div)

Figure 48. Large Signal Pulse Response



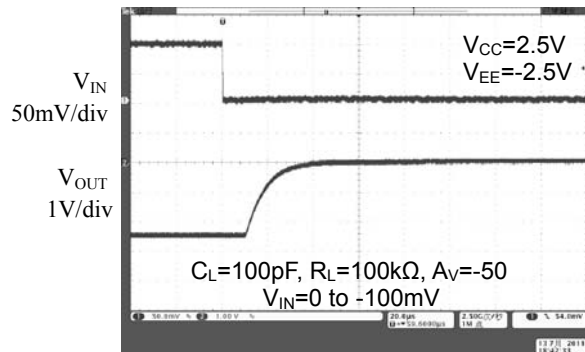
Time (10µs/div)

Figure 49. Large Signal Pulse Response



Time (200µs/div)

Figure 50. No Phase Reversal



Time (20µs/div)

Figure 51. Overload Recovery Time

**Single/Dual Low Bias Current, Low Voltage, Rail-to-Rail  
Input/Output CMOS Operational Amplifiers**

**AZV831/2**

**Typical Performance Characteristics (Continued)**

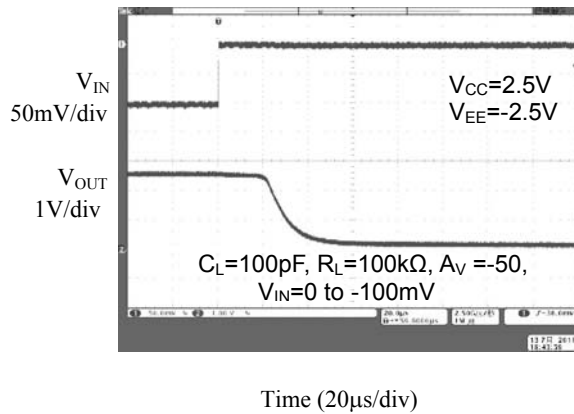


Figure 52. Overload Recovery Time

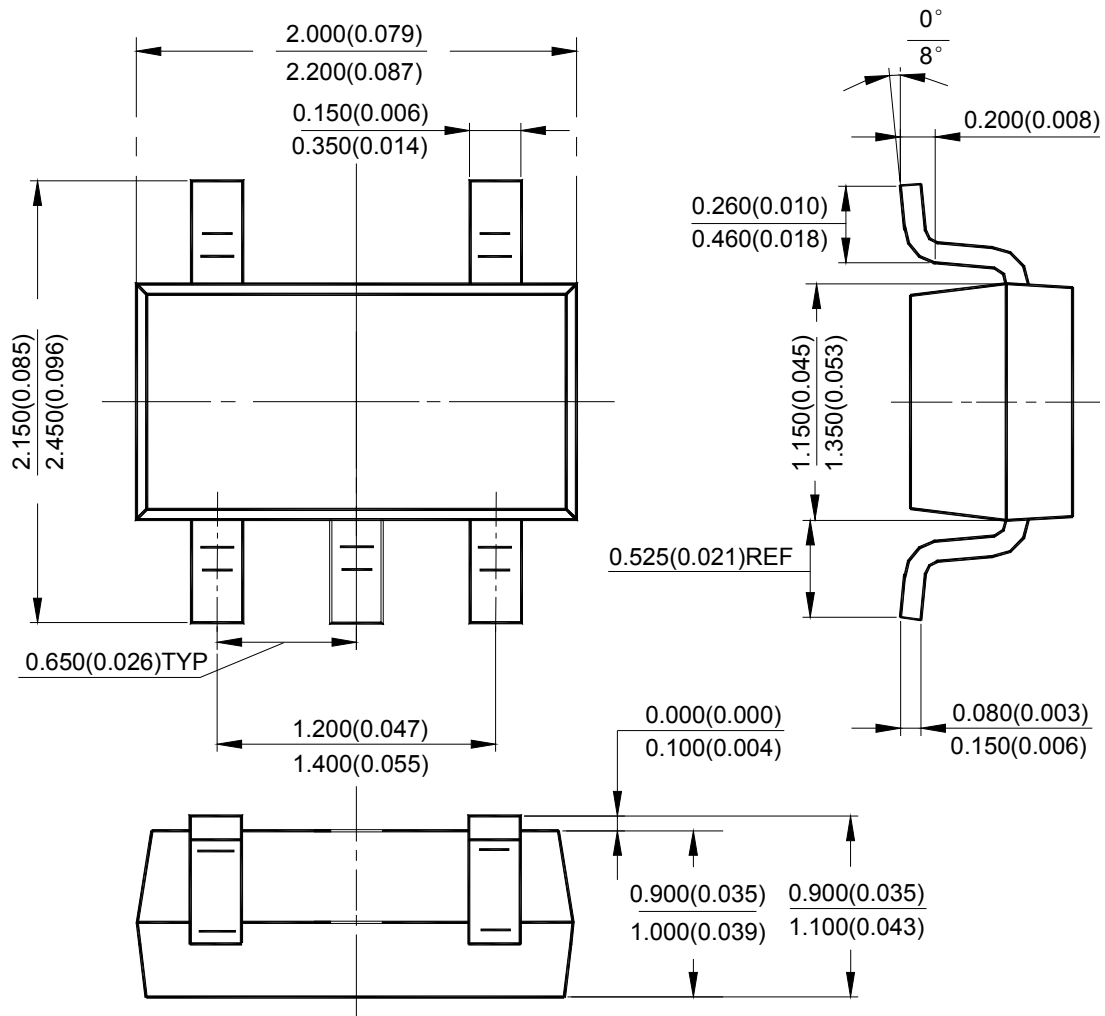
**Single/Dual Low Bias Current, Low Voltage, Rail-to-Rail  
Input/Output CMOS Operational Amplifiers**

**AZV831/2**

**Mechanical Dimensions**

**SC-70-5**

**Unit: mm(inch)**





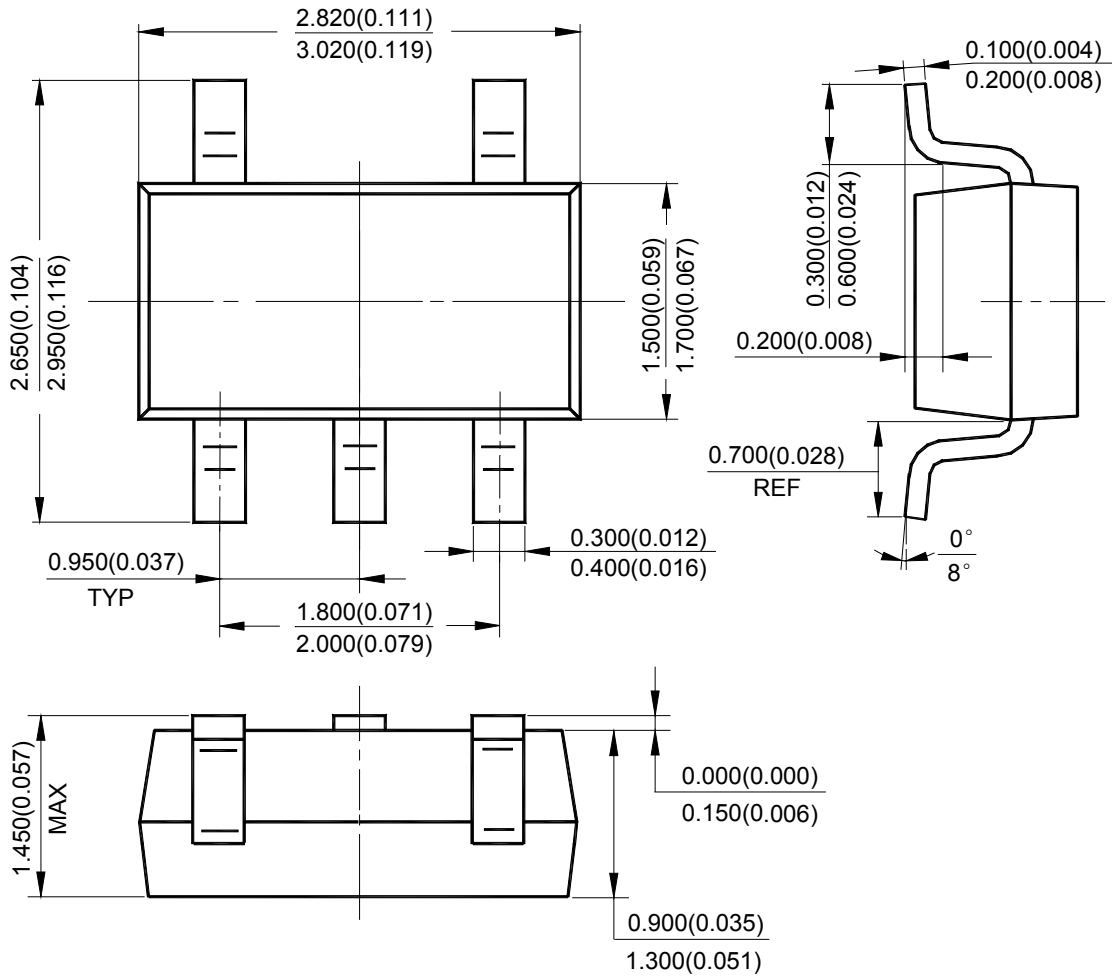
**Single/Dual Low Bias Current, Low Voltage, Rail-to-Rail  
Input/Output CMOS Operational Amplifiers**

**AZV831/2**

**Mechanical Dimensions (Continued)**

**SOT-23-5**

**Unit: mm(inch)**







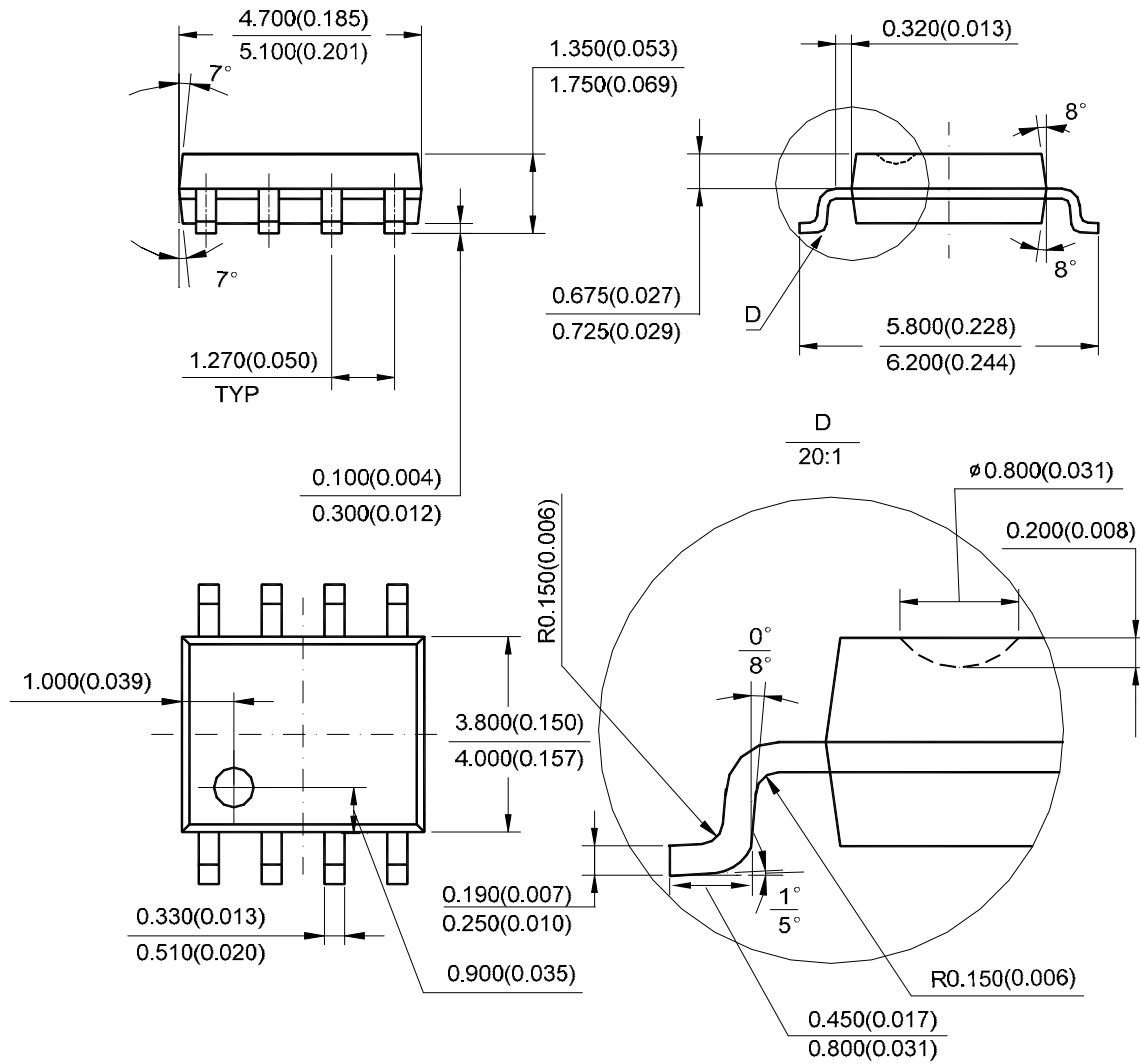
**Single/Dual Low Bias Current, Low Voltage, Rail-to-Rail  
Input/Output CMOS Operational Amplifiers**

**AZV831/2**

**Mechanical Dimensions (Continued)**

**SOIC-8**

**Unit: mm(inch)**



Note: Eject hole, oriented hole and mold mark is optional.

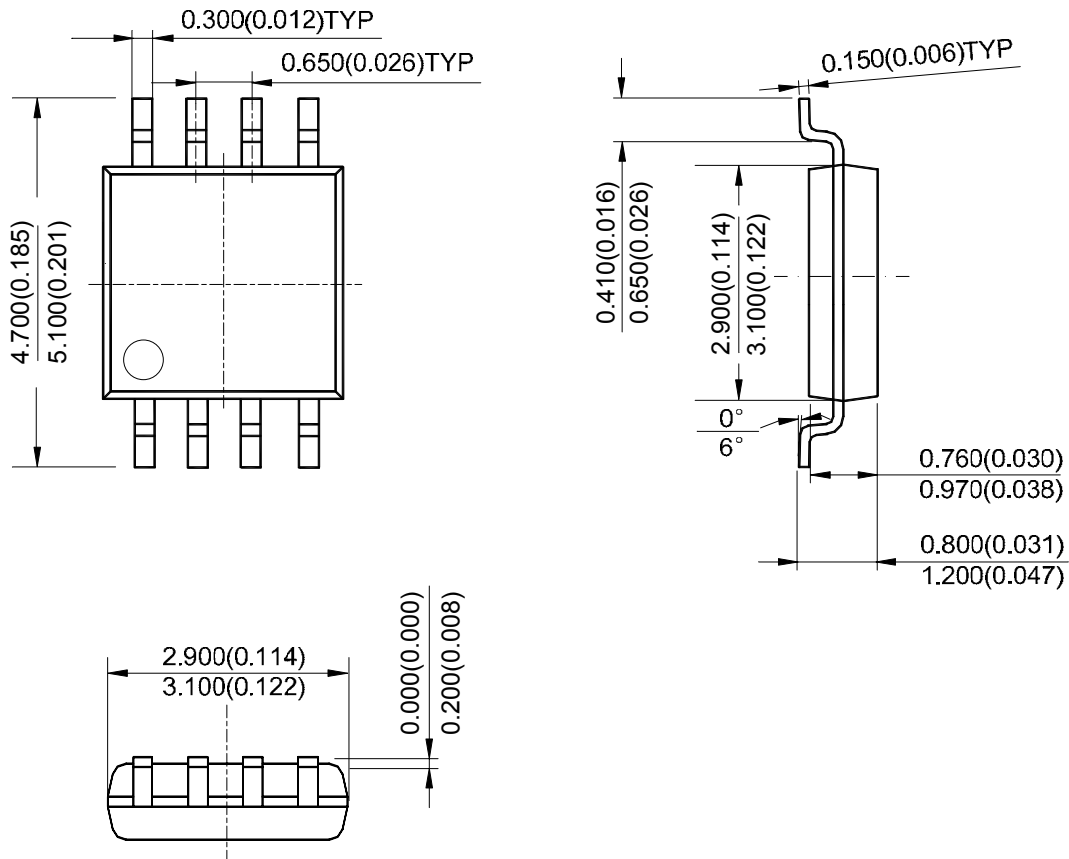
**Single/Dual Low Bias Current, Low Voltage, Rail-to-Rail  
Input/Output CMOS Operational Amplifiers**

**AZV831/2**

**Mechanical Dimensions (Continued)**

**MSOP-8**

**Unit: mm(inch)**



Note: Eject hole, oriented hole and mold mark is optional.



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