IC WORKS

W48C54A/55A

PRELIMINARY, JANUARY 1995

Frequency Generators

FEATURES

- New proprietary crystal oscillator circuitry provides low REFOUT jitter, excellent duty cycle
- Power-on delay feature ensures full VCC is reached prior to output clocks
- 3.3V and 5V operation supported including the VRE (Voltage Regulated Extended) specification for Pentium™ processor
- Pin and function compatible with W48C54/W48C55 and AV9154/AV9155
- Integral PLL loop filter components ensures stable PLL operation in noisy system environment
- Smooth, glitch free frequency transition of CPU and 2XCPU outputs
- Compatible with Intel x86 and other high performance processors
- Up to eight clock outputs for CPU and peripherals
- Supports Green PC and notebook designs
- Custom options available with metal layer change
- High performance, low power CMOS

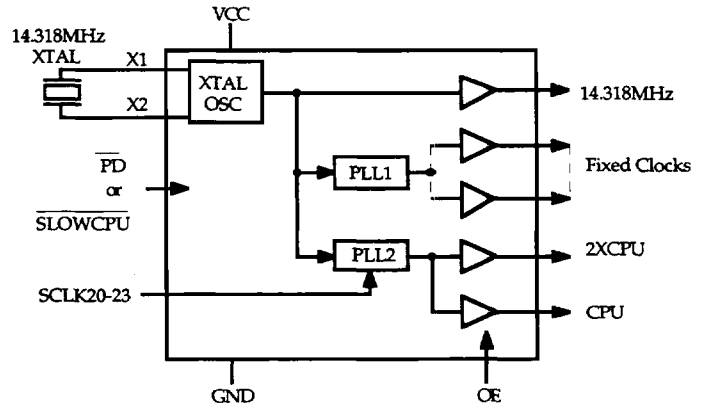
GENERAL DESCRIPTION

The W48C54A and W48C55A are low cost, general purpose clock generator ICs. The standard device options described in this document are designed for PC motherboard applications. Backward compatible with the W48C54 and W48C55, these dual-PLL clock devices incorporate an improved crystal oscillator as well as other refinements. On-chip loop filter components ensure stable operation even with the noise typical of a digital system. Device functionality, including input/output options and frequency selection is determined by a single metal mask that allows quick-turn customization capability. Both 3.3 and 5 Volt operation is supported.

The improved crystal oscillator of the W48C54A and W48C55A most notably provides improved duty cycle at the 14.318 MHz output(s). With this new design, duty cycle is not affected by varying operating conditions such as with the addition of external crystal load capacitors. Clock jitter from the 14.318 MHz output(s) is also improved, as is the crystal oscillation frequency accuracy.

Like the W48C54 and W48C55, the W48C54A and W48C55A have a unique power-on delay circuit. This feature allows compatiblility with certain microprocessor devices that cannot withstand clock input toggling until full supply voltage is reached. Upon application of power to the VCC pins, the W48C54A/55A output clocks are delayed (held low) for approximately 15 msec, after which they assume normal operation.

FUNCTIONAL BLOCK DIAGRAM : W48C54A/55A



Pentium is a trademark of Intel Corp.

FUNCTIONAL DESCRIPTION

The Functional Block Diagram shows the reference clock source can be (1) a 14.318MHz crystal connected across the X1 and X2 input pins, or (2) an input clock connected to the X1 input pin with a frequency of 14.318MHz. In the latter case, the X2 pin is left open. With either source as reference, both the W48C54A and W48C55A generate all necessary clocks at their respective frequencies to drive the CPUCLK (including 2XCPUCLK frequency), keyboard (KBCLK), local bus (BUSCLK), floppy disk (FDCLK) and communications (COMMCLK) clocks. To provide the broadest possible range of frequencies typically required for CPU mother-board designs, the target frequencies can be selected via the SCLK20-SCLK23 inputs. Consult the appropriate tables for the clock selection range. In addition, the W48C54A has one rebuffered reference clock output (14.318MHz) while the W48C55A has two. Quite often, these rebuffered reference clocks (14.318MHz) are used as the sources for the video adapter (as well as video controller designed right on the motherboard) or other function, eliminating the need for extra crystals.

Both the W48C54A and W48C55A offer smooth, glitch-free transitions when changing CPUCLK/2XCPUCLK output frequency. This feature can best be used by power management systems where it is frequently necessary to slow down the clock to conserve power. By controlling the rate of frequency transition, both devices are designed to be compatible with Intel cycle to cycle processor timing specifications. For W48C54A and W48C55A devices which have eight CPUCLK/2XCPUCLK output frequency selections (three select pins), smooth transition occurs with any new frequency selection. However, for W48C54A and W48C55A devices with sixteen CPUCLK/2XCPUCLK selections (four select pins), smooth transition occurs only when changing frequencies among the top eight table selections or among the bottom eight table selections (in other words, SCLK23 must remain low or high during frequency change). Jumping between the top and bottom eight table selections will result in a non-smooth frequency transition (this also is true with the AV9154 and AV9155).

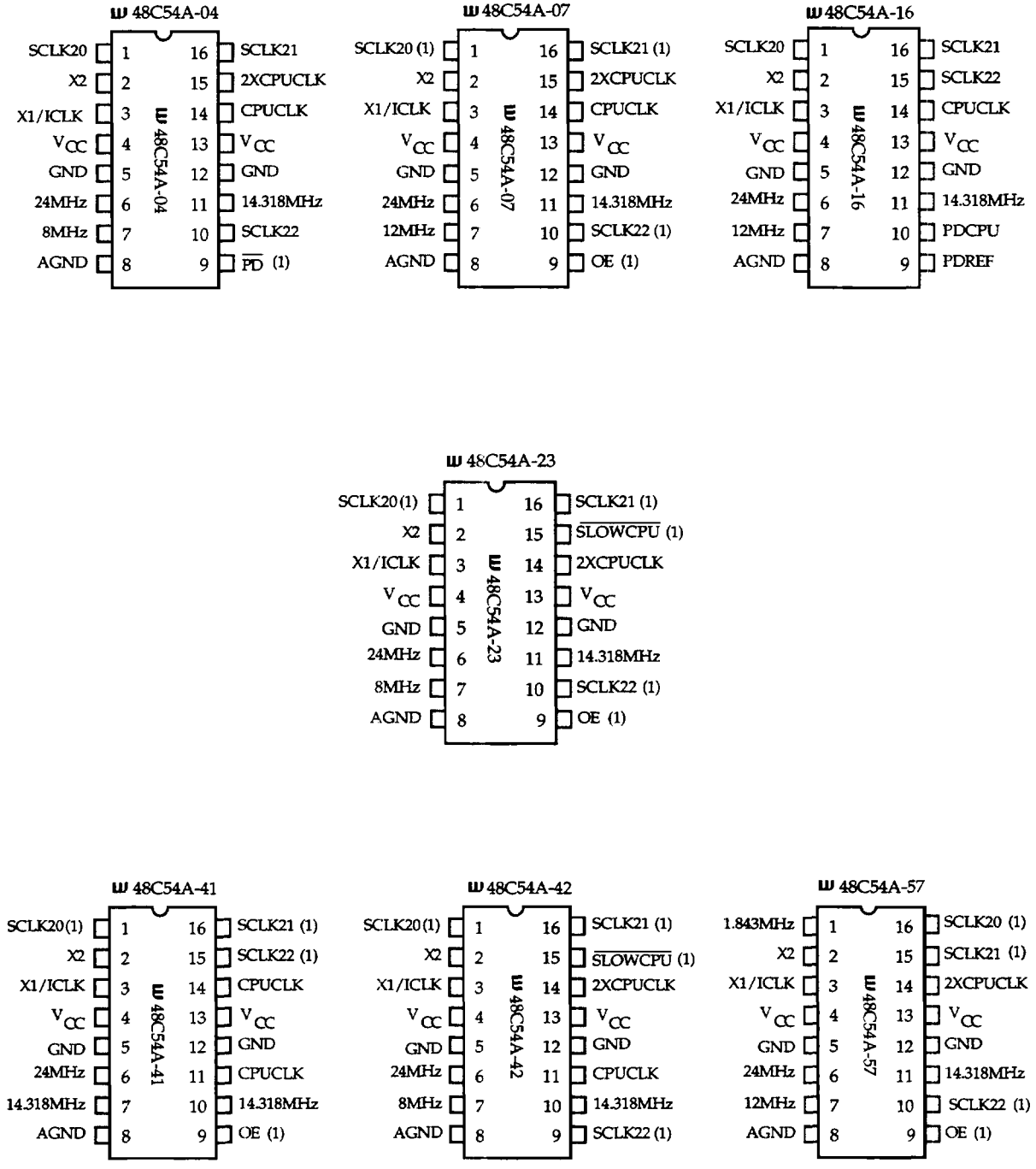
To facilitate automated board level testing, the W48C55A and some W48C54A have an active high OE (Output Enable) input pin. When pin OE is forced low, all clock outputs are tri-stated. Most logic input pins of the W48C54A and W48C55A, such as Select, OE and PD, have an internal pull-up resistor. These unused inputs can either be connected to Ground, VCC or left unconnected (an unconnected input pin implementing an internal pull-up resistor will assume a logic high state due to the pull-up resistor).

While featured in all versions of the W48C55A, power down capability is available in selected versions of the W48C54A. When PD is active (low), the device is placed in a standby mode during which power dissipation is at its minimum; all clock outputs are forced low. Similarly, complete device power down is available for W48C54A-04 and W48C54A-63. Partial power down is available for the W48C54A-16. When PDREF and PDCPU of W48C54A-16 are active (high), the reference clock (14.318MHz) and the CPUCLK will be turned off and forced low, respectively.

PIN DESCRIPTIONS: W48C54A and W48C55A

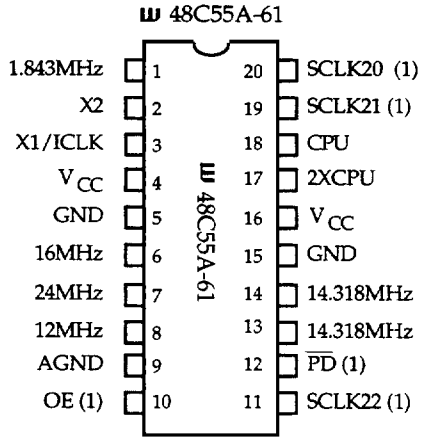
Pin Name	I/O	Description
1.843 MHz	O	Fixed 1.843MHz output for serial I/O clock application
8MHz	O	Fixed 8MHz output for keyboard clock application
12MHz	O	Fixed 12MHz output for keyboard clock application
14.318MHz	O	Fixed 14.318MHz output for various motherboard functions from 14.318MHz crystal or external clock output
15MHz	O	Fixed 15MHz output for keyboard or bus clock application
16MHz	O	Fixed 16MHz output for APIC or bus clock application
24MHz	O	Fixed 24MHz output for floppy drive or super I/O applications
32MHz	O	Fixed 32MHz output for ISA or PCI bus clock applications
40MHz	O	Fixed 40MHz output for SCSI clock applications
2XCPUCLK	O	Clock Output (refer to Frequency Selection Table)
AGND	-	Analog ground connection
CPUCLK	O	Clock Output (refer to Frequency Selection Table)
SCLK20	I	Frequency Selection input, LSB
SCLK21	I	Frequency Selection input
SCLK22	I	Frequency Selection input
SCLK23	I	Frequency Selection input, MSB
GND	-	Ground connection
OE	I	Output Enable, puts all outputs in high impedance state when low
$\overline{\text{SLOWCPU}}$	I	Slow CPU input, slows 2XCPUCLK output to 16MHz and CPUCLK output to 8MHz when low
$\overline{\text{PD}}$	I	Power Down input, puts W48C54A/55A in power down mode when low
PDCPU	I	Power Down CPU Clock circuit; when high, puts CPU PLL in power down mode and forces CPUCLK output low
PDREF	I	Power Down REF; when high, forces 14.318 MHz output low
V_{CC}	-	Power supply connection
X1/ICLK	I	Crystal connection or external clock frequency input
X2	O	Crystal connection, leave unconnected when using external clock

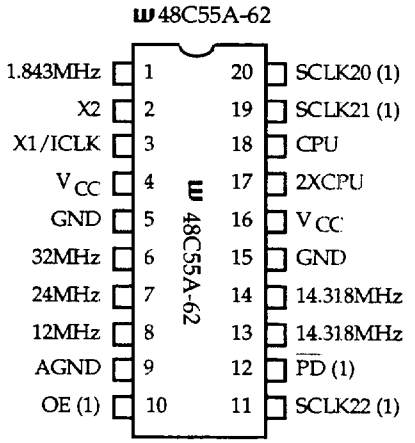
PIN CONFIGURATIONS: W48C54A-04, -07, -16, -23, -41, -42 and -57

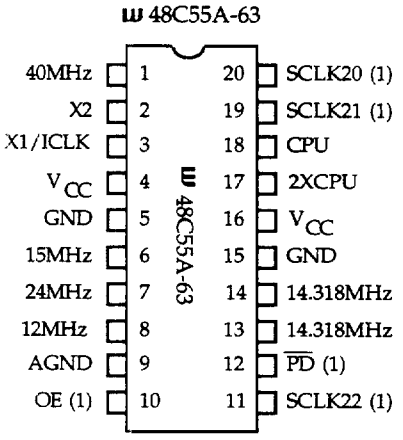


Note 1: Input pin has internal pull-up resistor.

PIN CONFIGURATIONS: W48C55A -61, -62, and -63







Note 1: Input pin has internal pull-up resistor

FREQUENCY SELECTION FOR W48C54A (using 14.318MHz input; 3.3V and 5.0V)

SCLK	-04		-07		-16	-23	-41	-42		-57
(23-20)	2XCPUCLK	CPUCLK	2XCPUCLK	CPUCLK	CPUCLK	2XCPUCLK	CPUOUT	2XCPUCLK	CPUCLK	2XCPUCLK
0	100 -(NOTE 1)-	50	100 -(NOTE 1)-	50	16	16	8	16	8	75
1	80	40	80	40	20	40	8	40	20	32
2	66.6	33.3	66.6	33.3	25	33.3	8	33.3	16.7	60
3	50	25	50	25	33.3	25	16	25	12.5	40
4	40	20	40	20	40	60	25	60	30	50
5	32	16	32	16	50	20	33.3	20	10	66.6
6	24	12	24	12	66.6	66.6	40	66.6	33.3	80
7	16	8	16	8	80	50	50	50	25	52
8	-	-	-	-	-	-	-	-	-	-
9	-	-	-	-	-	-	-	-	-	-
A	-	-	-	-	-	-	-	-	-	-
B	-	-	-	-	-	-	-	-	-	-
C	-	-	-	-	-	-	-	-	-	-
D	-	-	-	-	-	-	-	-	-	-
E	-	-	-	-	-	-	-	-	-	-
F	-	-	-	-	-	-	-	-	-	-

Note 1: Not guaranteed when Vcc < 4.5V.

PERIPHERAL CLOCKS

	-04	-07	-16	-23	-41	-42	-57
FDCLK	24	24	24	24	24	24	24
BUSCLK	-	-	-	-	-	-	-
KBCLK	8	12	12	8	-	8	12
COMMCLK	-	-	-	-	-	-	1.843
REFCLK	14.318	14.318	14.318	14.318	14.318	14.318	14.318

FREQUENCY SELECTION FOR W48C55A (using 14.318MHz input; 3.3V and 5.0V)

SCLK (23-20)	-61		-62		-63	
	2XCPU	CPU	2XCPU	CPU	2XCPU	CPU
0	8	4	8	4	8	4
1	16	8	16	8	16	8
2	32	16	32	16	60	30
3	40	20	40	20	40	20
4	50	25	50	25	50	25
5	66.66	33.33	66.66	33.33	66.66	33.33
6	80	40	80	40	80	40
7	100 -NOTE1-	50	100 -NOTE1-	50	100 -NOTE1-	50
8	-	-	-	-	-	-
9	-	-	-	-	-	-
A	-	-	-	-	-	-
B	-	-	-	-	-	-
C	-	-	-	-	-	-
D	-	-	-	-	-	-
E	-	-	-	-	-	-
F	-	-	-	-	-	-

Note 1: Not guaranteed when Vcc < 4.5V.

PERIPHERAL CLOCKS

	-61	-62	-63
FDCLK	24	24	24
BUSCLK	16	32	15
KBCLK	12	12	12
COMMCLK	1.843	1.843	40
REFCLK1	14.318	14.318	14.318
REFCLK2	14.318	14.318	14.318

ABSOLUTE MAXIMUM RATINGS (Note 1)

Parameter	Sym	Rating
V_{CC} referenced to GND		7.0V
Storage temperature	T_{STG}	-40° to +150°C
Operating temperature	T_A	0° to +70°C

Parameter	Sym	Rating
V on I/O ref to GND	-	GND-0.5V to V_{CC}+0.5V
Power dissipation	PD	0.5 Watts

Note 1: Stresses above those listed under Absolute Maximum ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the devices at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure the absolute maximum conditions for extended periods may affect devices reliability.

ELECTRICAL CHARACTERISTICS AT 5.0V

DC CHARACTERISTICS (V_{CC} = +5.0V ± 10%, T_A = 0°C to +70°C)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Input Low Voltage	V_{IL}	V_{CC} = 5V	-	-	0.8	V
Input High Voltage	V_{IH}	V_{CC} = 5V	2.0	-	-	V
Input Low Current (Note 2)	I_{IL}	V_{IN} = 0V	-	-	-100	µA
Input High Current	I_{IH}	V_{IN} = V_{CC}	-	-	10	µA
Output Low Voltage	V_{OL}	I_{OL} = 4 mA	-	-	0.4	V
Output High Voltage	V_{OH}	I_{OH} = -1 mA, V_{CC}=5V	V_{CC} -0.4V	-	-	V
Output High Voltage	V_{OH}	I_{OH} = -4 mA, V_{CC}=5V	V_{CC} -0.8V	-	-	V
Output High Voltage	V_{OH}	I_{OH} = - 8 mA	2.4	-	-	V
Supply Current (Note 3)	I_{CC}	No load	-	25	40	mA
Output Freq Change (Note 4)	F_D	Over supply and temperature	-	0.002	0.01	%
Short Circuit Current	I_{SC}	Each output clock	25	40	-	mA
Supply Current, Pwr Dwn(Note 5)	I_{CCSTBY}		-	30	-	µA
Input Capacitance	C_{IN}	Except X1, X2	-	-	10	pF
Load Capacitance	C_L	Pins X1, X2	-	20	-	pF
Pull-Up Resistor Value	R_P	Except X1, X2	-	250		kΩ

Note 2: Includes pull-up resistor.
Note 3: No output load capacitance, CPUCLK or 2XCPUCLK running at 50MHz. Power supply current can change with different mask configuration.
Note 4: Consideration of reference crystal shift only.
Note 5: With full chip power down pin low.

ELECTRICAL CHARACTERISTICS AT 5.0V(cont.)

AC CHARACTERISTICS (V_{CC} = +5.0V± 10%, T_A = 0°C to +70°C)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Input Clock Rise Time	T_{ICR}		-	-	20	ns
Input Clock Fall Time	T_{ICF}		-	-	20	ns
Output Rise Time, 0.8 to 2.0V	T_R	25 pf load	-	1	2	ns
Rise Time, 20% to 80% V_{CC}	T_R	25 pf load	-	2	4	ns
Output Fall Time, 2.0 to 0.8V	T_F	25 pf load	-	1	2	ns
Fall Time, 80% to 20% V_{CC}	T_F	25 pf load	-	2	4	ns
Duty Cycle, All Outputs	D_T	25 pf load	40/60	50/50	60/40	%
Jitter, 1 Sigma	T_{J1S}	As compared	-	0.8	2.5	%
Jitter, Absolute	T_{JAB}	With clock period	-	2	5	%
Jitter, Absolute	T_{JAB}	16-100 MHz clocks	-	-	700	ps
Input Frequency	F_I		-	14.318	-	MHz
Clock Skew Between CPU and 2XCPU Outputs	T_{SK}		-		1.0	ns
Frequency Transition Time	T_{FT}	From 8-100 MHz	-	40	50	ms

NOTES

ELECTRICAL CHARACTERISTICS AT 3.3V

DC CHARACTERISTICS (V_{CC} = +3.3V ± 10%, T_A = 0°C to +70°C)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Input Low Voltage	V_{IL}	V_{CC} = 3.3V	-	-	0.15Vcc	V
Input High Voltage	V_{IH}	V_{CC} = 3.3V	0.7Vcc	-	-	V
Input Low Current (Note 2)	I_{IL}	V_{IN} = 0V	-	-	-100	µA
Input High Current	I_{IH}	V_{IN} = V_{CC}	-	-	10	µA
Output Low Voltage	V_{OL}	I_{OL} = 4 mA	-	-	0.4	V
Output High Voltage	V_{OH}	I_{OH} = -4 mA, V_{CC}=3.3V	2.4	-	-	V
Supply Current (Note 3)	I_{CC}	No load	-	20	35	mA
Output Freq Change (Note 4)	F_D	Over supply and temperature	-	0.002	0.01	%
Short Circuit Current	I_{SC}	Each output clock	25	40	-	mA
Supply Current, Pwr Dwn (Note 5)	I_{CCSTBY}		-	25	-	µA
Input Capacitance	C_{IN}	Except X1, X2	-	-	10	pF
Load Capacitance	C_L	Pins X1, X2	-	20	-	pF
Pull-Up Resistor Value	R_P	Except X1, X2	-	250		kΩ

Note 2: Includes pull-up resistor.
Note 3: No output load capacitance, CPUCLK or 2XCPUCLK running at 50MHz. Power supply current can change with different mask configuration.
Note 4: Consideration of reference crystal shift only.
Note 5: With full chip power down pin low.

ELECTRICAL CHARACTERISTICS AT 3.3V (cont.)

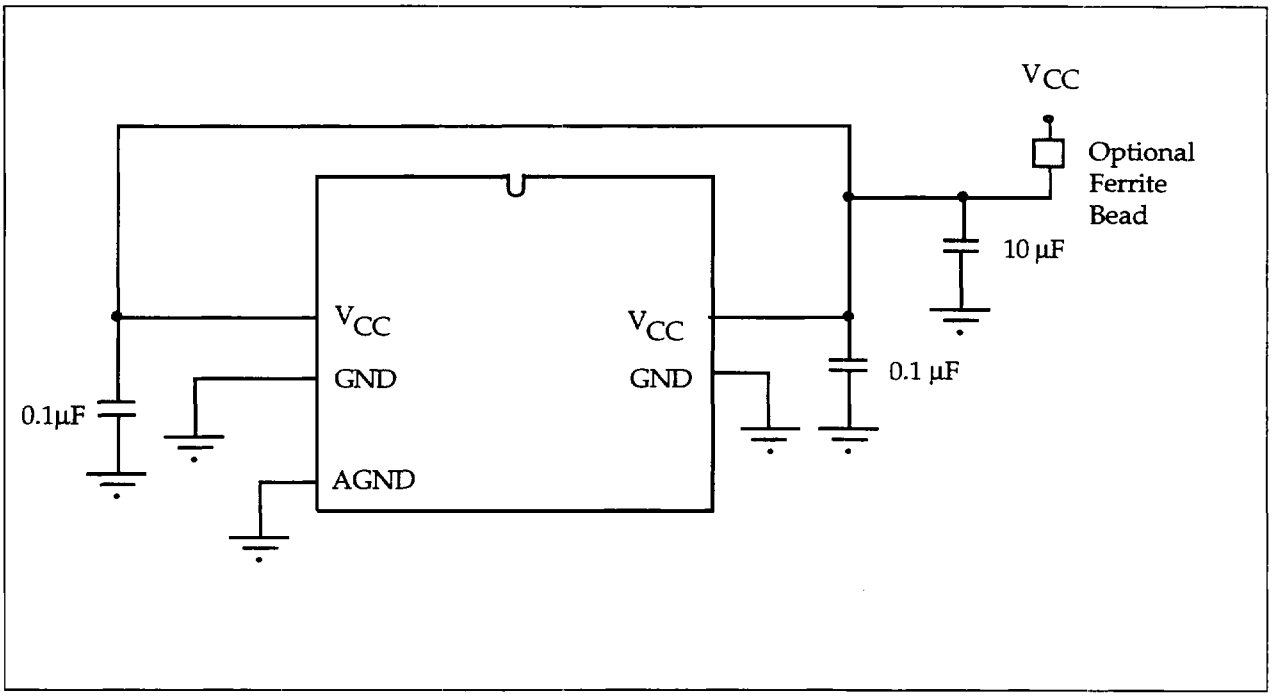
AC CHARACTERISTICS (V_{CC} = +3.3V± 10%, T_A = 0°C to +70°C)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Input Clock Rise Time	T_{ICR}		-	-	20	ns
Input Clock Fall Time	T_{ICF}		-	-	20	ns
Rise Time, 20% to 80% V_{CC}	T_R	15 pf load	-	2	4	ns
Fall Time, 80% to 20% V_{CC}	T_F	15 pf load	-	2	4	ns
Duty Cycle, All Outputs	D_T	15 pf load	40/60	50/50	60/40	%
Jitter, 1 Sigma	T_{J1S}	As compared	-	0.8	2.5	%
Jitter, Absolute	T_{JAB}	with clock period	-	2	5	%
Jitter, Absolute	T_{JAB}	16-80 MHz clocks	-	-	700	ps
Input Frequency	F_I		-	14.318	-	MHz
Clock Skew Between CPU and 2XCPU Outputs	T_{SK}		-		1.0	ns
Frequency Transition Time	T_{FT}	From 8-100 MHz	-	40	50	ms

CROSS REFERENCE LIST: ω48C54A/55A

IC WORKS Device	Compatible Device
ω48C54A-04	AV9154-04
ω48C54A-07	AV9154-26
ω48C54A-16	AV9154-16
ω48C54A-42	AV9154-42
ω48C54A-57	AV9154-27
ω48C55A-61	AV9155-01
ω48C55A-62	AV9155-02
ω48C55A-63	AV9155-36

RECOMMENDED CIRCUIT CONFIGURATION

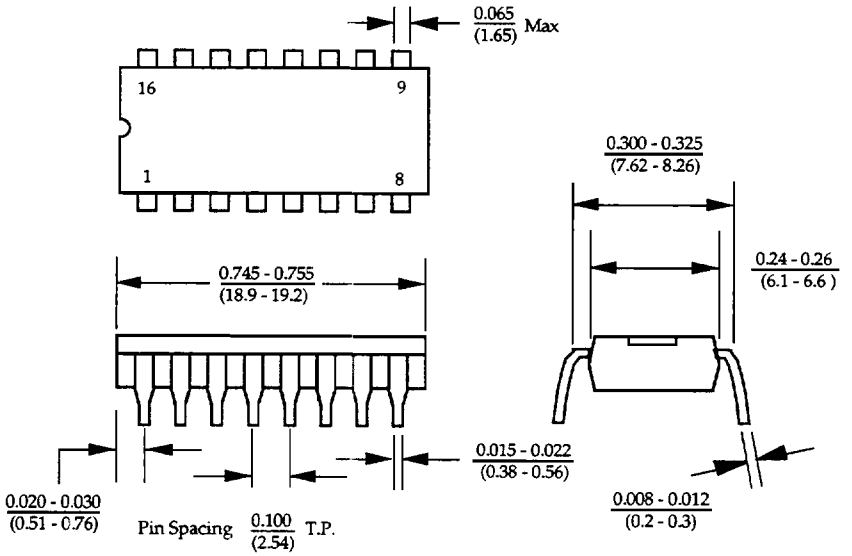


RECOMMENDED BOARD LAYOUT: ICW48C54A/55A

For optimum performance in system applications the above power supply decoupling scheme should be used. All GND pins are connected directly to the ground plane.

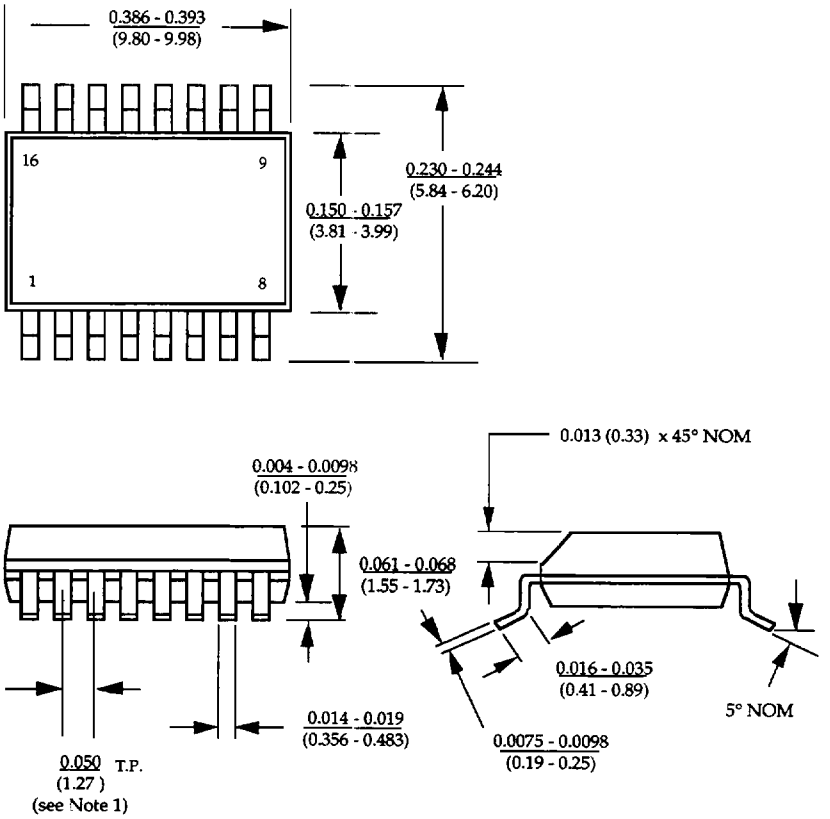
VCC decoupling is important to both reduce phase jitter and EMI radiation. The 0.1µf decoupling capacitors should be placed as close to the VCC pins as possible, otherwise the increased trace inductance will negate its decoupling capability. The 10µf decoupling capacitor shown should be a tantalum type. For further EMI protection, the VCC connection can be made via a ferrite bead, as shown above.

Figure 2 : 16 pin Plastic Dual In-Line Package



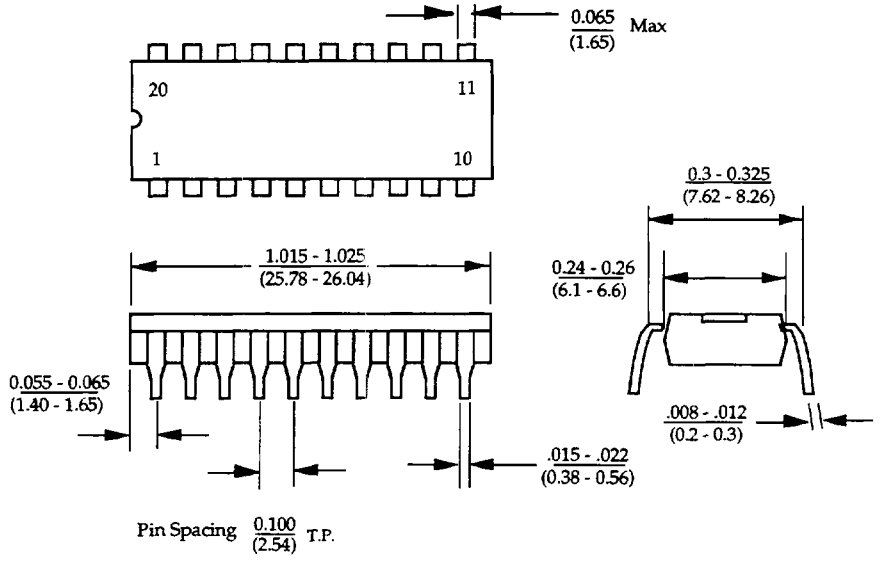
Note: All linear dimensions are in inches and parenthetically in millimeters, min - max.

Figure 3: 16 lead Plastic Small Outline Package



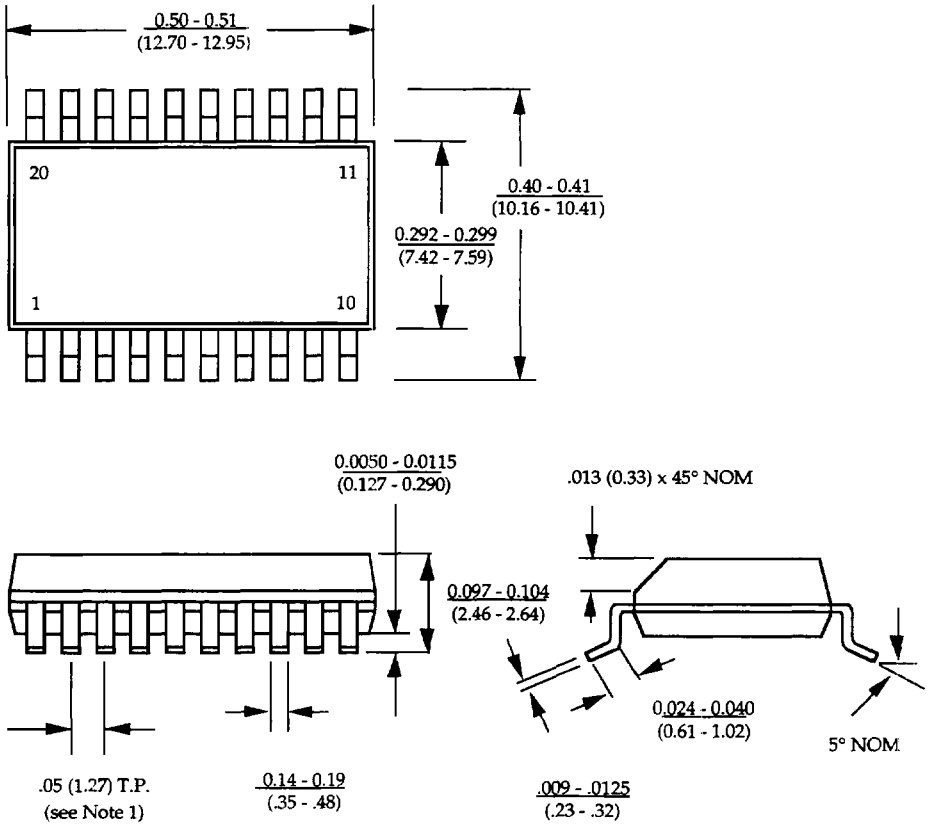
Note 1: Leads are within 0.010 (0.25) radius of true position at maximum material condition.
Note 2: All linear dimensions are in inches and parenthetically in millimeters, min - max.

Figure 4: 20 pin Plastic Dual In-Line Package



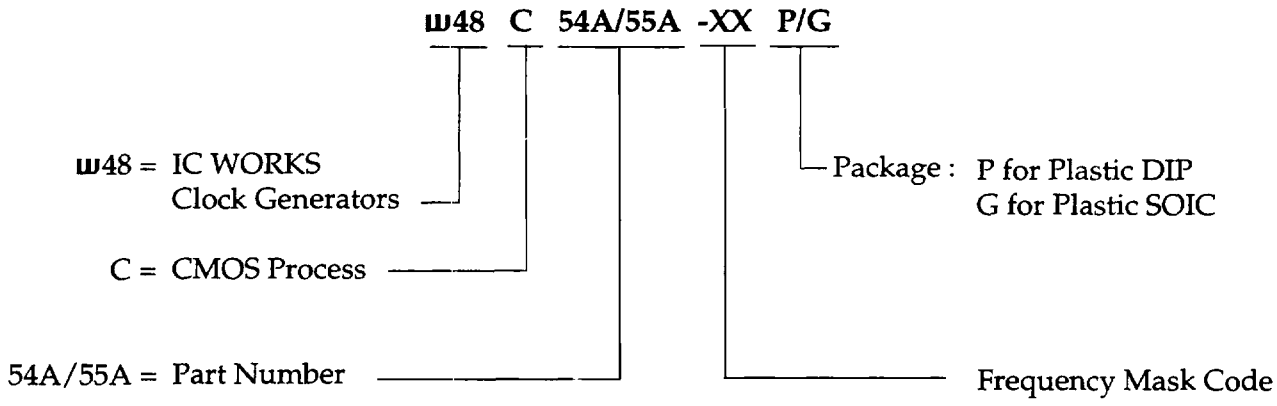
Note: All linear dimensions are in inches and parenthetically in millimeters, min - max.

Figure 5: 20 lead Plastic Small Outline Package



Note 1: Leads are within 0.010 (0.25) radius of true position at maximum material condition.
Note 2: All linear dimensions are in inches and parenthetically in millimeters, min - max.

ORDERING INFORMATION



VALID PART NUMBERS

ω48C54A-04 ω48C54A-07 ω48C54A-16 ω48C54A-23 ω48C54A-41 ω48C54A-42 ω48C54A-57

ω48C55A-61 ω48C55A-62 ω48C55A-63

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