DATA SHEET

PCF8890

240 + 1 outputs TFT LCD gate driver

Objective specification

2003 Feb 25

Philips
Semiconductors

PHILIPS

CONTENTS

240 + 1 outputs TFT LCD gate driver PCF8890

1 FEATURES

- Low power TFT LCD gate driver and DC/DC controller
- 240 + 1 outputs
- Programmable number of active outputs from 1 to 240 + 1
- 4-level gate driving, 4-level HAPD (Philips) driving scheme (1 high and 3 low levels) and additional V_{SS} step for power reduction
- On-chip DC/DC controller
- High output voltage range: V_{VH} = +20 V (maximum programmed indirectly via V1 settings) and V_{EE} = −20 V (minimum)
- Row inversion with pre-pulse
- Operating frequency: up to 100 kHz
- Automatic reset for shift register by frame start
- Supports line and frame inversion for gate coupled driving
- Low power consumption optimized for battery operation
- Slim chip layout for COG, TCP and COF applications
- Compatible with PCF8880 source driver.

2 APPLICATION

The chip set PCF8890 and PCF8880 is optimized for low power colour TFT LCDs in portable applications such as cellular phones, PDAs and MP3 players, instrumentation, automotive informations system, etc. The gate driver can be used for small to medium sized panels with up to 240 lines (e.g. 1/4 VGA) and maximal 300 pF load per line.

3 GENERAL DESCRIPTION

PCF8890 is a high-voltage CMOS IC designed to drive 240 + 1 gate lines of a TFT LCD with an output voltage up to 40 V. The device includes:

- A 241-bit shift register with high-voltage output stages
- A switch matrix with 5 output levels (for 4-level driving scheme plus V_{SS})
- An automatic reset by pin FRAMESTART
- A DC/DC controller and regulator
- A voltage generator for all output levels of the gate driver and for the companion source driver (PCF8880).

The device is manufactured in a high-voltage n-well CMOS technology.

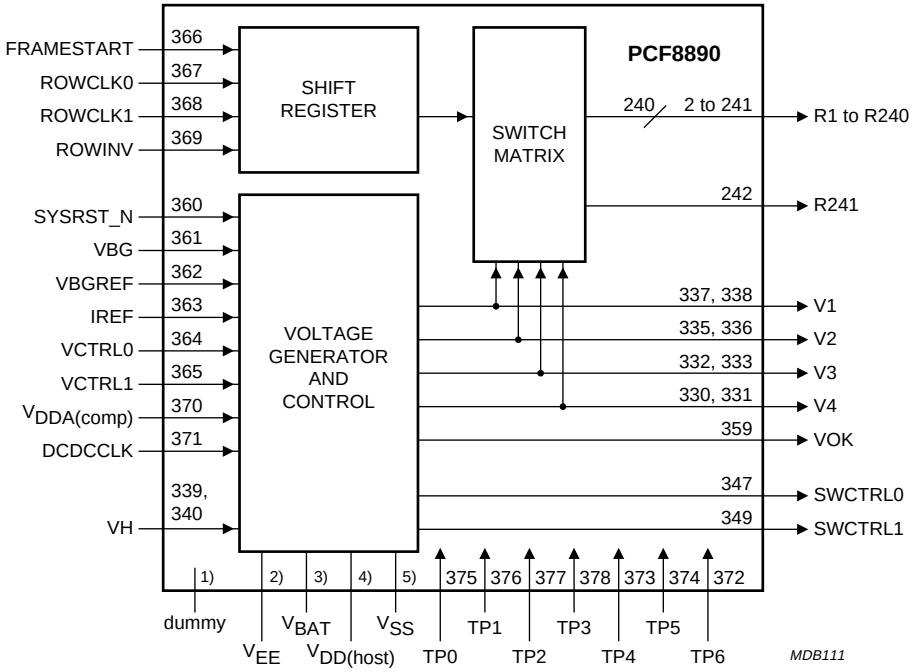
The PCF8890 is completely controlled by the PCF8880. No interface to external controller systems is required.

The gate driver is tailored to panels which operate with a patented gate coupled driving. On the panel, the storage capacitor must be connected to the next row. Thus, an extra row line is required to invert the last line of the display.

4 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCF8890U	–	chip assembly on the glass module	–
	–	chip assembly on foil (tbf)	–

5 BLOCK DIAGRAM



(1) dummy = 1, 243, 247 to 325, 345, 346, 350, 351, 380 and 381.
(2) V_{EE} = 246, 327 to 329 and 382.
(3) V_{BAT} = 244, 342 to 344 and 384.
(4) $V_{DD(host)}$ = 356 to 358.
(5) V_{SS} = 245, 326, 334, 341, 348, 352 to 355, 379 and 383.

Fig.1 Block diagram.

6 PINNING

SYMBOL	PAD	TYPE[1]	DESCRIPTION
dummy	1, 243, 247 to 325, 345, 346, 350, 351, 380, 381	–	
R1 to R240	2 to 241	O	row output 1 to 240; 4-level high-voltage output to the TFT gate and storage capacitor; not connected if display with less than 240 lines is used
R241	242	O	row output 241; 3-level high-voltage pre-pulse output to the storage capacitor; not connected if display with less than 241 lines is used
V_{BAT}	244, 342 to 344, 384	S	battery supply voltage; input for DC/DC converter and power supply; connect to battery
V_{SS}	245, 326, 334, 341, 348, 352 to 355, 379, 383	S	logic ground
V_{EE}	246, 327 to 329, 382	S	chip bulk; generated chip bulk voltage (used for external capacitor)
V4	330 to 331	S	gate low pre-pulse level output; not used and not connected (only used for testing)
V3	332 to 333	S	gate low-level voltage output; not used and not connected (only used for testing)
V2	335 to 336	S	gate high pre-pulse level output; not used and not connected (only used for testing)
V1	337 to 338	S	regulated high-level voltage output; (used for external capacitor)
VH	339 to 340	S	generated high-level voltage; (used for external capacitor)
SWCTRL0	347	O	switching control 0 output; controls the external switches of the DC/DC converter
SWCTRL1	349	O	switching control 1 output; controls the external switches of the DC/DC converter
$V_{DD(host)}$	356 to 358	S	logic power supply voltage; power supply for digital circuitry
VOK	359	O	generated voltages status output; used for start up of voltage generator; connect to VOK input of PCF8880
SYSRST_N	360	I	system reset input; if SYSRST_N = LOW the shift register is cleared and all analog blocks are switched off (no high-voltage available); connect to SYSRST_N output of PCF8880
VBG	361	I	band gap voltage input (1.22 V); connect to VBG output of PCF8880
VBGREF	362	I	band gap reference voltage input; high-ohmic reference voltage for band gap (0 V); connect to VBGREF output of PCF8880
IREF	363	I	2.2 μA current source for analog blocks input; connect to IREF output of PCF8880
VCTRL0	364	I	voltage control 0 input; serial data link from the source driver for programming of the output levels; connect to VCTRL0 output of PCF8880

SYMBOL	PAD	TYPE(1)	DESCRIPTION
VCTRL1	365	I	voltage control 1 input; serial data link from the source driver for programming of the output levels; connect to VCTRL1 output of PCF8880
FRAMESTART	366	I	shift register for gate signals input; connect to FRAMESTART output of PCF8880
ROWCLK0	367	I	shift register clock 0 input; the shift register data is shifted on the rising edge of ROWCLK0; connect to ROWCLK0 output of PCF8880
ROWCLK1	368	I	shift register clock 1 input; connect to ROWCLK1 output of PCF8880
ROWINV	369	I	pre-pulse polarity control input; if ROWINV = HIGH, the pre-pulse is positive (V2), if ROWINV = LOW, the pre-pulse is negative (V4); connect to ROWINV output of PCF8880
$V_{DDA(comp)}$	370	I	V_{DDA} comparator input; this signal is used for voltage generation; connect to $V_{DDA(comp)}$ output of PCF8880
DCDCCLK	371	I	DC/DC converter chopping clock input; connect to DCDCCLK output of PCF8880
TP6	372	I	test pin 6: connect to V_{SS} (used for testing)
TP5	373	I	test pin 5: connect to V_{SS} (used for testing)
TP4	374	I	test pin 4: connect to V_{SS} (used for testing)
TP3	375	I	test pin 3: connect to V_{SS} (used for testing)
TP2	376	I	test pin 2: connect to V_{SS} (used for testing)
TP1	377	I	test pin 1: connect to V_{SS} (used for testing)
TP0	378	I	test pin 0: connect to V_{SS} (used for testing)

Note

1. S = supply, O = output and I = input

7 FUNCTIONAL DESCRIPTION

7.1 Power-up sequence

When powering up the device, a certain sequence of switching-on of the different supply voltages has to be followed (tbf).

7.2 Shift register

The shift register is controlled by the shift clock ROWCLK0.

On the rising edge of ROWCLK0, the data is shifted from R1 to R241.

7.3 I/O signal voltage levels

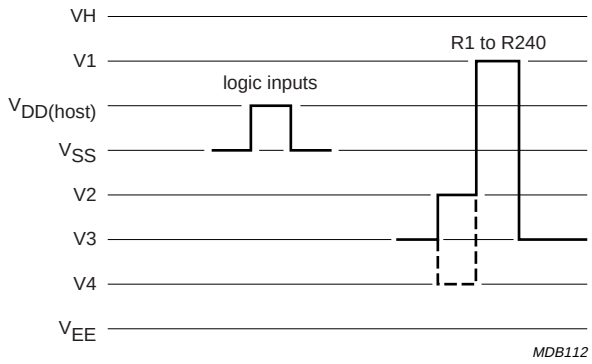


Fig.2 I/O signal voltage levels.

7.4 Pulse micro timing

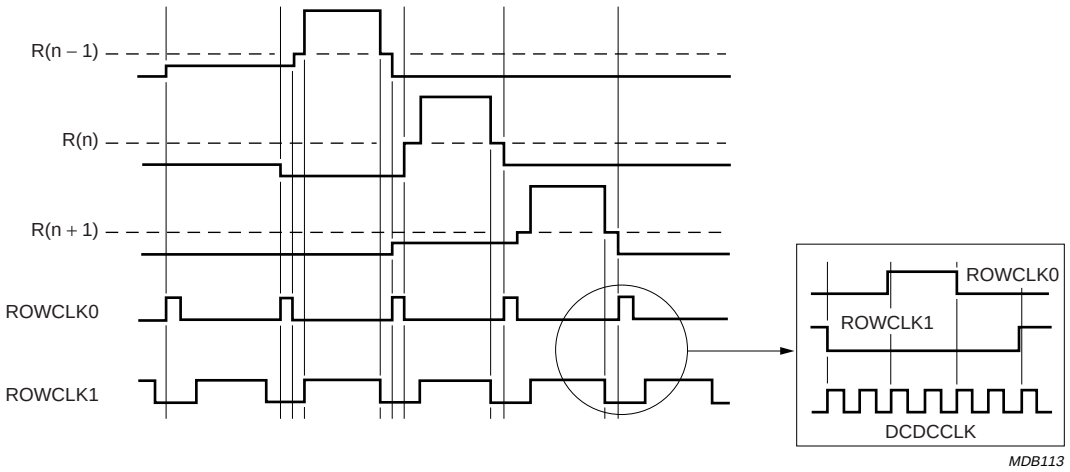


Fig.3 Pulse micro timing.

7.5 Waveforms

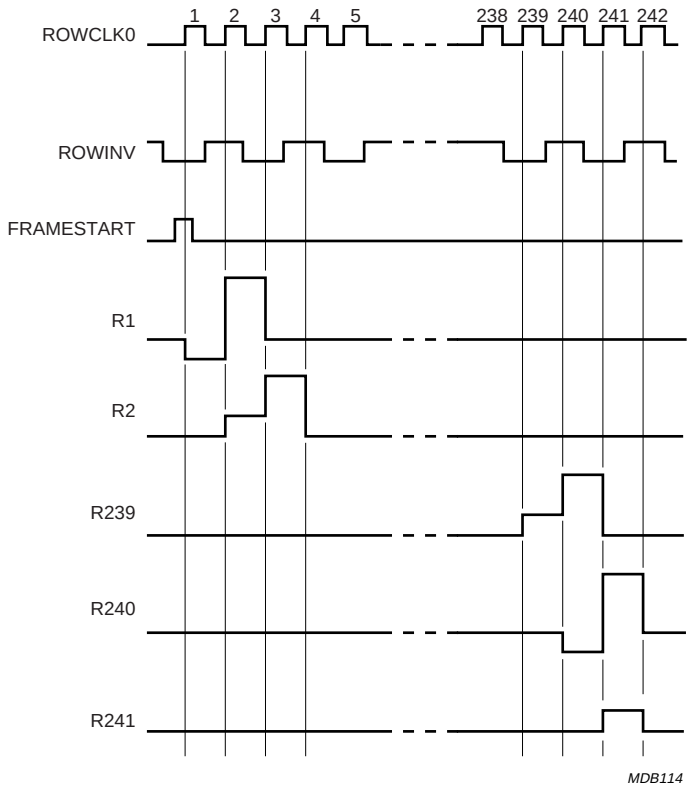


Fig.4 Shift operation.

8 PROGRAMMING

Table 1 Row driver voltage programming; $V1_{max}$ limited by V_{EE} and V_{BAT} ($V1 = V_{BAT} + V_{EE}$); V4 steps are the same as V3 step.

V3 PROG	V3 (V)	V1 (V)			V2 (V)			V4 (V)		V_{EE} (V)
		MIN.	MAX.	STEP	MIN.	MAX.	STEP	MIN.	MAX.	
11111	–8.057	11.25	18.750	0.5	–2.510	–6.494	–0.032	13.604	–17.588	–19.142
11110	–8.057	11.25	18.750	0.5	–2.510	–6.494	–0.031	13.604	–17.588	–19.142
11101	–7.910	11.25	18.750	0.5	–2.464	–6.375	–0.031	13.356	–17.268	–18.793
11100	–7.769	11.25	18.750	0.5	–2.420	–6.261	–0.030	13.118	–16.959	–18.457
11011	–7.633	11.25	18.750	0.5	–2.377	–6.151	–0.030	12.887	–16.661	–18.133
11010	–7.501	11.25	18.750	0.5	–2.336	–6.045	–0.029	12.665	–16.374	–17.820
11001	–7.374	11.25	18.750	0.5	–2.297	–5.943	–0.029	12.450	–16.096	–17.518
11000	–7.251	11.25	18.750	0.5	–2.258	–5.844	–0.028	12.242	–15.827	–17.225
10111	–7.132	11.25	18.750	0.5	–2.221	–5.748	–0.028	12.041	–15.568	–16.943
10110	–7.016	11.25	18.750	0.5	–2.185	–5.655	–0.027	11.847	–15.316	–16.669
10101	–6.905	11.25	18.750	0.5	–2.151	–5.565	–0.027	11.659	–15.073	–16.404
10100	–6.797	11.25	18.750	0.5	–2.117	–5.478	–0.026	11.476	–14.837	–16.148
10011	–6.692	11.25	18.599	0.5	–2.084	–5.394	–0.026	11.300	–14.609	–15.899
10010	–6.591	11.25	18.358	0.5	–2.053	–5.312	–0.026	11.128	–14.387	–15.658
10001	–6.492	11.25	18.124	0.5	–2.022	–5.232	–0.025	10.962	–14.172	–15.424
10000	–6.397	11.25	17.897	0.5	–1.992	–5.155	–0.025	10.801	–13.964	–15.197
01111	–6.304	11.25	17.676	0.5	–1.964	–5.081	–0.025	10.644	–13.761	–14.976
01110	–6.214	11.25	17.462	0.5	–1.935	–5.008	–0.024	10.492	–13.564	–14.762
01101	–6.126	11.25	17.254	0.5	–1.908	–4.937	–0.024	10.344	–13.373	–14.554
01100	–6.041	11.25	17.052	0.5	–1.882	–4.869	–0.024	10.200	–13.187	–14.352
01011	–5.958	11.25	16.855	0.5	–1.856	–4.802	–0.023	10.060	–13.006	–14.155
01010	–5.878	11.25	16.664	0.5	–1.831	–4.737	–0.023	9.924	–12.830	–13.964
01001	–5.799	11.25	16.477	0.5	–1.806	–4.674	–0.023	9.792	–12.659	–13.777
01000	–5.723	11.25	16.296	0.5	–1.783	–4.612	–0.022	9.663	–12.492	–13.596
00111	–5.648	11.25	16.119	0.5	–1.759	–4.552	–0.022	9.537	–12.330	–13.419
00110	–5.576	11.25	15.947	0.5	–1.737	–4.494	–0.022	9.415	–12.172	–13.247
00101	–5.505	11.25	15.779	0.5	–1.715	–4.437	–0.021	9.295	–12.018	–13.079
00100	–5.436	11.25	15.616	0.5	–1.693	–4.381	–0.021	9.179	–11.867	–12.916
00011	–5.369	11.25	15.456	0.5	–1.672	–4.327	–0.021	9.066	–11.721	–12.756
00010	–5.304	11.25	15.300	0.5	–1.652	–4.274	–0.021	8.955	–11.578	–12.600
00001	–5.240	11.25	15.148	0.5	–1.632	–4.223	–0.020	8.847	–11.438	–12.448
00000	–5.177	11.25	15.000	0.5	–1.613	–4.173	–0.020	8.742	–11.302	–12.300

9 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134); see notes 1 and 2; all values with respect to V_{SS} = 0 V.

SYMBOL	PARAMETER	CONDITION	MIN.	MAX.	UNIT
V_{BAT}	battery supply voltage		V_{SS} – 0.3	V_{SS} + 7.0	V
V_{SS}	interface ground voltage		V_{EE} – 0.3	V_{EE} + 10	V
$V_{DD(host)}$	interface high-voltage supply voltage		V_{SS} – 0.3	V_{SS} + 7.0	V
V_{EE}	bulk voltage		V_{VH} – 45	V_{VH} + 0.3	V
V_{VH}	not regulated high-voltage		V_{EE} – 0.3	V_{EE} + 45	V
V_{VBGREF}	band gap reference voltage		V_{SS} – 0.3	$V_{DD(host)}$ + 0.3	V
V_{V1}	drive 1 voltage		V_{EE} – 0.3	V_{EE} + 45	V
V_{V2}	drive 2 voltage		V_{EE} – 0.3	V_{EE} + 45	V
V_{V3}	drive 3 voltage		V_{EE} – 0.3	V_{EE} + 45	V
V_{V4}	drive 4 voltage		V_{EE} – 0.3	V_{EE} + 45	V
V_I	voltage on all digital input pins		V_{SS} – 0.3	$V_{DD(host)}$ + 0.3	V
V_O	voltage on all digital output pins		V_{SS} – 0.3	$V_{DD(host)}$ + 0.3	V
V_{SWCTRL}	voltage on all switch control pins		V_{SS} – 0.3	V_{BAT} + 0.3	V
$V_{R(x)}$	voltage on all row pins		V_{SS} – 0.3	V_{BAT} + 0.3	V
T_{oper}	operating temperature		–40	+85	°C
T_{stg}	storage temperature	note 3	–55	+125	°C

Notes

1. Stresses above those listed under limiting values may cause permanent damage to the device.
2. Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to V_{SS} unless otherwise noted.
3. The storage temperature specifies the temperature range within which the chip will not be damaged when it is not powered.

10 HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is recommended to take standard precautions appropriate for handling MOS devices (see *"Handling MOS Devices"*).

11 DC CHARACTERISTICS

$V_{DD(host)}$ = 1.8 V; V_{BAT} = 2.7 to 4.5 V; V_{SS} = 0 V; T_{amb} = –40 to +85 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{BAT}	battery supply voltage		2.7	–	4.5	V
$V_{DD(host)}$	interface high-voltage supply voltage		1.8	–	3.6	V
V_{VH}	not regulated high-voltage	$V_{BAT} - V_{EE}$	tbf	V_{BAT} + 18	tbf	V
V_{EE}	bulk voltage		tbf	–18.5	tbf	V
I_{BAT}	battery supply current	$V_{DD(host)}$ = 2.7 V; f_{osc} = 625 kHz; V_{V1} = 15 V; V_{V2} = –4 V; V_{V2} = –12 V; V_{EE} = 20 V	–	–	tbf	µA
$I_{BAT(idle)}$	idle battery supply current	$V_{DD(host)}$ = 2.7 V; f_{osc} = 0; $V_{V1} = V_{V2} = V_{V4}$ = 0 V_{EE} = 0	–	–	tbf	µA
$I_{DD(host)}$	interface high-voltage supply current	$V_{DD(host)}$ = 2.7 V; f_{osc} = 625 kHz	–	–	tbf	µA
$I_{DD(idle)}$	idle interface high-voltage supply current	$V_{DD(host)}$ = 2.7 V; f_{osc} = 0;	–	–	tbf	µA
Driver outputs; pins V1, V2, V3 and V4						
V_{V1}	drive 1 voltage	16 steps of 0.5 V	11.25	–	18.75	V
V_{V2}	drive 2 voltage	128 steps of 30 mV	–6	–	–2.5	V
V_{V3}	drive 3 voltage		tbf	–8	tbf	V
V_{V4}	drive 4 voltage	128 steps of 30 mV	–17	–	–13.5	V
R_{V1}	drive 1 resistance		–	tbf	1000	Ω
R_{V2}	drive 2 resistance		–	tbf	1000	Ω
R_{V3}	drive 3 resistance		–	tbf	1000	Ω
R_{V4}	drive 4 resistance		–	tbf	1000	Ω
$C_{o(L)}$	output load capacitance		–	150	300	pF
Generated voltages status; pin VOK						
V_{OH}	HIGH-level output voltage		$0.8V_{DD(host)}$	–	$V_{DD(host)}$	V
V_{OL}	LOW-level output voltage		V_{SS}	–	$0.2V_{DD(host)}$	V
I_O	output current		–	–	100	µA
DC/DC converter switch control outputs; pins SWCTRL0 and SWCTRL1						
V_{OH}	HIGH-level output voltage		tbf	–	tbf	V
V_{OL}	LOW-level output voltage		tbf	–	tbf	V
I_O	output current		–	–	tbf	µA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
All input pins						
V_{IH}	HIGH-level input voltage		$0.8V_{DD(host)}$	–	$V_{DD(host)}$	V
V_{IL}	LOW-level input voltage		V_{SS}	–	$0.2V_{DD(host)}$	V
I_{LI}	input leakage current		–5	–	+5	µA

12 AC CHARACTERISTICS

V_{BAT} = 3.6 V; V_{SS} = 0 V; $V_{DD(host)}$ = 1.8 V; VGON = 19 V; VGOFF = –8 V; T_{amb} = –40 to +85 °C; see Fig.5.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Shift register clocks; pins ROWCLK0 and ROWCLK1						
$T_{cy(ROWCLK0)}$	row clock0 cycle time		tbf	64	–	µs
$t_{ROWCLK0(H)}$	row clock0 HIGH time		tbf	3	–	µs
$t_{ROWCLK0(L)}$	row clock0 LOW time		tbf	61	–	µs
$T_{cy(ROWCLK1)}$	row clock1 cycle time		tbf	64	–	µs
$t_{ROWCLK1[H]}$	row clock1 HIGH time		tbf	55	–	µs
$t_{ROWCLK1[L]}$	row clock1 LOW time		tbf	9	–	µs
Shift register for gate signals; pin FRAMESTART						
t_{su}	data set-up time		tbf	–	–	ns
t_h	data hold time		tbf	–	–	ns
Row outputs; pins R1 to R241						
t_d	ROWCLK delay	C_L = 300 pF	–	–	–	ns

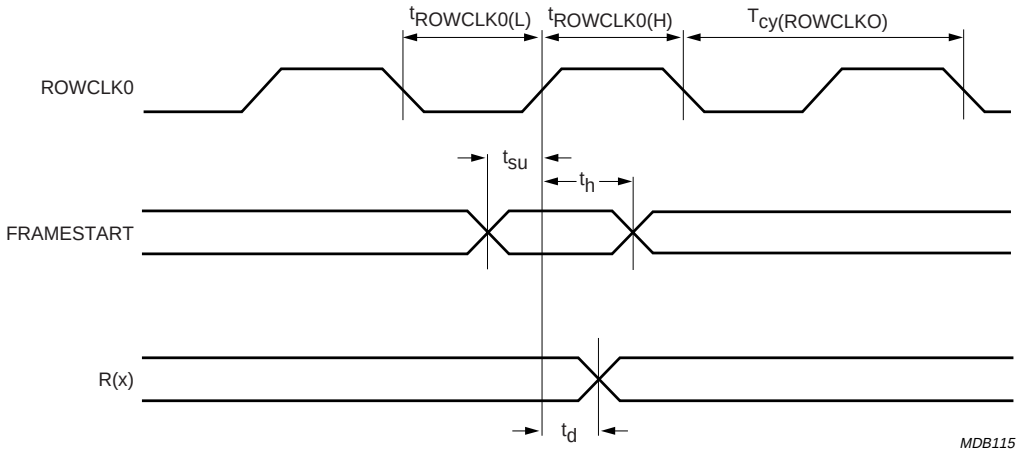
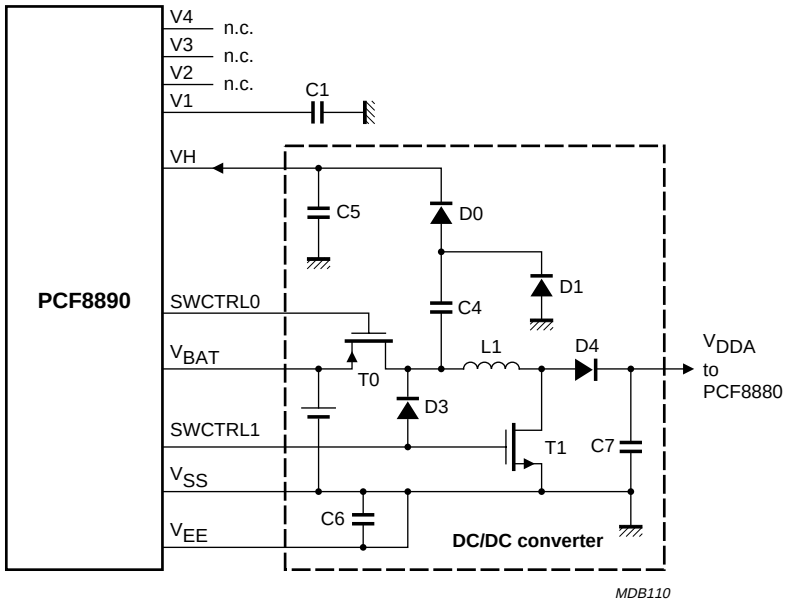


Fig.5 Timing waveforms.

13 APPLICATION INFORMATION



C1 = 50 nF.
C4 = 33 nF.
C5 and C6 = 330 nF.
C7 = 3.3 µF.
D0 to D3 = normal diode; breakthrough voltage >20 V.
D4 = Schottky diode; breakthrough voltage >6 V.
T0 = BSS84 (pMOS VT < 2 V; R_{on} < 10 Ω; V_{ds} > 50 V).
T1 = BSH103 (nMOS VT > −1 V; R_{on} < 5 Ω; V_{ds} > 30 V).
L1 = 150 µH; R < 5 Ω; rated current >180 mA (i.e. coil craft LPO1704-15).

Fig.6 Proposal for components.

14 OPEN SHORT DIAGRAMS

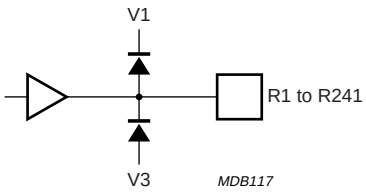


Fig.7 Row driver outputs.

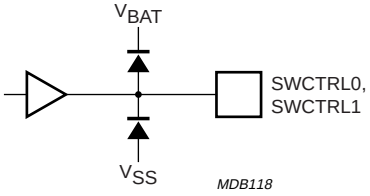


Fig.8 Switching control outputs.

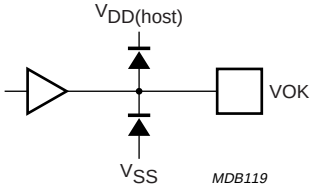


Fig.9 Voltage status output.

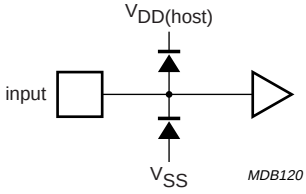


Fig.10 Inputs.

15 BONDING PAD INFORMATION

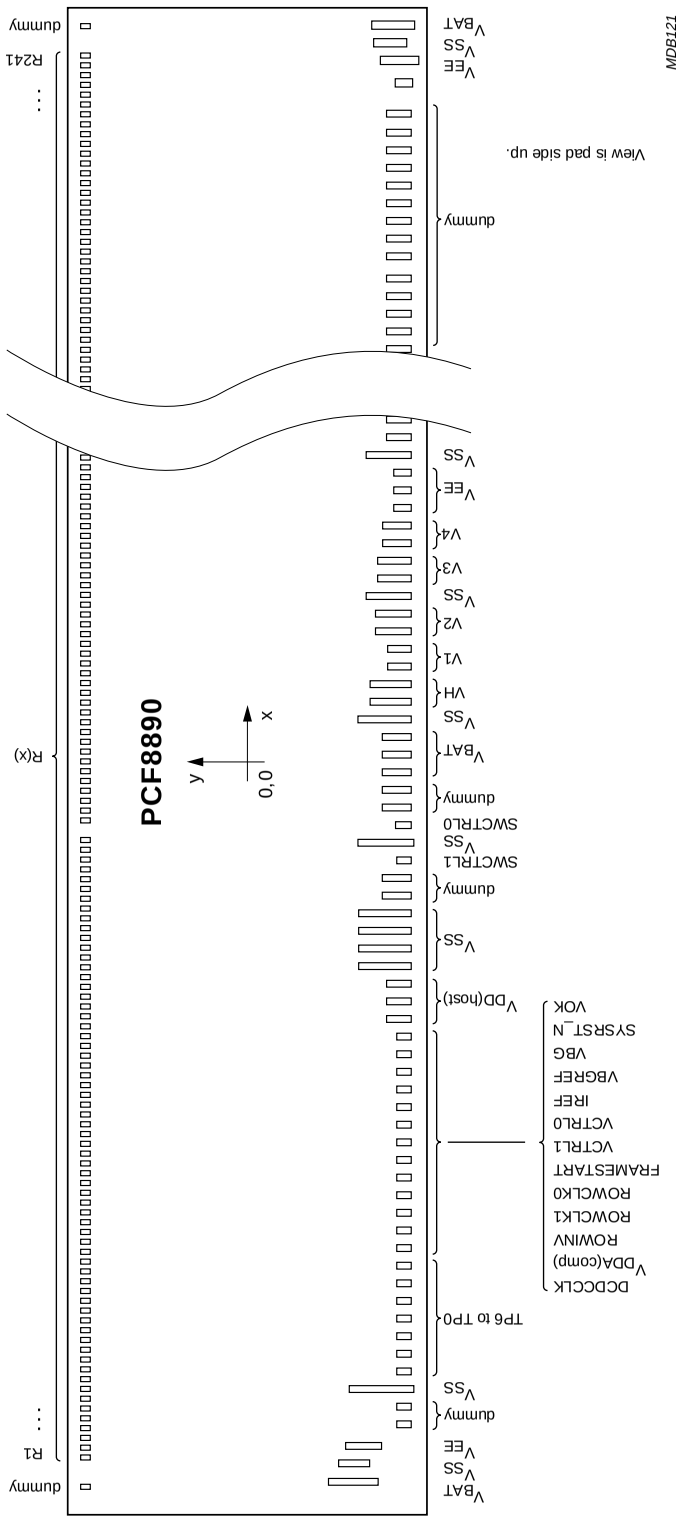


Fig.11 Bonding pad location.

Table 2 Bonding pad locations; all x and y coordinates are referenced to the centre of the chip (dimensions in μm; see Fig.11)

SYMBOL	PAD	COORDINATES		BUMP TYPE
		x	y	
dummy	1	–8002	+1153	1
R1	2	–7746	+1153	2
R2	3	–7682	+1153	2
R3	4	–7618	+1153	2
R4	5	–7554	+1153	2
R5	6	–7490	+1153	2
R6	7	–7426	+1153	2
R7	8	–7362	+1153	2
R8	9	–7298	+1153	2
R9	10	–7234	+1153	2
R10	11	–7170	+1153	2
R11	12	–7106	+1153	2
R12	13	–7042	+1153	2
R13	14	–6978	+1153	2
R14	15	–6914	+1153	2
R15	16	–6850	+1153	2
R16	17	–6786	+1153	2
R17	18	–6722	+1153	2
R18	19	–6658	+1153	2
R19	20	–6594	+1153	2
R20	21	–6530	+1153	2
R21	22	–6466	+1153	2
R22	23	–6402	+1153	2
R23	24	–6338	+1153	2
R24	25	–6274	+1153	2
R25	26	–6210	+1153	2
R26	27	–6146	+1153	2
R27	28	–6082	+1153	2
R28	29	–6018	+1153	2
R29	30	–5954	+1153	2
R30	31	–5890	+1153	2
R31	32	–5826	+1153	2
R32	33	–5762	+1153	2
R33	34	–5698	+1153	2
R34	35	–5634	+1153	2
R35	36	–5570	+1153	2
R36	37	–5506	+1153	2
R37	38	–5442	+1153	2
R38	39	–5378	+1153	2
R39	40	–5314	+1153	2
R40	41	–5250	+1153	2
R41	42	–5186	+1153	2
R42	43	–5122	+1153	2
R43	44	–5058	+1153	2
R44	45	–4994	+1153	2
R45	46	–4930	+1153	2
R46	47	–4866	+1153	2
R47	48	–4802	+1153	2
R48	49	–4738	+1153	2
R49	50	–4674	+1153	2
R50	51	–4610	+1153	2
R51	52	–4546	+1153	2
R52	53	–4482	+1153	2
R53	54	–4418	+1153	2
R54	55	–4354	+1153	2
R55	56	–4290	+1153	2
R56	57	–4226	+1153	2
R57	58	–4162	+1153	2
R58	59	–4098	+1153	2
R59	60	–4034	+1153	2
R60	61	–3970	+1153	2
R61	62	–3906	+1153	2
R62	63	–3842	+1153	2
R63	64	–3778	+1153	2
R64	65	–3714	+1153	2
R65	66	–3586	+1153	2
R66	67	–3522	+1153	2
R67	68	–3458	+1153	2
R68	69	–3394	+1153	2
R69	70	–3330	+1153	2
R70	71	–3266	+1153	2
R71	72	–3202	+1153	2
R72	73	–3138	+1153	2
R73	74	–3074	+1153	2
R74	75	–3010	+1153	2
R75	76	–2946	+1153	2

SYMBOL	PAD	COORDINATES		BUMP TYPE
		x	y	
R76	77	−2882	+1153	2
R77	78	−2818	+1153	2
R78	79	−2754	+1153	2
R79	80	−2690	+1153	2
R80	81	−2626	+1153	2
R81	82	−2562	+1153	2
R82	83	−2498	+1153	2
R83	84	−2434	+1153	2
R84	85	−2370	+1153	2
R85	86	−2306	+1153	2
R86	87	−2242	+1153	2
R87	88	−2178	+1153	2
R88	89	−2114	+1153	2
R89	90	−2050	+1153	2
R90	91	−1986	+1153	2
R91	92	−1922	+1153	2
R92	93	−1858	+1153	2
R93	94	−1794	+1153	2
R94	95	−1730	+1153	2
R95	96	−1666	+1153	2
R96	97	−1602	+1153	2
R97	98	−1538	+1153	2
R98	99	−1474	+1153	2
R99	100	−1410	+1153	2
R100	101	−1346	+1153	2
R101	102	−1282	+1153	2
R102	103	−1218	+1153	2
R103	104	−1154	+1153	2
R104	105	−1090	+1153	2
R105	106	−1026	+1153	2
R106	107	−962	+1153	2
R107	108	−898	+1153	2
R108	109	−834	+1153	2
R109	110	−770	+1153	2
R110	111	−706	+1153	2
R111	112	−642	+1153	2
R112	113	−578	+1153	2
R113	114	−514	+1153	2
R114	115	−450	+1153	2

SYMBOL	PAD	COORDINATES		BUMP TYPE
		x	y	
R115	116	−386	+1153	2
R116	117	−322	+1153	2
R117	118	−258	+1153	2
R118	119	−194	+1153	2
R119	120	−130	+1153	2
R120	121	−66	+1153	2
R121	122	−2	+1153	2
R122	123	+62	+1153	2
R123	124	+126	+1153	2
R124	125	+190	+1153	2
R125	126	+254	+1153	2
R126	127	+318	+1153	2
R127	128	+382	+1153	2
R128	129	+446	+1153	2
R129	130	+574	+1153	2
R130	131	+638	+1153	2
R131	132	+702	+1153	2
R132	133	+766	+1153	2
R133	134	+830	+1153	2
R134	135	+894	+1153	2
R135	136	+958	+1153	2
R136	137	+1022	+1153	2
R137	138	+1086	+1153	2
R138	139	+1150	+1153	2
R139	140	+1214	+1153	2
R140	141	+1278	+1153	2
R141	142	+1342	+1153	2
R142	143	+1406	+1153	2
R143	144	+1470	+1153	2
R144	145	+1534	+1153	2
R145	146	+1598	+1153	2
R146	147	+1662	+1153	2
R147	148	+1726	+1153	2
R148	149	+1790	+1153	2
R149	150	+1854	+1153	2
R150	151	+1918	+1153	2
R151	152	+1982	+1153	2
R152	153	+2046	+1153	2
R153	154	+2110	+1153	2

SYMBOL	PAD	COORDINATES		BUMP TYPE
		x	y	
R154	155	+2174	+1153	2
R155	156	+2338	+1153	2
R156	157	+2302	+1153	2
R157	158	+2366	+1153	2
R158	159	+2430	+1153	2
R159	160	+2494	+1153	2
R160	161	+2558	+1153	2
R161	162	+2622	+1153	2
R162	163	+2686	+1153	2
R163	164	+2750	+1153	2
R164	165	+2814	+1153	2
R165	166	+2878	+1153	2
R166	167	+2942	+1153	2
R167	168	+3006	+1153	2
R168	169	+3070	+1153	2
R169	170	+3134	+1153	2
R170	171	+3198	+1153	2
R171	172	+3262	+1153	2
R172	173	+3326	+1153	2
R173	174	+3390	+1153	2
R174	175	+3454	+1153	2
R175	176	+3518	+1153	2
R176	177	+3582	+1153	2
R177	178	+3646	+1153	2
R178	179	+3710	+1153	2
R179	180	+3774	+1153	2
R180	181	+3838	+1153	2
R181	182	+3902	+1153	2
R182	183	+3966	+1153	2
R183	184	+4030	+1153	2
R184	185	+4094	+1153	2
R185	186	+4158	+1153	2
R186	187	+4222	+1153	2
R187	188	+4286	+1153	2
R188	189	+4350	+1153	2
R189	190	+4414	+1153	2
R190	191	+4478	+1153	2
R191	192	+4542	+1153	2
R192	193	+4606	+1153	2

SYMBOL	PAD	COORDINATES		BUMP TYPE
		x	y	
R193	194	+4734	+1153	2
R194	195	+4798	+1153	2
R195	196	+4862	+1153	2
R196	197	+4926	+1153	2
R197	198	+4990	+1153	2
R198	199	+5054	+1153	2
R199	200	+5118	+1153	2
R200	201	+5182	+1153	2
R201	202+	+5246	+1153	2
R202	203	+5310	+1153	2
R203	204	+5374	+1153	2
R204	205	+5438	+1153	2
R205	206	+5502	+1153	2
R206	207	+5566	+1153	2
R207	208	+5630	+1153	2
R208	209	+5694	+1153	2
R209	210	+5758	+1153	2
R210	211	+5822	+1153	2
R211	212	+5886	+1153	2
R212	213	+5950	+1153	2
R213	214	+6014	+1153	2
R214	215	+6078	+1153	2
R215	216	+6142	+1153	2
R216	217	+6206	+1153	2
R217	218	+6270	+1153	2
R218	219	+6334	+1153	2
R219	220	+6398	+1153	2
R220	221	+6462	+1153	2
R221	222	+6526	+1153	2
R222	223	+6590	+1153	2
R223	224	+6654	+1153	2
R224	225	+6718	+1153	2
R225	226	+6782	+1153	2
R226	227	+6846	+1153	2
R227	228	+6910	+1153	2
R228	229	+6974	+1153	2
R229	230	+7038	+1153	2
R230	231	+7102	+1153	2
R231	232	+7166	+1153	2

SYMBOL	PAD	COORDINATES		BUMP TYPE
		x	y	
R232	233	+7230	+1153	2
R233	234	+7294	+1153	2
R234	235	+7358	+1153	2
R235	236	+7422	+1153	2
R236	237	+7486	+1153	2
R237	238	+7550	+1153	2
R238	239	+7614	+1153	2
R239	240	+7678	+1153	2
R240	241	+7742	+1153	2
R241	242	+7806	+1153	2
dummy	243	+7998	+1153	2
V_{BAT}	244	+7773	–1232	3
V_{SS}	245	+7663	–1232	4
V_{EE}	246	+7553	–1232	5
dummy	247	+7443	–1232	6
dummy	248	+7223	–1232	7
dummy	249	+7113	–1232	7
dummy	250	+7003	–1232	7
dummy	251	+6893	–1232	7
dummy	252	+6783	–1232	7
dummy	253	+6673	–1232	7
dummy	254	+6563	–1232	7
dummy	255	+6453	–1232	7
dummy	256	+6343	–1232	7
dummy	257	+6233	–1232	7
dummy	258	+6123	–1232	7
dummy	259	+6013	–1232	7
dummy	260	+5903	–1232	7
dummy	261	+5793	–1232	7
dummy	262	+5683	–1232	7
dummy	263	+5573	–1232	7
dummy	264	+5463	–1232	7
dummy	265	+5353	–1232	7
dummy	266	+5243	–1232	7
dummy	267	+5133	–1232	7
dummy	268	+5023	–1232	7
dummy	269	+4913	–1232	7
dummy	270	+4803	–1232	7
dummy	271	+4693	–1232	7

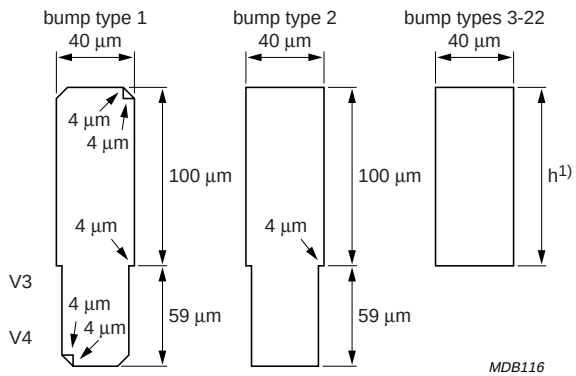
SYMBOL	PAD	COORDINATES		BUMP TYPE
		x	y	
dummy	272	+4583	–1232	7
dummy	273	+4473	–1232	7
dummy	274	+4363	–1232	7
dummy	275	+4253	–1232	7
dummy	276	+4143	–1232	7
dummy	277	+4033	–1232	7
dummy	278	+3923	–1232	7
dummy	279	+3813	–1232	7
dummy	280	+3703	–1232	7
dummy	281	+3593	–1232	7
dummy	282	+3483	–1232	7
dummy	283	+3373	–1232	7
dummy	284	+3263	–1232	7
dummy	285	+3153	–1232	7
dummy	286	+3043	–1232	7
dummy	287	+2933	–1232	7
dummy	288	+2823	–1232	7
dummy	289	+2713	–1232	7
dummy	290	+2603	–1232	7
dummy	291	+2493	–1232	7
dummy	292	+2383	–1232	7
dummy	293	+2273	–1232	7
dummy	294	+2163	–1232	7
dummy	295	+2053	–1232	7
dummy	296	+1943	–1232	7
dummy	297	+1833	–1232	7
dummy	298	+1723	–1232	7
dummy	299	+1613	–1232	7
dummy	300	+1503	–1232	7
dummy	301	+1393	–1232	7
dummy	302	+1283	–1232	7
dummy	303	+1173	–1232	7
dummy	304	+1063	–1232	7
dummy	305	+953	–1232	7
dummy	306	+843	–1232	7
dummy	307	+733	–1232	7
dummy	308	+623	–1232	7
dummy	309	+513	–1232	7
dummy	310	+403	–1232	7

SYMBOL	PAD	COORDINATES		BUMP TYPE
		x	y	
dummy	311	+293	−1232	7
dummy	312	+183	−1232	7
dummy	313	+73	−1232	7
dummy	314	−37	−1232	7
dummy	315	−147	−1232	7
dummy	316	−257	−1232	7
dummy	317	−367	−1232	7
dummy	318	−477	−1232	7
dummy	319	−587	−1232	7
dummy	320	−697	−1232	7
dummy	321	−807	−1232	7
dummy	322	−917	−1232	7
dummy	323	−1027	−1232	7
dummy	324	−1137	−1232	7
dummy	325	−1247	−1232	7
V_{SS}	326	−1357	−1232	8
V_{EE}	327	−1467	−1232	9
V_{EE}	328	−1577	−1232	9
V_{EE}	329	−1687	−1232	9
V4	330	−1797	−1232	10
V4	331	−1907	−1232	10
V3	332	−2017	−1232	11
V3	333	−2127	−1232	11
V_{SS}	334	−2237	−1232	8
V2	335	−2347	−1232	12
V2	336	−2457	−1232	12
V1	337	−2567	−1232	13
V1	338	−2677	−1232	13
VH	339	−2787	−1232	14
VH	340	−2897	−1232	14
V_{SS}	341	−3007	−1232	15
V_{BAT}	342	−3117	−1232	10
V_{BAT}	343	−3227	−1232	10
V_{BAT}	344	−3337	−1232	10
dummy	345	−3447	−1232	10
dummy	346	−3557	−1232	10
SWCTRL0	347	−3667	−1232	6
V_{SS}	348	−3777	−1232	16
SWCTRL1	349	−3887	−1232	6

SYMBOL	PAD	COORDINATES		BUMP TYPE
		x	y	
dummy	350	−3997	−1232	10
dummy	351	−4107	−1232	10
V_{SS}	352	−4217	−1232	15
V_{SS}	353	−4327	−1232	15
V_{SS}	354	−4437	−1232	15
V_{SS}	355	−4547	−1232	15
$V_{DD(host)}$	356	−4657	−1232	17
$V_{DD(host)}$	357	−4667	−1232	17
$V_{DD(host)}$	358	−4877	−1232	17
VOK	359	−4987	−1232	6
SYSRST_N	360	−5097	−1232	6
VBG	361	−5207	−1232	6
VBGREF	362	−5317	−1232	6
IREF	363	−5427	−1232	6
VCTRL0	364	−5537	−1232	6
VCTRL1	365	−5647	−1232	6
FRAMESTART	366	−5757	−1232	6
ROWCLK0	367	−5867	−1232	6
ROWCLK1	368	−5977	−1232	6
ROWINV	369	−6087	−1232	6
$V_{DDA(comp)}$	370	−6197	−1232	6
DCDCCLK	371	−6307	−1232	6
TP6	372	−6417	−1232	6
TP4	373	−6527	−1232	6
TP5	374	−6637	−1232	6
TP0	375	−6747	−1232	6
TP1	376	−6857	−1232	6
TP2	377	−6967	−1232	6
TP3	378	−7077	−1232	6
V_{SS}	379	−7187	−1232	18
dummy	380	−7297	−1232	6
dummy	381	−7407	−1232	6
V_{EE}	382	−7517	−1232	19
V_{SS}	383	−7627	−1232	20
V_{BAT}	384	−7737	−1232	21

Table 3 Bonding pad information

ITEM	DIMENSIONS
Pad pitch	64 μm
Bump dimension	see Fig.12
Chip size	16300 × 2950 μm
Wafer thickness (bumps not included)	380 μm



(1) see Table 4

Fig.12 Bump dimensions.

Table 4 Bump dimensions

BUMP TYPE	h (μm)
3	333
4	234
5	273
6	106
7	180
8	344
9	113
10	212
11	245
12	278
13	179
14	311
15	410
16	442
17	166
18	512
19	272
20	233
21	383

16 TRAY INFORMATION

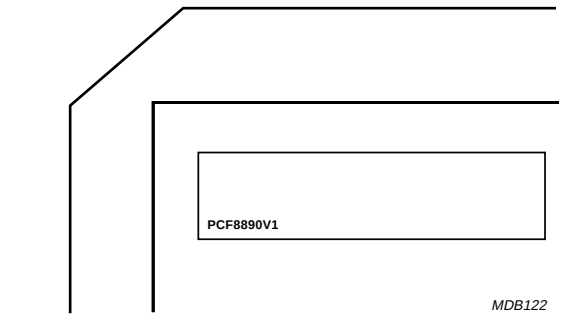


Fig.13 Chip orientation.

17 DATA SHEET STATUS

LEVEL	DATA SHEET STATUS(1)	PRODUCT STATUS(2)(3)	DEFINITION
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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3. For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

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Printed in The Netherlands 403512/01/pp24 Date of release: 2003 Feb 25 Document order number: 9397 750 10898

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