

# 74HC373; 74HCT373

Octal D-type transparent latch; 3-state

Rev. 03 — 20 January 2006

Product data sheet

## 1. General description

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The 74HC373; 74HCT373 is a high-speed Si-gate CMOS device and is pin compatible with Low-power Schottky TTL. It is specified in compliance with JEDEC standard no. 7A.

The 74HC373; 74HCT373 is an octal D-type transparent latch featuring separate D-type inputs for each latch and 3-state outputs for bus oriented applications. A latch enable (LE) input and an output enable ( $\overline{OE}$ ) input are common to all latches.

The 74HC373; HCT373 consists of eight D-type transparent latches with 3-state true outputs. When LE is HIGH, data at the Dn inputs enters the latches. In this condition the latches are transparent, i.e. a latch output will change state each time its corresponding D input changes.

When LE is LOW the latches store the information that was present at the D inputs a set-up time preceding the HIGH-to-LOW transition of LE. When  $\overline{OE}$  is LOW, the contents of the 8 latches are available at the outputs. When  $\overline{OE}$  is HIGH, the outputs go to the high-impedance OFF-state. Operation of the  $\overline{OE}$  input does not affect the state of the latches.

The 74HC373; 74HCT373 is functionally identical to:

- 74HC533; 74HCT533: but inverted outputs
- 74HC563; 74HCT563: but inverted outputs and different pin arrangement
- 74HC573; 74HCT573: but different pin arrangement

## 2. Features

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- 3-state non-inverting outputs for bus oriented applications
- Common 3-state output enable input
- Functionally identical to the 74HC563; 74HCT563, 74HC573; 74HCT573 and 74HC533; 74HCT533
- ESD protection:
  - ◆ HBM EIA/JESD22-A114-C exceeds 2 000 V
  - ◆ MM EIA/JESD22-A115-A exceeds 200 V
- Specified from  $-40\text{ }^{\circ}\text{C}$  to  $+85\text{ }^{\circ}\text{C}$  and from  $-40\text{ }^{\circ}\text{C}$  to  $+125\text{ }^{\circ}\text{C}$

**PHILIPS**

### 3. Quick reference data

**Table 1: Quick reference data**

$GND = 0\text{ V}$ ;  $T_{amb} = 25\text{ °C}$ ;  $t_r = t_f = 6\text{ ns}$ .

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	
<b>74HC373</b>							
$t_{PHL}$ , $t_{PLH}$	propagation delay	$V_{CC} = 5\text{ V}$ ; $C_L = 15\text{ pF}$					
	Dn to Qn		-	12	-	ns	
	LE to Qn		-	15	-	ns	
$C_i$	input capacitance		-	3.5	-	pF	
$C_{PD}$	power dissipation capacitance	per latch; $V_I = GND$ to $V_{CC}$	[1]	-	45	-	pF
<b>74HCT373</b>							
$t_{PHL}$ , $t_{PLH}$	propagation delay	$V_{CC} = 5\text{ V}$ ; $C_L = 15\text{ pF}$					
	Dn to Qn		-	14	-	ns	
	LE to Qn		-	13	-	ns	
$C_i$	input capacitance		-	3.5	-	pF	
$C_{PD}$	power dissipation capacitance	per latch; $V_I = GND$ to $(V_{CC} - 1.5\text{ V})$	[1]	-	41	-	pF

[1]  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu\text{W}$ ).

$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum(C_L \times V_{CC}^2 \times f_o)$  where:

$f_i$  = input frequency in MHz;

$f_o$  = output frequency in MHz;

$C_L$  = output load capacitance in pF;

$V_{CC}$  = supply voltage in V;

$N$  = number of inputs switching;

$\sum(C_L \times V_{CC}^2 \times f_o)$  = sum of outputs.

### 4. Ordering information

**Table 2: Ordering information**

Type number	Package			
	Temperature range	Name	Description	Version
<b>74HC373</b>				
74HC373N	-40 °C to +125 °C	DIP20	plastic dual in-line package; 20 leads (300 mil)	SOT146-1
74HC373D	-40 °C to +125 °C	SO20	plastic small outline package; 20 leads; body width 7.5 mm	SOT163-1
74HC373DB	-40 °C to +125 °C	SSOP20	plastic shrink small outline package; 20 leads; body width 5.3 mm	SOT339-1
74HC373PW	-40 °C to +125 °C	TSSOP20	plastic thin shrink small outline package; 20 leads; body width 4.4 mm	SOT360-1
74HC373BQ	-40 °C to +125 °C	DHVQFN20	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 20 terminals; body 2.5 × 4.5 × 0.85 mm	SOT764-1

Table 2: Ordering information ...continued

Type number	Package			Version
	Temperature range	Name	Description	
<b>74HCT373</b>				
74HCT373N	-40 °C to +125 °C	DIP20	plastic dual in-line package; 20 leads (300 mil)	SOT146-1
74HCT373D	-40 °C to +125 °C	SO20	plastic small outline package; 20 leads; body width 7.5 mm	SOT163-1
74HCT373DB	-40 °C to +125 °C	SSOP20	plastic shrink small outline package; 20 leads; body width 5.3 mm	SOT339-1
74HCT373PW	-40 °C to +125 °C	TSSOP20	plastic thin shrink small outline package; 20 leads; body width 4.4 mm	SOT360-1
74HCT373BQ	-40 °C to +125 °C	DHVQFN20	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 20 terminals; body 2.5 × 4.5 × 0.85 mm	SOT764-1

## 5. Functional diagram

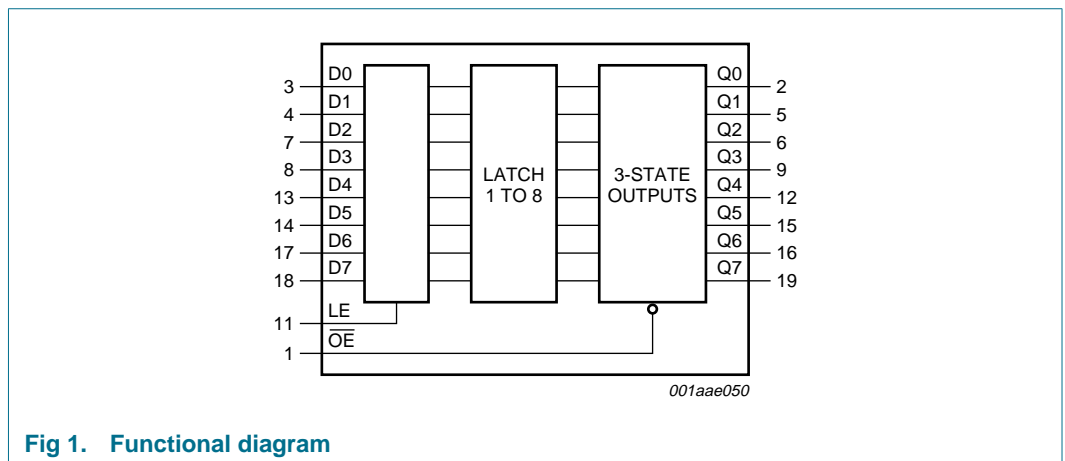


Fig 1. Functional diagram

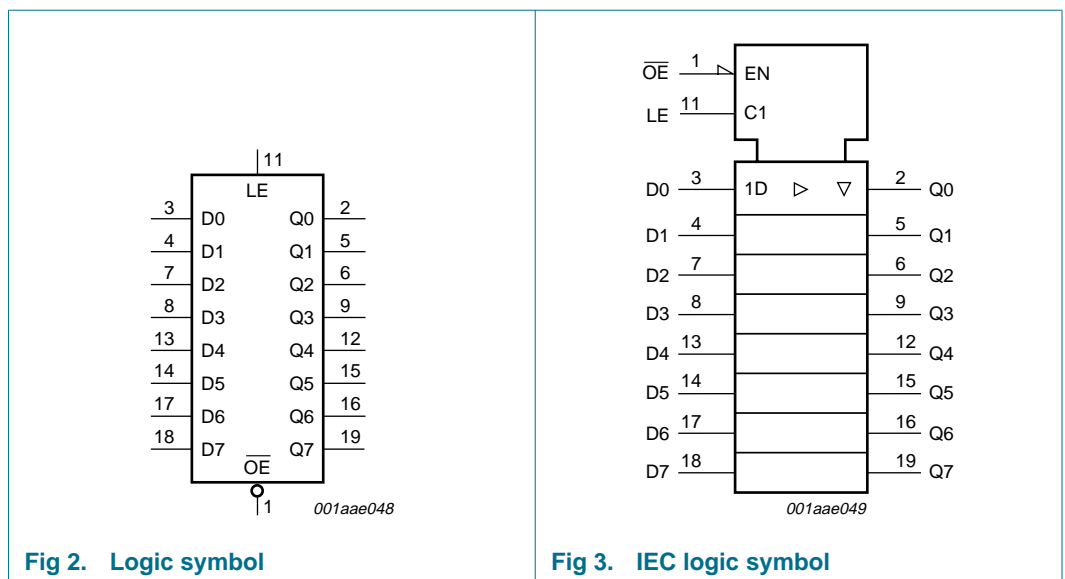
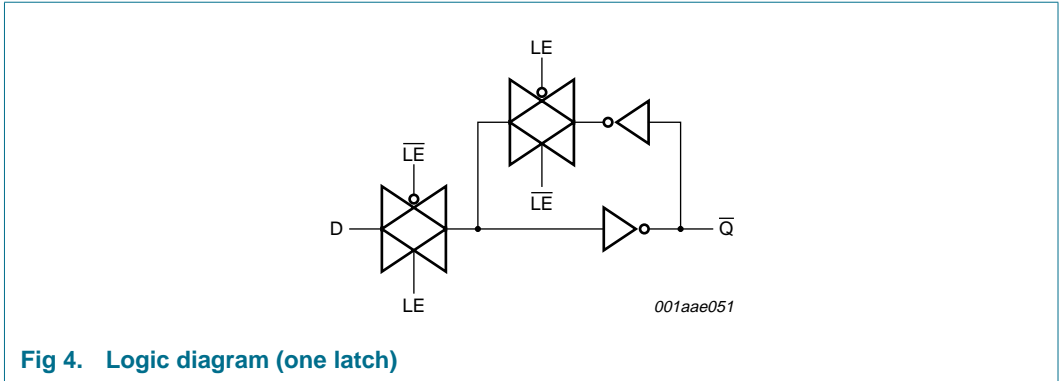
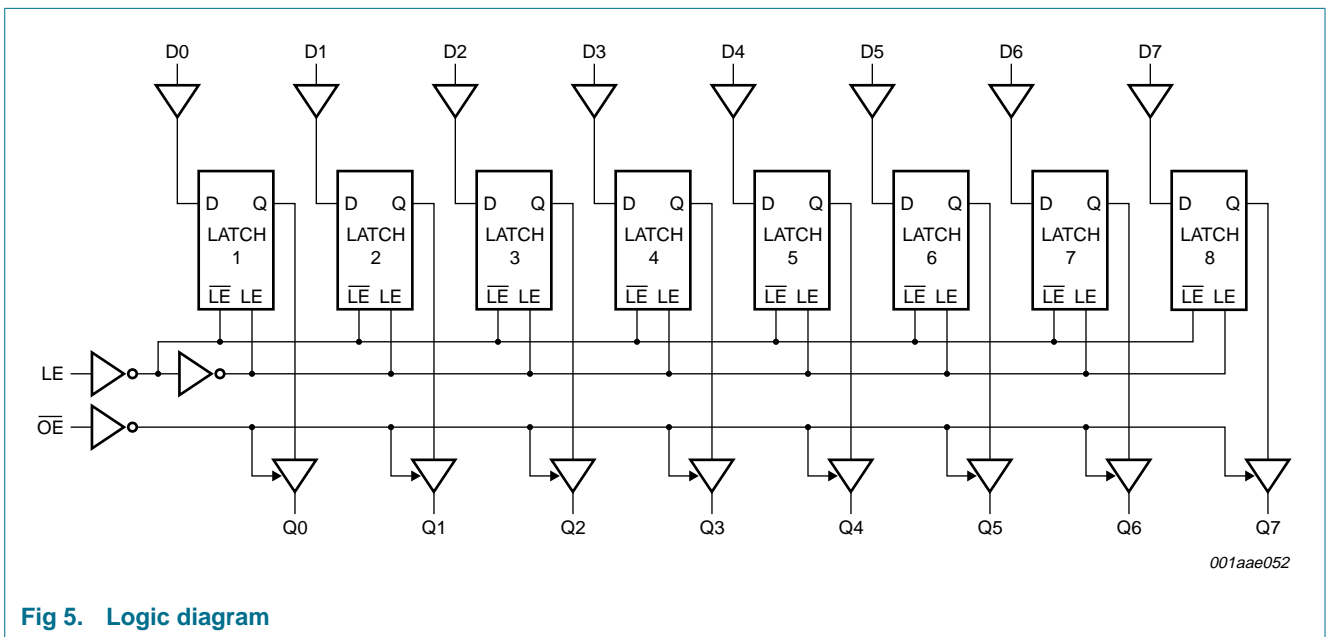


Fig 2. Logic symbol

Fig 3. IEC logic symbol



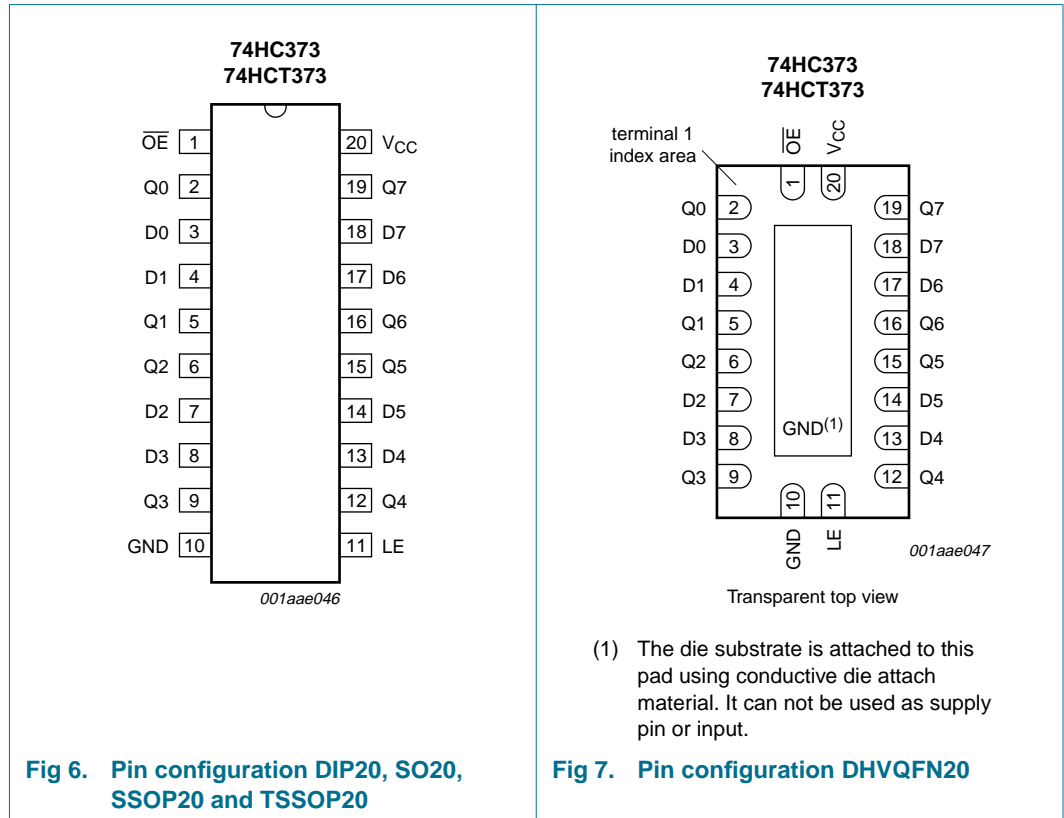
**Fig 4. Logic diagram (one latch)**



**Fig 5. Logic diagram**

## 6. Pinning information

### 6.1 Pinning



### 6.2 Pin description

Table 3: Pin description

Symbol	Pin	Description
OE	1	3-state output enable input (active LOW)
Q0	2	3-state latch output 0
D0	3	data input 0
D1	4	data input 1
Q1	5	3-state latch output 1
Q2	6	3-state latch output 2
D2	7	data input 2
D3	8	data input 3
Q3	9	3-state latch output 3
GND	10	ground (0 V)
LE	11	latch enable input (active HIGH)
Q4	12	3-state latch output 4
D4	13	data input 4
D5	14	data input 5

Table 3: Pin description ...continued

Symbol	Pin	Description
Q5	15	3-state latch output 5
Q6	16	3-state latch output 6
D6	17	data input 6
D7	18	data input 7
Q7	19	3-state latch output 7
V <sub>CC</sub>	20	supply voltage

## 7. Functional description

### 7.1 Function table

Table 4: Function table [1]

Operating mode	Control		Input	Internal latches	Output
	OE	LE	D <sub>n</sub>		Q <sub>n</sub>
Enable and read register (transparent mode)	L	H	L	L	L
			H	H	H
Latch and read register	L	L	I	L	L
			h	H	H
Latch register and disable outputs	H	X	X	X	Z

- [1] H = HIGH voltage level;  
 h = HIGH voltage level one set-up time prior to the HIGH-to-LOW LE transition;  
 L = LOW voltage level;  
 I = LOW voltage level one set-up time prior to the HIGH-to-LOW LE transition;  
 X = don't care;  
 Z = high-impedance OFF-state.

## 8. Limiting values

**Table 5: Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC}$	supply voltage		-0.5	+7	V
$I_{IK}$	input clamping current	$V_I < -0.5\text{ V}$ or $V_I > V_{CC} + 0.5\text{ V}$	-	$\pm 20$	mA
$I_{OK}$	output clamping current	$V_O < -0.5\text{ V}$ or $V_O > V_{CC} + 0.5\text{ V}$	-	$\pm 20$	mA
$I_O$	output current	$V_O = -0.5\text{ V}$ to $(V_{CC} + 0.5\text{ V})$	-	$\pm 35$	mA
$I_{CC}$	quiescent supply current		-	+70	mA
$I_{GND}$	ground current		-	-70	mA
$T_{stg}$	storage temperature		-65	+150	°C
$P_{tot}$	total power dissipation				
	DIP20 package		[1] -	750	mW
	SO20 package		[2] -	500	mW
	SSOP20 package		[3]	500	mW
	TSSOP20 package		[3]	500	mW
	DHVQFN20 package		[4] -	500	mW

[1] For DIP20 package:  $P_{tot}$  derates linearly with 12 mW/K above 70 °C.

[2] For SO20:  $P_{tot}$  derates linearly with 8 mW/K above 70 °C.

[3] For SSOP20 and TSSOP20 packages:  $P_{tot}$  derates linearly with 5.5 mW/K above 60 °C.

[4] For DHVQFN20 package:  $P_{tot}$  derates linearly with 4.5 mW/K above 60 °C.

## 9. Recommended operating conditions

**Table 6: Recommended operating conditions**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>74HC373</b>						
$V_{CC}$	supply voltage		2.0	5.0	6.0	V
$V_I$	input voltage		0	-	$V_{CC}$	V
$V_O$	output voltage		0	-	$V_{CC}$	V
$T_{amb}$	ambient temperature		-40	+25	+125	°C
$t_r, t_f$	input rise and fall time	$V_{CC} = 2.0\text{ V}$	-	-	1000	ns
		$V_{CC} = 4.5\text{ V}$	-	6.0	500	ns
		$V_{CC} = 6.0\text{ V}$	-	-	400	ns
<b>74HCT373</b>						
$V_{CC}$	supply voltage		4.5	5.0	5.5	V
$V_I$	input voltage		0	-	$V_{CC}$	V
$V_O$	output voltage		0	-	$V_{CC}$	V
$T_{amb}$	ambient temperature		-40	+25	+125	°C
$t_r, t_f$	input rise and fall time	$V_{CC} = 4.5\text{ V}$	-	6.0	500	ns

## 10. Static characteristics

**Table 7: Static characteristics 74HC373**
*At recommended operating conditions; voltages are referenced to GND (ground = 0 V).*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b><math>T_{amb} = 25\text{ °C}</math></b>						
$V_{IH}$	HIGH-state input voltage	$V_{CC} = 2.0\text{ V}$	1.5	1.2	-	V
		$V_{CC} = 4.5\text{ V}$	3.15	2.4	-	V
		$V_{CC} = 6.0\text{ V}$	4.2	3.2	-	V
$V_{IL}$	LOW-state input voltage	$V_{CC} = 2.0\text{ V}$	-	0.8	0.5	V
		$V_{CC} = 4.5\text{ V}$	-	2.1	1.35	V
		$V_{CC} = 6.0\text{ V}$	-	2.8	1.8	V
$V_{OH}$	HIGH-state output voltage	$V_I = V_{IH}$ or $V_{IL}$	-	-	-	
		$I_O = -20\text{ }\mu\text{A}$ ; $V_{CC} = 2.0\text{ V}$	1.9	2.0	-	V
		$I_O = -20\text{ }\mu\text{A}$ ; $V_{CC} = 4.5\text{ V}$	4.4	4.5	-	V
		$I_O = -20\text{ }\mu\text{A}$ ; $V_{CC} = 6.0\text{ V}$	5.9	6.0	-	V
		$I_O = -6.0\text{ mA}$ ; $V_{CC} = 4.5\text{ V}$	3.98	4.32	-	V
$V_{OL}$	LOW-state output voltage	$V_I = V_{IH}$ or $V_{IL}$	-	-	-	
		$I_O = 20\text{ }\mu\text{A}$ ; $V_{CC} = 2.0\text{ V}$	-	0	0.1	V
		$I_O = 20\text{ }\mu\text{A}$ ; $V_{CC} = 4.5\text{ V}$	-	0	0.1	V
		$I_O = 20\text{ }\mu\text{A}$ ; $V_{CC} = 6.0\text{ V}$	-	0	0.1	V
		$I_O = 6.0\text{ mA}$ ; $V_{CC} = 4.5\text{ V}$	-	0.15	0.26	V
	$I_O = 7.8\text{ mA}$ ; $V_{CC} = 6.0\text{ V}$	-	0.16	0.26	V	
$I_{LI}$	input leakage current	$V_I = V_{CC}$ or GND; $V_{CC} = 6.0\text{ V}$	-	-	$\pm 0.1$	$\mu\text{A}$
$I_{OZ}$	OFF-state output current	$V_I = V_{IH}$ or $V_{IL}$ ; $V_{CC} = 6.0\text{ V}$ ; $V_O = V_{CC}$ or GND	-	-	$\pm 0.5$	$\mu\text{A}$
$I_{CC}$	quiescent supply current	$V_{CC} = 6.0\text{ V}$ ; $I_O = 0\text{ A}$ ; $V_I = V_{CC}$ or GND	-	-	8.0	$\mu\text{A}$
$C_i$	input capacitance		-	3.5	-	pF
<b><math>T_{amb} = -40\text{ °C to }+85\text{ °C}</math></b>						
$V_{IH}$	HIGH-state input voltage	$V_{CC} = 2.0\text{ V}$	1.5	-	-	V
		$V_{CC} = 4.5\text{ V}$	3.15	-	-	V
		$V_{CC} = 6.0\text{ V}$	4.2	-	-	V
$V_{IL}$	LOW-state input voltage	$V_{CC} = 2.0\text{ V}$	-	-	0.5	V
		$V_{CC} = 4.5\text{ V}$	-	-	1.35	V
		$V_{CC} = 6.0\text{ V}$	-	-	1.8	V
$V_{OH}$	HIGH-state output voltage	$V_I = V_{IH}$ or $V_{IL}$	-	-	-	
		$I_O = -20\text{ }\mu\text{A}$ ; $V_{CC} = 2.0\text{ V}$	1.9	-	-	V
		$I_O = -20\text{ }\mu\text{A}$ ; $V_{CC} = 4.5\text{ V}$	4.4	-	-	V
		$I_O = -20\text{ }\mu\text{A}$ ; $V_{CC} = 6.0\text{ V}$	5.9	-	-	V
		$I_O = -6.0\text{ mA}$ ; $V_{CC} = 4.5\text{ V}$	3.84	-	-	V
	$I_O = -7.8\text{ mA}$ ; $V_{CC} = 6.0\text{ V}$	5.34	-	-	V	



**Table 7: Static characteristics 74HC373 ...continued**

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V <sub>OL</sub>	LOW-state output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>				
		I <sub>O</sub> = 20 μA; V <sub>CC</sub> = 2.0 V	-	-	0.1	V
		I <sub>O</sub> = 20 μA; V <sub>CC</sub> = 4.5 V	-	-	0.1	V
		I <sub>O</sub> = 20 μA; V <sub>CC</sub> = 6.0 V	-	-	0.1	V
		I <sub>O</sub> = 6.0 mA; V <sub>CC</sub> = 4.5 V	-	-	0.33	V
		I <sub>O</sub> = 7.8 mA; V <sub>CC</sub> = 6.0 V	-	-	0.33	V
I <sub>LI</sub>	input leakage current	V <sub>I</sub> = V <sub>CC</sub> or GND; V <sub>CC</sub> = 6.0 V	-	-	±1.0	μA
I <sub>OZ</sub>	OFF-state output current	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; V <sub>CC</sub> = 6.0 V; V <sub>O</sub> = V <sub>CC</sub> or GND	-	-	±5.0	μA
I <sub>CC</sub>	quiescent supply current	V <sub>CC</sub> = 6.0 V; I <sub>O</sub> = 0 A; V <sub>I</sub> = V <sub>CC</sub> or GND		-	80	μA
<b>T<sub>amb</sub> = -40 °C to +125 °C</b>						
V <sub>IH</sub>	HIGH-state input voltage	V <sub>CC</sub> = 2.0 V	1.5	-	-	V
		V <sub>CC</sub> = 4.5 V	3.15	-	-	V
		V <sub>CC</sub> = 6.0 V	4.2	-	-	V
V <sub>IL</sub>	LOW-state input voltage	V <sub>CC</sub> = 2.0 V	-	-	0.5	V
		V <sub>CC</sub> = 4.5 V	-	-	1.35	V
		V <sub>CC</sub> = 6.0 V	-	-	1.8	V
V <sub>OH</sub>	HIGH-state output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>				
		I <sub>O</sub> = -20 μA; V <sub>CC</sub> = 2.0 V	1.9	-	-	V
		I <sub>O</sub> = -20 μA; V <sub>CC</sub> = 4.5 V	4.4	-	-	V
		I <sub>O</sub> = -20 μA; V <sub>CC</sub> = 6.0 V	5.9	-	-	V
		I <sub>O</sub> = -6.0 mA; V <sub>CC</sub> = 4.5 V	3.7	-	-	V
		I <sub>O</sub> = -7.8 mA; V <sub>CC</sub> = 6.0 V	5.2	-	-	V
V <sub>OL</sub>	LOW-state output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>				
		I <sub>O</sub> = 20 μA; V <sub>CC</sub> = 2.0 V	-	-	0.1	V
		I <sub>O</sub> = 20 μA; V <sub>CC</sub> = 4.5 V	-	-	0.1	V
		I <sub>O</sub> = 20 μA; V <sub>CC</sub> = 6.0 V	-	-	0.1	V
		I <sub>O</sub> = 6.0 mA; V <sub>CC</sub> = 4.5 V	-	-	0.4	V
		I <sub>O</sub> = 7.8 mA; V <sub>CC</sub> = 6.0 V	-	-	0.4	V
I <sub>LI</sub>	input leakage current	V <sub>I</sub> = V <sub>CC</sub> or GND; V <sub>CC</sub> = 6.0 V	-	-	±1.0	μA
I <sub>OZ</sub>	OFF-state output current	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; V <sub>CC</sub> = 6.0 V; V <sub>O</sub> = V <sub>CC</sub> or GND	-	-	±10.0	μA
I <sub>CC</sub>	quiescent supply current	V <sub>CC</sub> = 6.0 V; I <sub>O</sub> = 0 A; V <sub>I</sub> = V <sub>CC</sub> or GND	-	-	160	μA

**Table 8: Static characteristics 74HCT373**

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>T<sub>amb</sub> = 25 °C</b>						
V <sub>IH</sub>	HIGH-state input voltage	V <sub>CC</sub> = 4.5 V to 5.5 V	2.0	1.6	-	V
V <sub>IL</sub>	LOW-state input voltage	V <sub>CC</sub> = 4.5 V to 5.5 V	-	1.2	0.8	V
V <sub>OH</sub>	HIGH-state output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>				
		I <sub>O</sub> = -20 µA; V <sub>CC</sub> = 4.5 V	4.4	4.5	-	V
		I <sub>O</sub> = -6.0 mA; V <sub>CC</sub> = 4.5 V	3.98	4.32	-	V
V <sub>OL</sub>	LOW-state output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>				
		I <sub>O</sub> = 20 µA; V <sub>CC</sub> = 4.5 V	-	0.0	0.1	V
		I <sub>O</sub> = 6.0 mA; V <sub>CC</sub> = 4.5 V	-	0.16	0.26	V
I <sub>LI</sub>	input leakage current	V <sub>I</sub> = V <sub>CC</sub> or GND; V <sub>CC</sub> = 5.5 V	-	-	±0.1	µA
I <sub>OZ</sub>	OFF-state output current	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; V <sub>CC</sub> = 5.5 V; V <sub>O</sub> = V <sub>CC</sub> or GND per input pin; other inputs at V <sub>CC</sub> or GND; I <sub>O</sub> = 0 A	-	-	±0.5	µA
I <sub>CC</sub>	quiescent supply current	V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0 A; V <sub>CC</sub> = 5.5 V	-	-	8.0	µA
ΔI <sub>CC</sub>	additional quiescent supply current	V <sub>I</sub> = V <sub>CC</sub> - 2.1 V; other inputs at V <sub>CC</sub> or GND; V <sub>CC</sub> = 4.5 V to 5.5 V; I <sub>O</sub> = 0 A				
		Dn	-	30	108	µA
		LE	-	150	540	µA
		$\overline{OE}$	-	100	360	µA
C <sub>i</sub>	input capacitance		-	3.5	-	pF
<b>T<sub>amb</sub> = -40 °C to +85 °C</b>						
V <sub>IH</sub>	HIGH-state input voltage	V <sub>CC</sub> = 4.5 V to 5.5 V	2.0	-	-	V
V <sub>IL</sub>	LOW-state input voltage	V <sub>CC</sub> = 4.5 V to 5.5 V	-	-	0.8	V
V <sub>OH</sub>	HIGH-state output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>				
		I <sub>O</sub> = -20 µA; V <sub>CC</sub> = 4.5 V	4.4	-	-	V
		I <sub>O</sub> = -6.0 µA; V <sub>CC</sub> = 4.5 V	3.84	-	-	V
V <sub>OL</sub>	LOW-state output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>				
		I <sub>O</sub> = 20 µA; V <sub>CC</sub> = 4.5 V	-	-	0.1	V
		I <sub>O</sub> = 6.0 mA; V <sub>CC</sub> = 4.5 V	-	-	0.33	V
I <sub>LI</sub>	input leakage current	V <sub>I</sub> = V <sub>CC</sub> or GND; V <sub>CC</sub> = 5.5 V	-	-	±1.0	µA
I <sub>OZ</sub>	OFF-state output current	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; V <sub>CC</sub> = 5.5 V; V <sub>O</sub> = V <sub>CC</sub> or GND per input pin; other inputs at V <sub>CC</sub> or GND; I <sub>O</sub> = 0 A	-	-	±5.0	µA
I <sub>CC</sub>	quiescent supply current	V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0 A; V <sub>CC</sub> = 5.5 V	-	-	80	µA
ΔI <sub>CC</sub>	additional quiescent supply current	V <sub>I</sub> = V <sub>CC</sub> - 2.1 V; other inputs at V <sub>CC</sub> or GND; V <sub>CC</sub> = 4.5 V to 5.5 V; I <sub>O</sub> = 0 A				
		Dn	-	-	135	µA
		LE	-	-	675	µA
		$\overline{OE}$	-	-	450	µA

**Table 8:** Static characteristics 74HCT373 ...continued

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>T<sub>amb</sub> = -40 °C to +125 °C</b>						
V <sub>IH</sub>	HIGH-state input voltage	V <sub>CC</sub> = 4.5 V to 5.5 V	2.0	-	-	V
V <sub>IL</sub>	LOW-state input voltage	V <sub>CC</sub> = 4.5 V to 5.5 V	-	-	0.8	V
V <sub>OH</sub>	HIGH-state output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>				
		I <sub>O</sub> = -20 µA; V <sub>CC</sub> = 4.5 V	4.4	-	-	V
		I <sub>O</sub> = -6.0 mA; V <sub>CC</sub> = 4.5 V	3.7	-	-	V
V <sub>OL</sub>	LOW-state output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>				
		I <sub>O</sub> = 20 µA; V <sub>CC</sub> = 4.5 V	-	-	0.1	V
		I <sub>O</sub> = 6.0 mA; V <sub>CC</sub> = 4.5 V	-	-	0.4	V
I <sub>LI</sub>	input leakage current	V <sub>I</sub> = V <sub>CC</sub> or GND; V <sub>CC</sub> = 5.5 V	-	-	±1.0	µA
I <sub>OZ</sub>	OFF-state output current	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; V <sub>CC</sub> = 5.5 V; V <sub>O</sub> = V <sub>CC</sub> or GND per input pin; other inputs at V <sub>CC</sub> or GND; I <sub>O</sub> = 0 A	-	-	±10	µA
I <sub>CC</sub>	quiescent supply current	V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0 A; V <sub>CC</sub> = 5.5 V	-	-	160	µA
ΔI <sub>CC</sub>	additional quiescent supply current	V <sub>I</sub> = V <sub>CC</sub> - 2.1 V; other inputs at V <sub>CC</sub> or GND; V <sub>CC</sub> = 4.5 V to 5.5 V; I <sub>O</sub> = 0 A				
		Dn	-	-	147	µA
		LE	-	-	735	µA
		$\overline{\text{OE}}$	-	-	490	µA

## 11. Dynamic characteristics

**Table 9:** Dynamic characteristics 74HC373Voltages are referenced to GND (ground = 0 V); C<sub>L</sub> = 50 pF unless otherwise specified; for test circuit see [Figure 12](#).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>T<sub>amb</sub> = 25 °C</b>						
t <sub>PHL</sub> , t <sub>PLH</sub>	propagation delay					
	Dn to Qn	see <a href="#">Figure 8</a>				
		V <sub>CC</sub> = 2.0 V	-	41	150	ns
		V <sub>CC</sub> = 4.5 V	-	15	30	ns
		V <sub>CC</sub> = 5 V; C <sub>L</sub> = 15 pF	-	12	-	ns
		V <sub>CC</sub> = 6.0 V	-	12	26	ns
	LE to Qn	see <a href="#">Figure 9</a>				
		V <sub>CC</sub> = 2.0 V	-	50	175	ns
		V <sub>CC</sub> = 4.5 V	-	18	35	ns
		V <sub>CC</sub> = 5 V; C <sub>L</sub> = 15 pF	-	15	-	ns
		V <sub>CC</sub> = 6.0 V	-	14	30	ns

**Table 9: Dynamic characteristics 74HC373 ...continued**

Voltages are referenced to GND (ground = 0 V);  $C_L = 50$  pF unless otherwise specified; for test circuit see [Figure 12](#).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	
t <sub>PZH</sub> , t <sub>PZL</sub>	3-state output enable time $\overline{OE}$ to Qn	see <a href="#">Figure 10</a>					
		$V_{CC} = 2.0$ V	-	44	150	ns	
		$V_{CC} = 4.5$ V	-	16	30	ns	
		$V_{CC} = 6.0$ V	-	13	26	ns	
t <sub>PHZ</sub> , t <sub>PLZ</sub>	3-state output disable time $\overline{OE}$ to Qn	see <a href="#">Figure 10</a>					
		$V_{CC} = 2.0$ V	-	47	150	ns	
		$V_{CC} = 4.5$ V	-	17	30	ns	
		$V_{CC} = 6.0$ V	-	14	26	ns	
t <sub>THL</sub> , t <sub>TLH</sub>	output transition time	see <a href="#">Figure 9</a>					
		$V_{CC} = 2.0$ V	-	14	60	ns	
		$V_{CC} = 4.5$ V	-	5	12	ns	
		$V_{CC} = 6.0$ V	-	4	10	ns	
t <sub>w</sub>	pulse width LE HIGH	see <a href="#">Figure 9</a>					
		$V_{CC} = 2.0$ V	80	17	-	ns	
		$V_{CC} = 4.5$ V	16	6	-	ns	
		$V_{CC} = 6.0$ V	14	5	-	ns	
t <sub>su</sub>	set-up time Dn to LE	see <a href="#">Figure 11</a>					
		$V_{CC} = 2.0$ V	50	14	-	ns	
		$V_{CC} = 4.5$ V	10	5	-	ns	
		$V_{CC} = 6.0$ V	9	4	-	ns	
t <sub>h</sub>	hold time Dn to LE	see <a href="#">Figure 11</a>					
		$V_{CC} = 2.0$ V	+5	-8	-	ns	
		$V_{CC} = 4.5$ V	+5	-3	-	ns	
		$V_{CC} = 6.0$ V	+5	-2	-	ns	
C <sub>PD</sub>	power dissipation capacitance	per latch; V <sub>I</sub> = GND to V <sub>CC</sub>	[1]	-	45	pF	
<b>T<sub>amb</sub> = -40 °C to +85 °C</b>							
t <sub>PHL</sub> , t <sub>PLH</sub>	propagation delay Dn to Qn	see <a href="#">Figure 8</a>					
		$V_{CC} = 2.0$ V	-	-	190	ns	
		$V_{CC} = 4.5$ V	-	-	38	ns	
			$V_{CC} = 6.0$ V	-	-	33	ns
	LE to Qn	see <a href="#">Figure 9</a>					
		$V_{CC} = 2.0$ V	-	-	220	ns	
		$V_{CC} = 4.5$ V	-	-	44	ns	
			$V_{CC} = 6.0$ V	-	-	37	ns
	t <sub>PZH</sub> , t <sub>PZL</sub>	3-state output enable time $\overline{OE}$ to Qn	see <a href="#">Figure 10</a>				
$V_{CC} = 2.0$ V			-	-	190	ns	
$V_{CC} = 4.5$ V			-	-	38	ns	
		$V_{CC} = 6.0$ V	-	-	33	ns	

**Table 9: Dynamic characteristics 74HC373 ...continued**

Voltages are referenced to GND (ground = 0 V);  $C_L = 50$  pF unless otherwise specified; for test circuit see [Figure 12](#).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{PHZ}$ , $t_{PLZ}$	3-state output disable time $\overline{OE}$ to Qn	see <a href="#">Figure 10</a>				
		$V_{CC} = 2.0$ V	-	-	190	ns
		$V_{CC} = 4.5$ V	-	-	38	ns
		$V_{CC} = 6.0$ V	-	-	33	ns
$t_{THL}$ , $t_{TLH}$	output transition time	see <a href="#">Figure 8</a>				
		$V_{CC} = 2.0$ V	-	-	75	ns
		$V_{CC} = 4.5$ V	-	-	15	ns
		$V_{CC} = 6.0$ V	-	-	13	ns
$t_W$	pulse width LE HIGH	see <a href="#">Figure 9</a>				
		$V_{CC} = 2.0$ V	100	-	-	ns
		$V_{CC} = 4.5$ V	20	-	-	ns
		$V_{CC} = 6.0$ V	17	-	-	ns
$t_{su}$	set-up time Dn to LE	see <a href="#">Figure 11</a>				
		$V_{CC} = 2.0$ V	65	-	-	ns
		$V_{CC} = 4.5$ V	13	-	-	ns
		$V_{CC} = 6.0$ V	11	-	-	ns
$t_h$	hold time Dn to LE	see <a href="#">Figure 11</a>				
		$V_{CC} = 2.0$ V	5	-	-	ns
		$V_{CC} = 4.5$ V	5	-	-	ns
		$V_{CC} = 6.0$ V	5	-	-	ns
<b><math>T_{amb} = -40</math> °C to <math>+125</math> °C</b>						
$t_{PHL}$ , $t_{PLH}$	propagation delay Dn to Qn	see <a href="#">Figure 8</a>				
		$V_{CC} = 2.0$ V	-	-	225	ns
		$V_{CC} = 4.5$ V	-	-	45	ns
		$V_{CC} = 6.0$ V	-	-	38	ns
	LE to Qn	see <a href="#">Figure 9</a>				
		$V_{CC} = 2.0$ V	-	-	265	ns
		$V_{CC} = 4.5$ V	-	-	53	ns
		$V_{CC} = 6.0$ V	-	-	45	ns
$t_{PZH}$ , $t_{PZL}$	3-state output enable time $\overline{OE}$ to Qn	see <a href="#">Figure 10</a>				
		$V_{CC} = 2.0$ V	-	-	225	ns
		$V_{CC} = 4.5$ V	-	-	45	ns
		$V_{CC} = 6.0$ V	-	-	38	ns
$t_{PHZ}$ , $t_{PLZ}$	3-state output disable time $\overline{OE}$ to Qn	see <a href="#">Figure 10</a>				
		$V_{CC} = 2.0$ V	-	-	225	ns
		$V_{CC} = 4.5$ V	-	-	45	ns
		$V_{CC} = 6.0$ V	-	-	38	ns

**Table 9: Dynamic characteristics 74HC373 ...continued**

*Voltages are referenced to GND (ground = 0 V); C<sub>L</sub> = 50 pF unless otherwise specified; for test circuit see Figure 12.*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t <sub>THL</sub> , t <sub>TLH</sub>	output transition time	see <a href="#">Figure 8</a>				
		V <sub>CC</sub> = 2.0 V	-	-	90	ns
		V <sub>CC</sub> = 4.5 V	-	-	18	ns
		V <sub>CC</sub> = 6.0 V	-	-	15	ns
t <sub>w</sub>	pulse width LE HIGH	see <a href="#">Figure 9</a>				
		V <sub>CC</sub> = 2.0 V	120	-	-	ns
		V <sub>CC</sub> = 4.5 V	24	-	-	ns
		V <sub>CC</sub> = 6.0 V	20	-	-	ns
t <sub>su</sub>	set-up time Dn to LE	see <a href="#">Figure 11</a>				
		V <sub>CC</sub> = 2.0 V	75	-	-	ns
		V <sub>CC</sub> = 4.5 V	15	-	-	ns
		V <sub>CC</sub> = 6.0 V	13	-	-	ns
t <sub>h</sub>	hold time Dn to LE	see <a href="#">Figure 11</a>				
		V <sub>CC</sub> = 2.0 V	5	-	-	ns
		V <sub>CC</sub> = 4.5 V	5	-	-	ns
		V <sub>CC</sub> = 6.0 V	5	-	-	ns

[1] C<sub>PD</sub> is used to determine the dynamic power dissipation (P<sub>D</sub> in μW).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum(C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f<sub>i</sub> = input frequency in MHz;

f<sub>o</sub> = output frequency in MHz;

C<sub>L</sub> = output load capacitance in pF;

V<sub>CC</sub> = supply voltage in V;

N = number of inputs switching;

$\sum(C_L \times V_{CC}^2 \times f_o)$  = sum of outputs.

**Table 10: Dynamic characteristics 74HCT373**

*Voltages are referenced to GND (ground = 0 V); C<sub>L</sub> = 50 pF unless otherwise specified; for test circuit see Figure 12.*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>T<sub>amb</sub> = 25 °C</b>						
t <sub>PHL</sub> , t <sub>PLH</sub>	propagation delay					
	Dn to Qn	see <a href="#">Figure 8</a>				
		V <sub>CC</sub> = 4.5 V	-	17	30	ns
		V <sub>CC</sub> = 5 V; C <sub>L</sub> = 15 pF	-	14	-	ns
	LE to Qn	see <a href="#">Figure 9</a>				
		V <sub>CC</sub> = 4.5 V	-	16	32	ns
		V <sub>CC</sub> = 5 V; C <sub>L</sub> = 15 pF	-	13	-	ns
t <sub>PZH</sub> , t <sub>PZL</sub>	3-state output enable time $\overline{OE}$ to Qn	V <sub>CC</sub> = 4.5 V; see <a href="#">Figure 10</a>	-	19	32	ns
t <sub>PHZ</sub> , t <sub>PLZ</sub>	3-state output disable time $\overline{OE}$ to Qn	V <sub>CC</sub> = 4.5 V; see <a href="#">Figure 10</a>	-	18	30	ns
t <sub>THL</sub> , t <sub>TLH</sub>	output transition time	V <sub>CC</sub> = 4.5 V; see <a href="#">Figure 8</a>	-	5	12	ns

**Table 10: Dynamic characteristics 74HCT373 ...continued**

Voltages are referenced to GND (ground = 0 V);  $C_L = 50$  pF unless otherwise specified; for test circuit see [Figure 12](#).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_W$	pulse width LE HIGH	$V_{CC} = 4.5$ V; see <a href="#">Figure 9</a>	16	4	-	ns
$t_{su}$	set-up time Dn to LE	$V_{CC} = 4.5$ V; see <a href="#">Figure 11</a>	12	6	-	ns
$t_h$	hold time Dn to LE	$V_{CC} = 4.5$ V; see <a href="#">Figure 11</a>	4	-1	-	ns
$C_{PD}$	power dissipation capacitance	per latch; $V_I = \text{GND to } (V_{CC} - 1.5 \text{ V})$	[1]	-	41	pF
<b><math>T_{amb} = -40</math> °C to <math>+85</math> °C</b>						
$t_{PHL}$ , $t_{PLH}$	propagation delay					
	Dn to Qn	$V_{CC} = 4.5$ V; see <a href="#">Figure 8</a>	-	-	38	ns
	LE to Qn	$V_{CC} = 4.5$ V; see <a href="#">Figure 9</a>	-	-	40	ns
$t_{PZH}$ , $t_{PZL}$	3-state output enable time $\overline{OE}$ to Qn	$V_{CC} = 4.5$ V; see <a href="#">Figure 10</a>	-	-	40	ns
$t_{PHZ}$ , $t_{PLZ}$	3-state output disable time $\overline{OE}$ to Qn	$V_{CC} = 4.5$ V; see <a href="#">Figure 10</a>	-	-	38	ns
$t_{THL}$ , $t_{TLH}$	output transition time	$V_{CC} = 4.5$ V; see <a href="#">Figure 8</a>	-	-	15	ns
$t_W$	pulse width LE HIGH	$V_{CC} = 4.5$ V; see <a href="#">Figure 9</a>	20	-	-	ns
$t_{su}$	set-up time Dn to LE	$V_{CC} = 4.5$ V; see <a href="#">Figure 11</a>	15	-	-	ns
$t_h$	hold time Dn to LE	$V_{CC} = 4.5$ V; see <a href="#">Figure 11</a>	4	-	-	ns
<b><math>T_{amb} = -40</math> °C to <math>+125</math> °C</b>						
$t_{PHL}$ , $t_{PLH}$	propagation delay					
	Dn to Qn	$V_{CC} = 4.5$ V; see <a href="#">Figure 8</a>	-	-	45	ns
	LE to Qn	$V_{CC} = 4.5$ V; see <a href="#">Figure 9</a>	-	-	48	ns
$t_{PZH}$ , $t_{PZL}$	3-state output enable time $\overline{OE}$ to Qn	$V_{CC} = 4.5$ V; see <a href="#">Figure 10</a>	-	-	48	ns
$t_{PHZ}$ , $t_{PLZ}$	3-state output disable time $\overline{OE}$ to Qn	$V_{CC} = 4.5$ V; see <a href="#">Figure 10</a>	-	-	45	ns
$t_{THL}$ , $t_{TLH}$	output transition time	$V_{CC} = 4.5$ V; see <a href="#">Figure 8</a>	-	-	18	ns
$t_W$	pulse width LE HIGH	$V_{CC} = 4.5$ V; see <a href="#">Figure 8</a>	24	-	-	ns
$t_{su}$	set-up time Dn to LE	$V_{CC} = 4.5$ V; see <a href="#">Figure 11</a>	18	-	-	ns
$t_h$	hold time Dn to LE	$V_{CC} = 4.5$ V; see <a href="#">Figure 11</a>	4	-	-	ns

[1]  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu\text{W}$ ).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum(C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

$f_i$  = input frequency in MHz;

$f_o$  = output frequency in MHz;

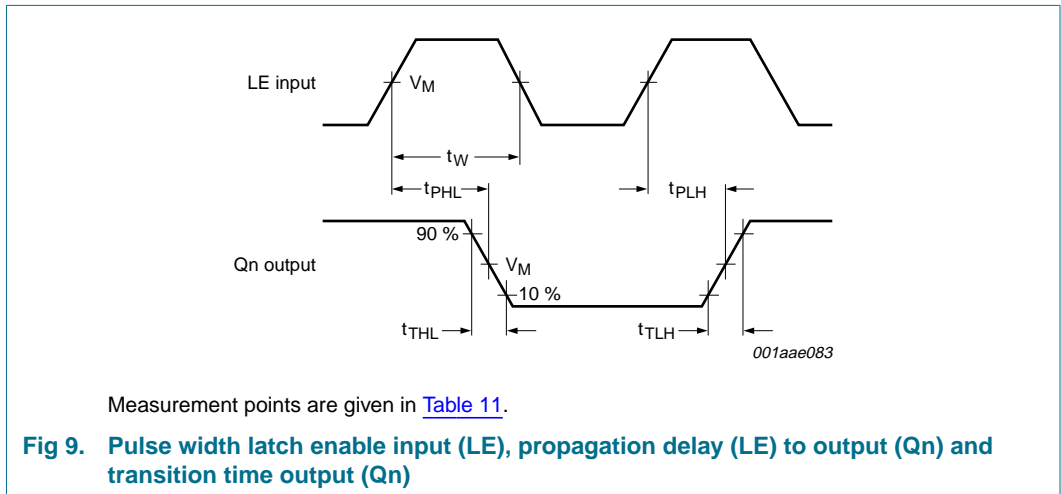
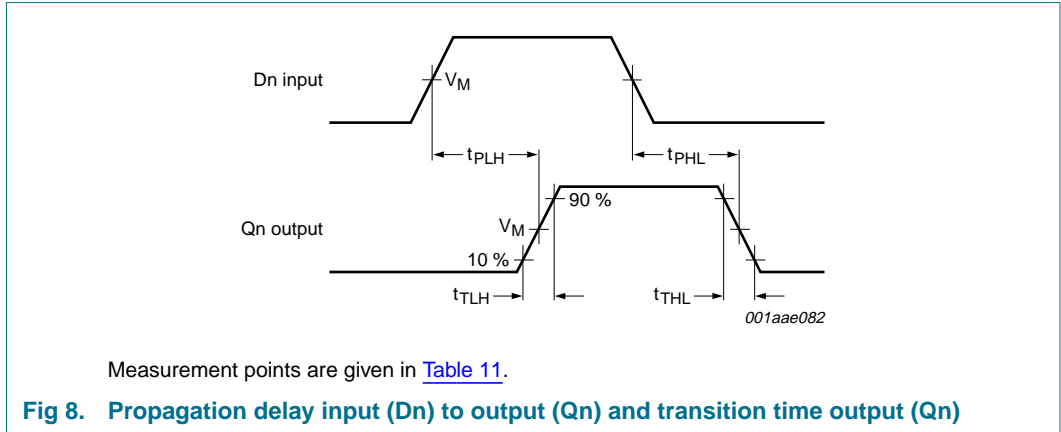
$C_L$  = output load capacitance in pF;

$V_{CC}$  = supply voltage in V;

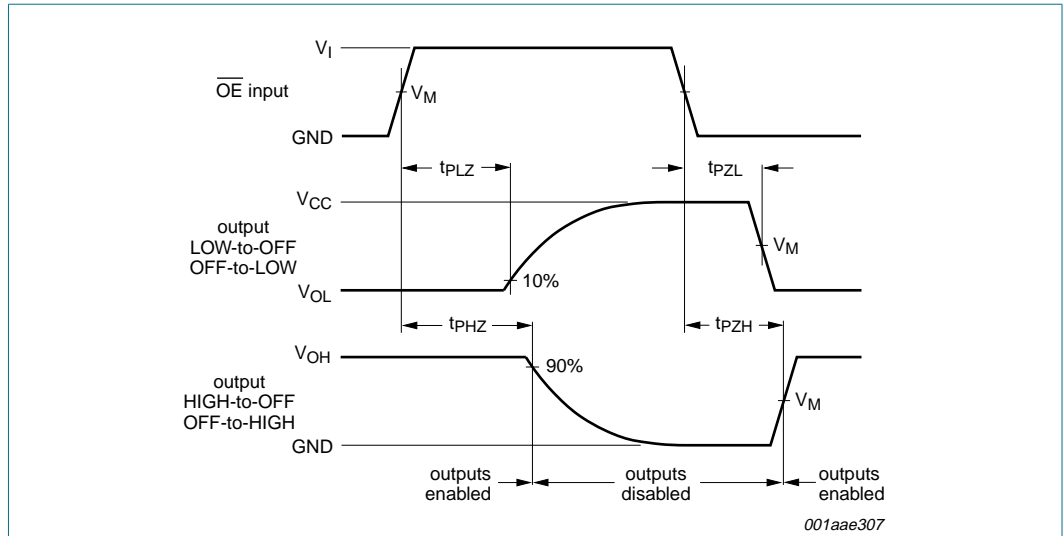
$N$  = number of inputs switching;

$\sum(C_L \times V_{CC}^2 \times f_o)$  = sum of outputs.

12. Waveforms

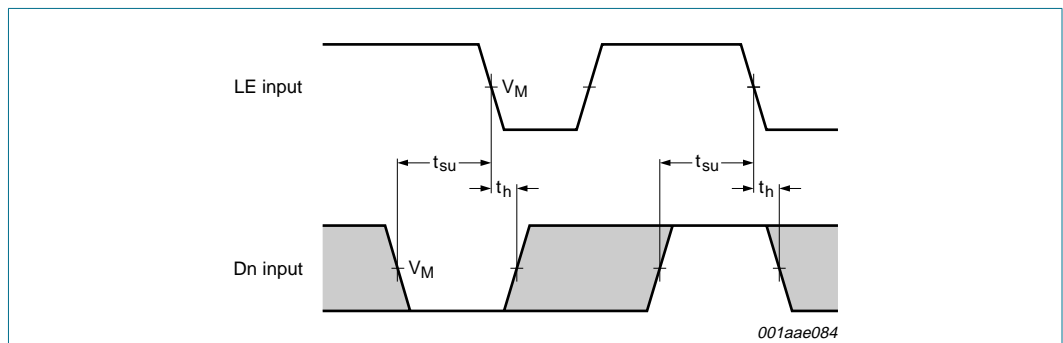






Measurement points are given in [Table 11](#).

**Fig 10. 3-state enable and disable time**



Measurement points are given in [Table 11](#).

**Fig 11. Set-up and hold time data input (Dn) to latch enable input (LE)**

**Table 11: Measurement points**

Type	Input	Output
	$V_M$	$V_M$
74HC373	$0.5V_{CC}$	$0.5V_{CC}$
74HCT373	1.3 V	1.3 V

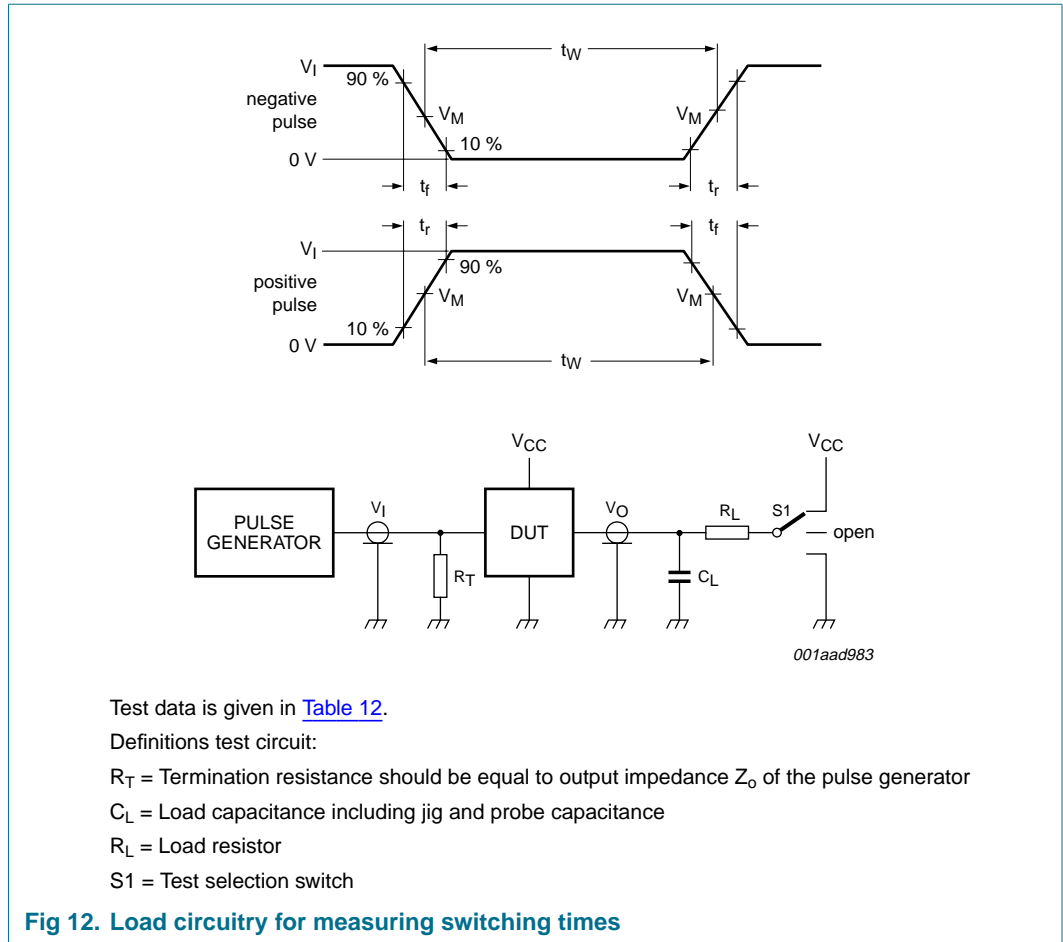


Table 12: Test data

Type	Input		Load		S1 position		
	$V_I$	$t_r, t_f$	$C_L$	$R_L$	$t_{PHL}, t_{PLH}$	$t_{PZH}, t_{PHZ}$	$t_{PZL}, t_{PLZ}$
74HC373	$V_{CC}$	6 ns	15 pF, 50 pF	1 k $\Omega$	open	GND	$V_{CC}$
74HCT373	3 V	6 ns	15 pF, 50 pF	1 k $\Omega$	open	GND	$V_{CC}$

13. Package outline

DIP20: plastic dual in-line package; 20 leads (300 mil)

SOT146-1

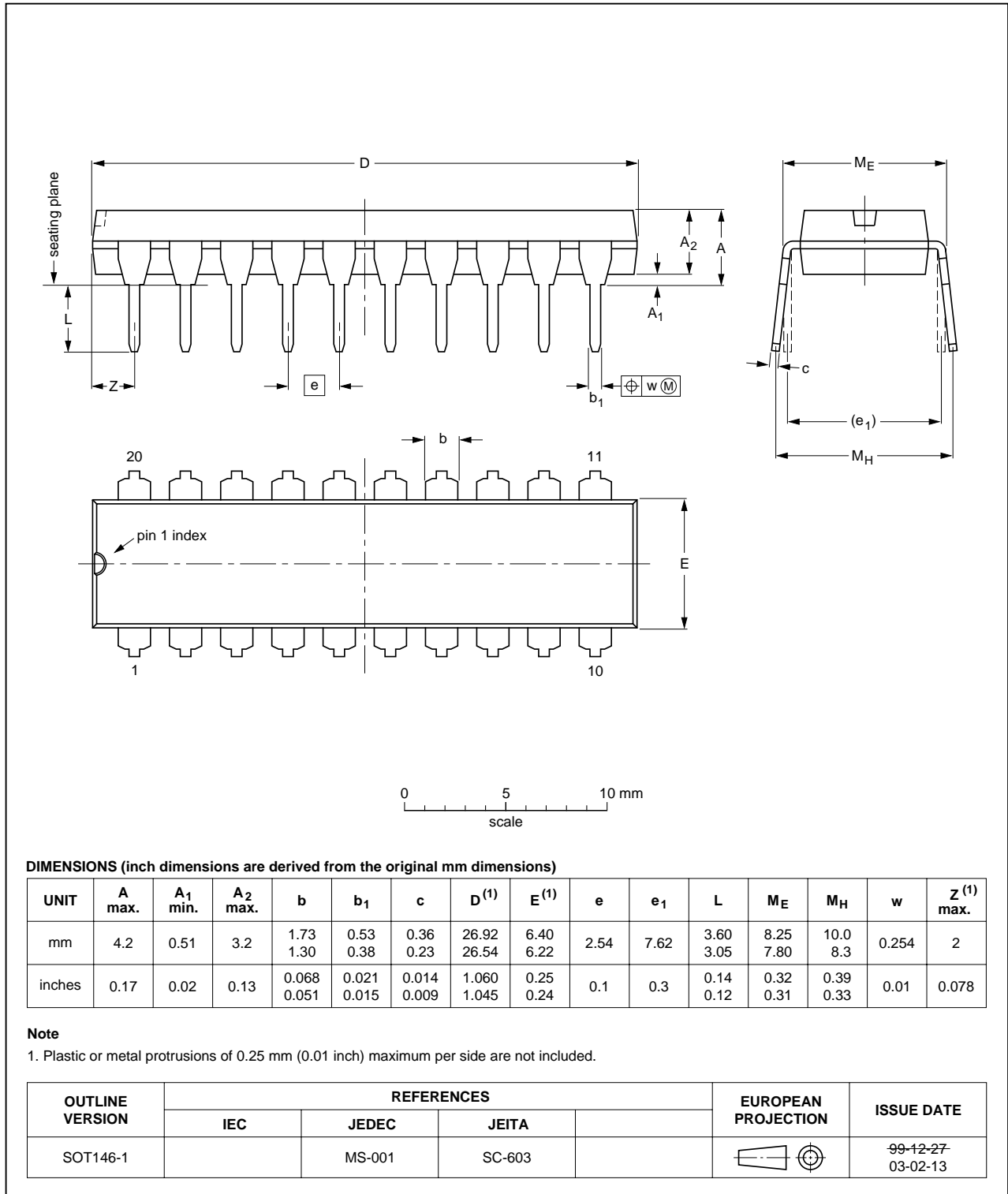


Fig 13. Package outline SOT146-1 (DIP20)

SO20: plastic small outline package; 20 leads; body width 7.5 mm

SOT163-1

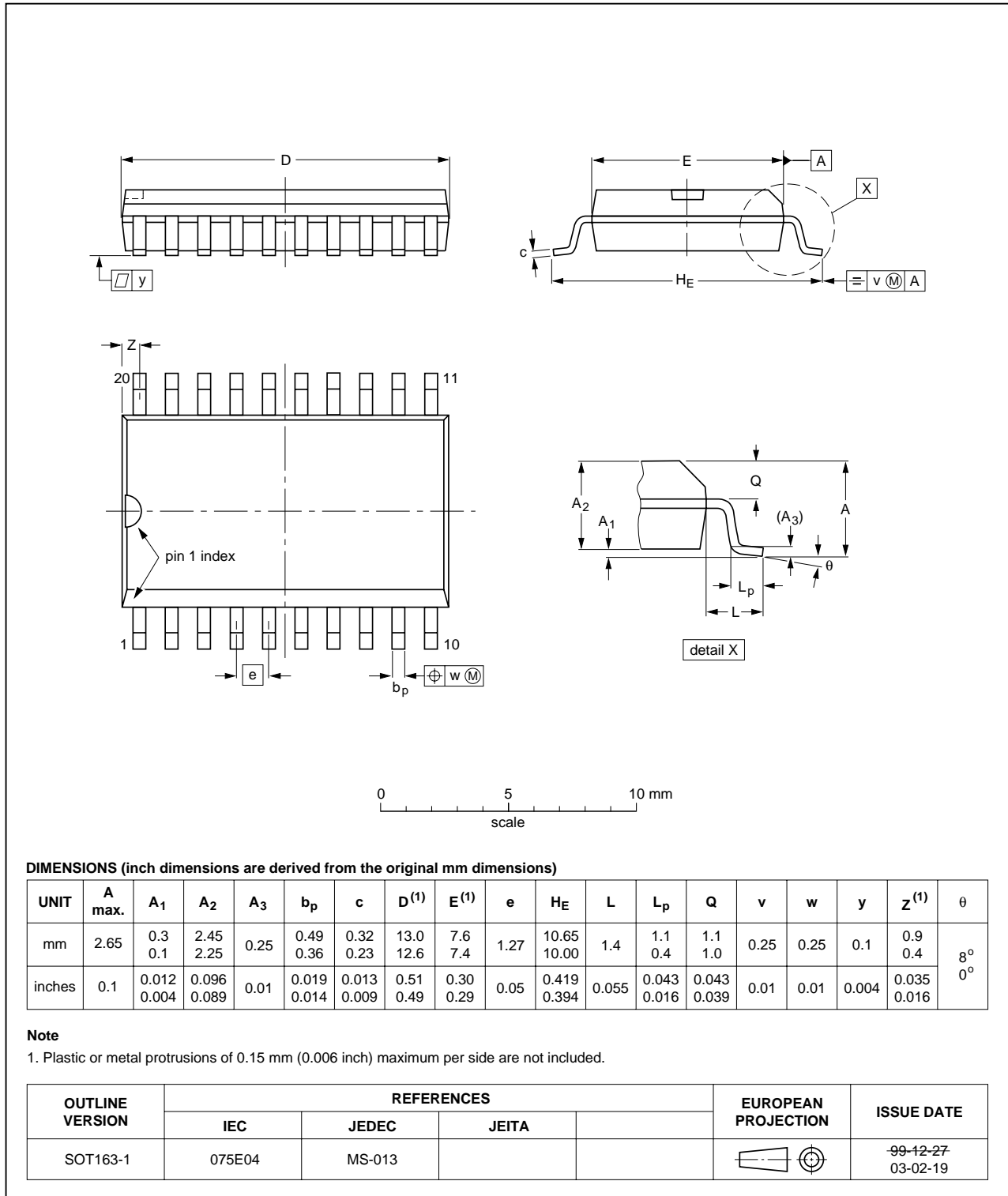


Fig 14. Package outline SOT163-1 (SO20)

SSOP20: plastic shrink small outline package; 20 leads; body width 5.3 mm

SOT339-1

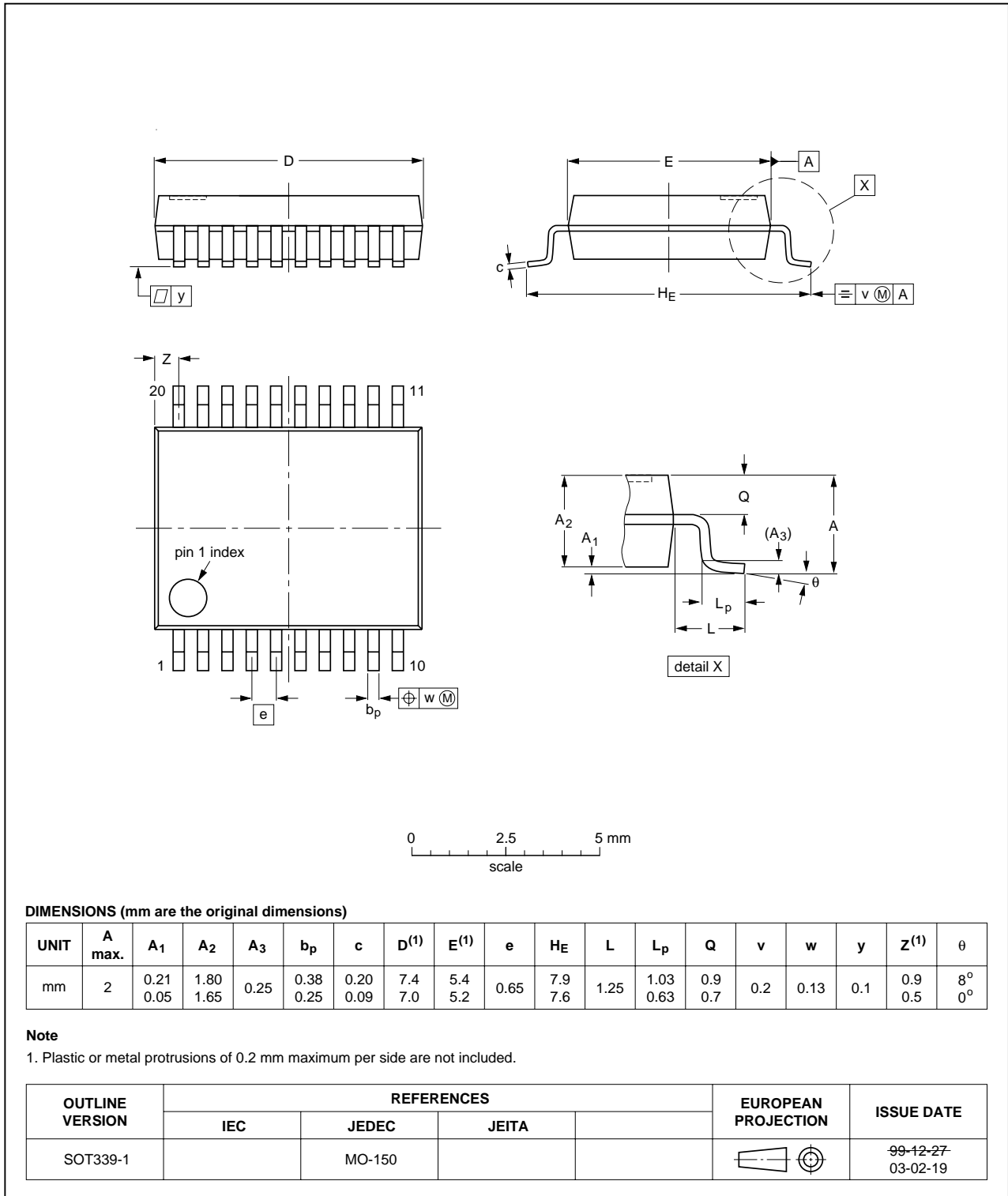


Fig 15. Package outline SOT339-1 (SSOP20)

TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm

SOT360-1



Fig 16. Package outline SOT360-1 (TSSOP20)

DHVQFN20: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 20 terminals; body 2.5 x 4.5 x 0.85 mm

SOT764-1

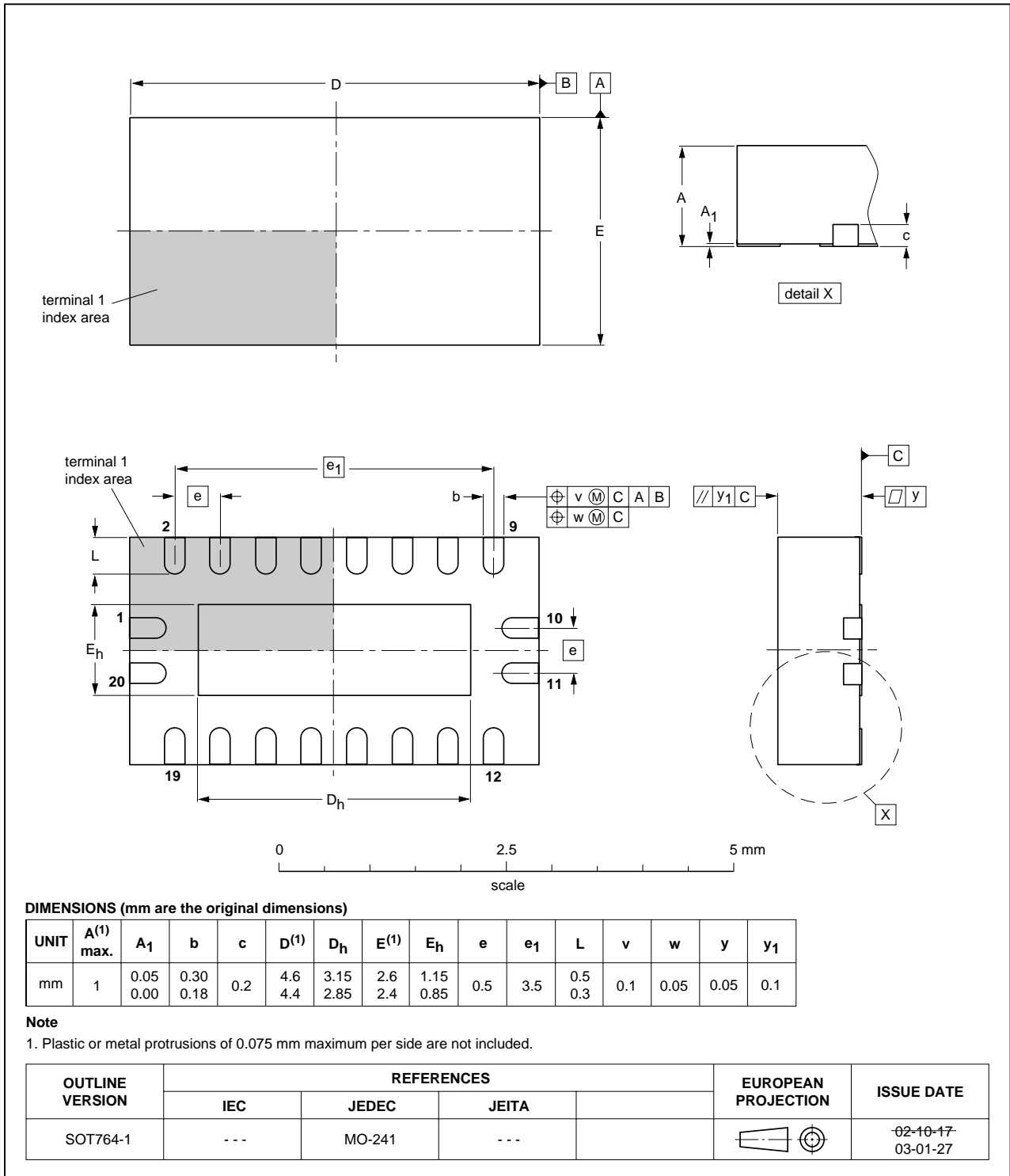


Fig 17. Package outline SOT764-1 (DHVQFN20)

## 14. Abbreviations

Table 13: Abbreviations

Acronym	Description
CMOS	Complementary Metal Oxide Semiconductor
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

## 15. Revision history

Table 14: Revision history

Document ID	Release date	Data sheet status	Change notice	Doc. number	Supersedes
74HC_HCT373_3	20060120	Product data sheet	-	-	74HC_HCT373_CNV_2
Modifications:					
			<ul style="list-style-type: none"> <li>The format of this data sheet is redesigned to comply with the current presentation and information standard of Philips Semiconductors.</li> <li>Added type numbers 74HC373BQ and 74HCT373BQ (package DHVQFN20).</li> <li>Added family specifications.</li> <li>Added abbreviations list.</li> </ul>		
74HC_HCT373_CNV_2	19970827	Product specification	-	-	-



## 16. Data sheet status

Level	Data sheet status <sup>[1]</sup>	Product status <sup>[2] [3]</sup>	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
III	Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN).

[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL <http://www.semiconductors.philips.com>.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

## 17. Definitions

**Short-form specification** — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

**Limiting values definition** — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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## 20. Contact information

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