Ordering number : EN8924B

SANYO Semiconductors
DATA SHEET

LV23100T-A — Bi-CMOS IC For Portable Audio System 1-chip Tuner IC Incorporating PLL

Overview

The LV23100T-A is a one-chip tuner IC incorporating PLL for portable audio system.

Functions

- FM tuner
- MPX stereo decoder
- PLL frequency synthesizer

Specifications

Maximum Ratings at Ta = 25 °C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{CC} max	V_{CC}	4.0	V
	V_{DD} max	V_{DD}	4.0	V
Maximum input voltage	$V_{IN}1$ max	CE, CI, CL	6.0	V
	$V_{IN}2$ max	XIN	V_{DD}+0.3	V
Allowable power dissipation	Pd max	Ta≤70°C	180	mW
Maximum output voltage	V_O1 max	DO	6.0	V
	V_O2 max	XOUT, PD	V_{DD}+0.3	V
	V_O3 max	BO1, BO2, AOUT	12.0	V
Operating temperature	Topr		-20 to +70	°C
Storage temperature	Tstg		-40 to +125	°C

Note : This product should be handled with care because the resistance against electrostatic discharge damage is low.

- CCB is a registered trademark of SANYO Electric Co., Ltd.
- CCB is SANYO Semiconductor's original bus format. All bus addresses are managed by SANYO Semiconductor for this format.

SANYO Semiconductor Co., Ltd.
TOKYO OFFICE Tokyo Bldg., 1-10, 1 Chome, Ueno, Taito-ku, TOKYO, 110-8534 JAPAN

Operating Condition at Ta = 25 °C

Parameter	Symbol	Conditions	Ratings	Unit
Recommended supply voltage	V_{CC}		3.0	V
	V_{DD}		3.0	V
Operating supply voltage range	V_{CC} op		2.2 to 3.6	V
	V_{DD} op		2.2 to 3.6	V

PLL block Allowable Operating Range at Ta = -20°C to +70°C, V_{SS} = 0V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Supply voltage	V_{DD}		2.2		3.6	V
Input high level voltage	V_{IH}	CE, CL, DI	$0.7V_{DD}$		6.0	V
Input low level voltage	V_{IL}	CE, CL, DI	0		$0.3V_{DD}$	-
Output voltage	V_O1	DO	0		6.0	V
	V_O2	BO1, BO2, AOUT	0		10	V
Operating frequency	$f_{IN}1$	XIN ; $V_{IN}1$		75		kHz
	$f_{IN}2$	FMIN ; $V_{IN}2$	10		160	MHz

Note : Due attention must be paid on leak because the XIN pin has an extremely high input impedance.

Operating Characteristics at Ta = 25°C, V_{CC} = V_{DD} = 3.0V, See the specified circuit.

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
[Current dissipation]						
FM tuner block	I_{CC}FM	No input in FM mode	9	12.5	16	mA
PLL block	I_{DD}FM	fr = 98MHz, No input at tuner	1	2	4	mA
[FM-FE characteristics] : fc = 98MHz, fm = 1kHz, dev = 22.5kHz						
3dB sensitivity	-3dBLS	V_{IN} = 60dBμV EMF reference, -3dB input		10		dBμV EMF
Actual sensitivity	QS	S/N = Input at S/N = 30dB		13		dBμV EMF
[FM-IF monaural characteristics] : fc = 10.7MHz, fm = 1kHz, dev = 75kHz						
Demodulation output	V_O	V_{IN} = 100dBμV	140	180	210	mVrms
3dB sensitivity	LS	V_{IN} = 100dBμV reference, -3dB input	26	31	36	dBμV
Signal-to-noise ratio	S/N	V_{IN} = 100dBμV	63	70		dB
IF count sensitivity	IF-C1	0%mod, SDC = 1	42	50	56	dBμV
Mute attenuation	MUTE	V_{IN} = 100dBμV, L output	55	60		dB
[FM-IF stereo characteristics] : fc = 10.7MHz, fm = 1kHz, dev = 75kHz (L+R = 90%, Pilot = 10%)						
Separation	SEP	V_{IN} = 100dBμV, L output/R output	25	40		dB
Total harmonic distortion	THD	V_{IN} = 100dBμV, MAIN-MOD		0.5	1.5	%

Continued on next page.

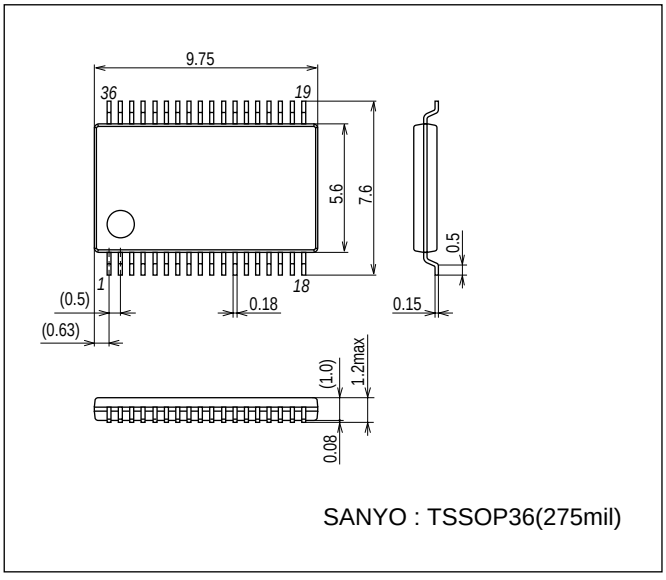
Continued from preceding page.

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
[PLL characteristics]						
Internal return resistance	Rf	XIN		8		MΩ
Built-in output resistance	Rd	XOUT		250		kΩ
Hysteresis width	VHIS	CE, CL, DI		$0.1V_{DD}$		V
Output high level voltage	V_{OH}	PD ; I_O = -1mA	V_{DD}-1.0			V
Output low level voltage	$V_{OL}1$	PD ; I_O = 1mA			1.0	V
	$V_{OL}2$	BO1, BO2 ; I_O = 1mA			0.25	V
		BO1, BO2 ; I_O = 5mA			1.25	V
	$V_{OL}3$	DO ; I_O = 1mA			0.25	V
	$V_{OL}4$	AOUT ; I_O = 1mA, AIN = 2.0V			0.5	V
Input high level current	$I_{IH}1$	CE, CL, DI ; V_I = 6.0V			5.0	μA
	$I_{IH}2$	XIN ; $V_I = V_{DD}$	0.16		0.9	μA
	$I_{IH}3$	AIN ; V_I = 6.0V			200	nA
Input low level current	$I_{IL}1$	CE, CL, DI ; V_I = 0V			5.0	μA
	$I_{IL}2$	XIN ; V_I = 0V	0.16		0.9	μA
	$I_{IL}3$	AIN ; V_I = 0V			200	nA
Output off-leak current	IOFF1	BO1, AOUT, BO2 ; V_O = 10V			5.0	μA
	IOFF2	DO ; V_O = 6.0V			5.0	μA
"H" level 3-state off-leak current	IOFFH	PD ; V_O = 6.0V		0.01	200	nA
"L" level 3-state off-leak current	IOFFL	PD ; V_O = 0V		0.01	200	NA

Note: For the internal return resistance, internal output resistance, hysteresis width, and output low level voltage ($V_{OL}2$) described in the above PLL characteristics table, the reference value is shown.

Package Dimensions

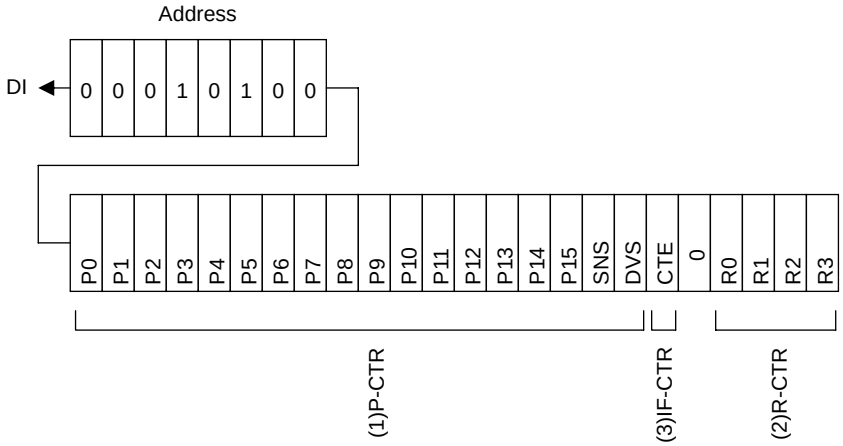
unit : mm (typ)
3247A



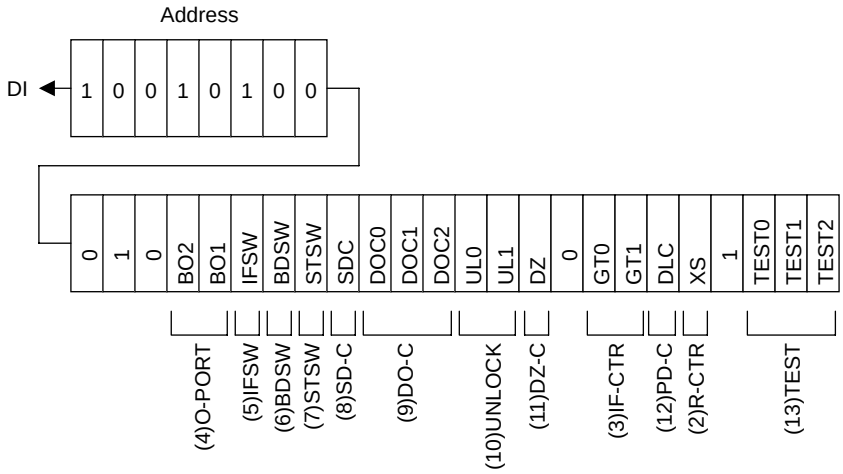
SANYO : TSSOP36(275mil)

Composition of DI control data (serial data input)

(1) IN mode



(2) IN2 mode



Description of DI control Data

No.	Control block data	Description	Related data
(1)	DO pin Control data DOC0 DOC1 DOC2	• Data to set the dividing number of programmable divider Binary value with P15 assumed to be MSB. LSB varies according to DVS and SNS. (* : don't care) DVS | SNS | LSB | set dividing number (N) | actual dividing number 1 | * | P0 | 272 to 65535 | Twice the set value 0 | 1 | P0 | 272 to 65535 | Set value 0 | 0 | P4 | 4 to 4095 | Set value * P0 to P3 invalid when LSB : P4 • To select the signal input (FMIN, AMIN) to the programmable divider and to change the input frequency range. (* : don't care) DVS | SNS | Input | Operation frequency range 1 | * | FMIN | 10 to 160MHz	

Continued on next page.

Continued from preceding page.

<table>
<tr><th>No.</th><th>Control block data</th><th>Description</th><th>Related data</th></tr>
<tr><td>(2)</td><td>Reference
divider data

R0 to R3
XS</td><td>• Reference frequency (fref) selection data
<table>
<tr><th>R3</th><th>R2</th><th>R1</th><th>R0</th><th>Reference frequency</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>25kHz</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>1</td><td>25kHz</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0</td><td>25kHz</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>1</td><td>25kHz</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>0</td><td>12.5kHz</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>1</td><td>6.25kHz</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>0</td><td>3.125kHz</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>1</td><td>3.125kHz</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>0</td><td>5kHz</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>1</td><td>5kHz</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>0</td><td>5kHz</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>1</td><td>1kHz</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>0</td><td>3kHz</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>1</td><td>15kHz</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>0</td><td>PLL INHIBIT+X'tal OSC STOP</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>1</td><td>PLL INHIBIT</td></tr>
</table>
* PLL INHIBIT
• The programmable divider and IF counter stop, with FMIN, AMIN, and IFIN inputs being in the pull-down condition (GND), and the charge pump has the high impedance.
• XS must be zero.</td><td></td></tr>
<tr><td>(3)</td><td>IF counter
control data

CTE
GT0, GT1</td><td>• IF counter counting start data
CTE = 1 : Counting start
= 0 : Counting start
• Determines the counting time of universal counter
<table>
<tr><th>GT1</th><th>GT0</th><th>Counting time</th><th>Wait time</th></tr>
<tr><td>0</td><td>0</td><td>4ms</td><td>3 to 4ms</td></tr>
<tr><td>0</td><td>1</td><td>8ms</td><td>3 to 4ms</td></tr>
<tr><td>1</td><td>0</td><td>16ms</td><td>3 to 4ms</td></tr>
<tr><td>1</td><td>1</td><td>32ms</td><td>3 to 4ms</td></tr>
</table></td><td></td></tr>
<tr><td>(4)</td><td>Output port data

$\overline{BO1}$, $\overline{BO2}$</td><td>• Data to determine output of output ports $\overline{BO1}$ and $\overline{BO2}$
"Data" = 0 : OPEN
1 : Low</td><td></td></tr>
<tr><td>(5)</td><td>MUTE control
data

IFSW</td><td>• Data to determine the output of output port IFSW, controlling the MUTE function.
"Data" = 0 : at receiving
1 : MUTE</td><td></td></tr>
<tr><td>(6)</td><td>FM/AM BAND
selection
control data
BDSW</td><td>• Data to determine the output of output port BDSW, controlling selection of BAND.
"Data" = 0 : AM
1 : FM</td><td></td></tr>
<tr><td>(7)</td><td>Forced monaural
control data

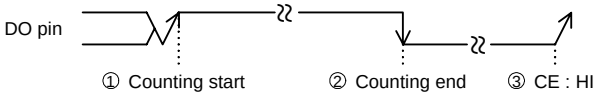
STSW</td><td>• Data to determine the output of output port STSW, controlling the forced stereo functions.
"Data" = 0 : MONO
1 : STEREO</td><td></td></tr>
<tr><td>(8)</td><td>SD sensitivity
control data

SDC</td><td>• Data to determine the output of output port SDC, controlling the FM-SD sensitivity (at IF input).
<table>
<tr><th>SDC</th><th>FM-SD sensitivity</th></tr>
<tr><td>0*</td><td>38dBμV</td></tr>
<tr><td>1</td><td>48dBμV</td></tr>
</table></td><td></td></tr>
</table>

Continued on next page.

Continued from preceding page.

<table>
<tr><th>No.</th><th>Control block data</th><th>Description</th><th>Related data</th></tr>
<tr><td>(9)</td><td>DO pin
control data

DOC0
DOC1
DOC2</td><td>• Data to determine the output of the DO pin.
<table>
<tr><th>DOC2</th><th>DOC1</th><th>DOC0</th><th>DO pin condition</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>Open</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>Low when unlock is detected.</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>end-UC (See the item with asterisk below)</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>Open</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>Open</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>Low when stereo</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>Low when SDON</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>Open</td></tr>
</table>
• The open condition is selected at power ON/reset.
* IF counter counting end check


① With end-UC set and IF counter starting (CTE = 0→1), DO pin opens automatically.
② At end of counting of the IF counter, DO pin goes LOW and check on counting end can be made.
③ DO pin opens when serial data is entered/output (CE pin : Hi)
Note : DO pin is always in the open condition during data input (IN1 and IN2 modes, during CE : Hi period), regardless of DO pin control data (DOC0 to 2). In the DO pin condition during data output (OUT mode, CE-Hi period), the content of internal DO serial data is output in synchronization with CL, regardless of DO pin control data (DOC).</td><td>UL0, UL1
CTE</td></tr>
<tr><td>(10)</td><td>Unlock detection
data

UL0, UL1</td><td>• Phase error (ϕE) detection width selection data to judge if PLL is locked.
• Phase error exceeding the detection width is judged that PLL is locked
(* : don't care)
<table>
<tr><th>UL1</th><th>UL0</th><th>ϕE Detection width</th><th>Detection output</th></tr>
<tr><td>0</td><td>0</td><td>Stop</td><td>Open</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>Direct output of ϕE</td></tr>
<tr><td>1</td><td>*</td><td>±6.67μs</td><td>ϕE extended by 1 to 2 ms</td></tr>
</table>
* DO pin is LOW. Serial data output : UL = 0.</td><td>DOC0
DOC1
DOC2</td></tr>
<tr><td>(11)</td><td>Phase
comparator
control data

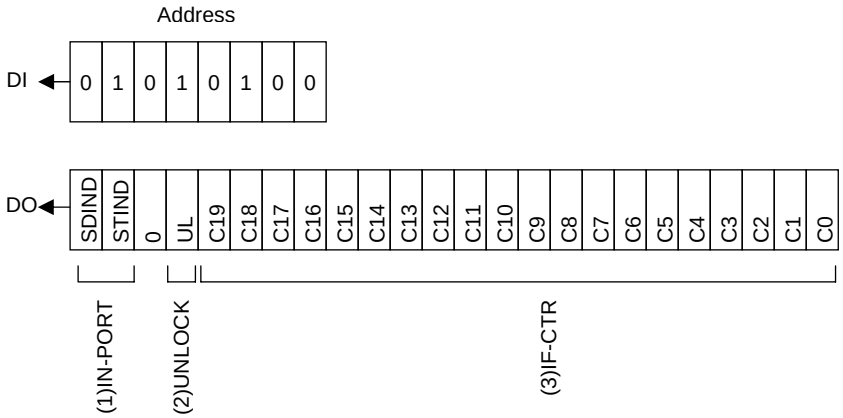
DZ</td><td>• Data to control the dead zone of phase comparator
<table>
<tr><th>DZ</th><th>Charge pump output</th></tr>
<tr><td>0</td><td>DZA</td></tr>
<tr><td>1</td><td>DZB</td></tr>
</table>
Dead zone width : DZA<DZB</td><td></td></tr>
<tr><td>(12)</td><td>Charge pump
control data

DLC</td><td>• Data to enforce control of charge pump output
<table>
<tr><th>DLC</th><th>Charge pump output</th></tr>
<tr><td>0</td><td>Normal</td></tr>
<tr><td>1</td><td>Forced to LOW</td></tr>
</table>
In case of dead lock because of VCO oscillation stop when the VCO control voltage (Vtune) is 0V, it is possible to clear dead lock by setting the charge pump output to LOW and V tune to V_{CC}.
(Dead lock clear circuit)</td><td></td></tr>
<tr><td>(13)</td><td>LSI test data

TEST0 to 2</td><td>• LSI test data
TEST0
TEST1
TEST2 ┘ All to be set to "0"
All set to zero at power ON/reset</td><td></td></tr>
</table>

DO control data (serial data output) composition

(1) OUT mode

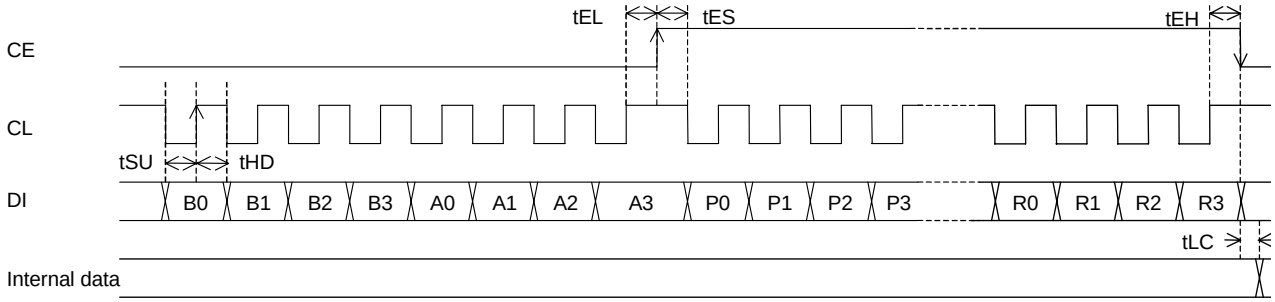


Description of DO output data

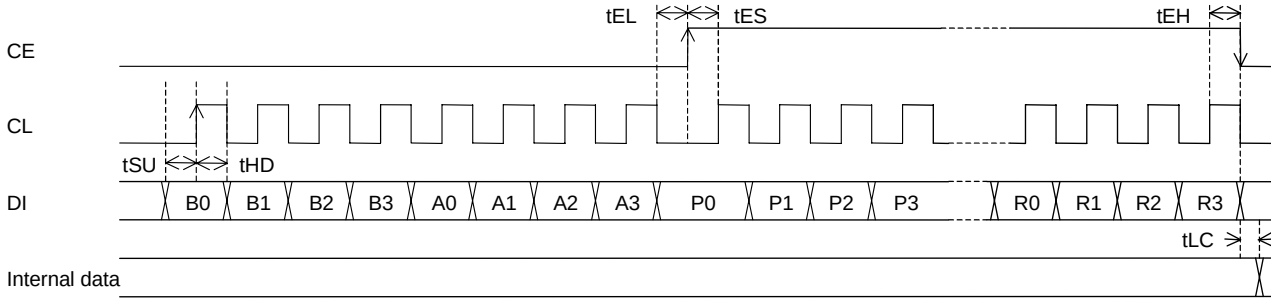
No.	Control block data	Description	Related data
(1)	SD and Stereo indicators control data STIND, SDIND	• Data latching SD and stereo indicator conditions. Latching made in the data output (OUT) mode. SDIND←SD indicator condition 0 : SD ON, 1 : SD OFF STIND←Stereo indicator condition 0 : ST ON, 1 : ST OFF	
(2)	PLL unlock data UL	• Data latching the content of unlock detection circuit UL←0 : At unlock 1 : At lock or detection stop mode	UL0 UL1
(3)	IF counter, binary counter C19 to C0	• Data latching the content of IF counter (20-bit binary counter) C19←MSB of binary counter C0 ←MSB of binary counter	CTE GT0 GT1

Serial data input (IN1/IN2) tSU, tHD, tEL, tES, tEH≥0.75μs tLC<0.75μs

CL : Normally Hi

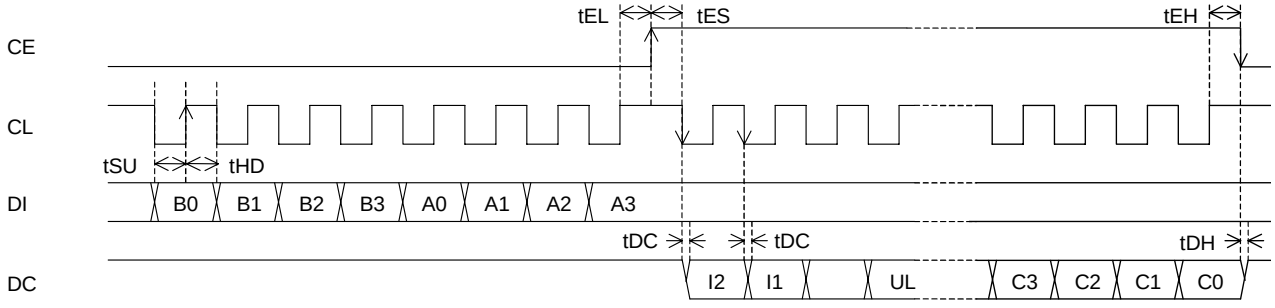


CL : Normally Low

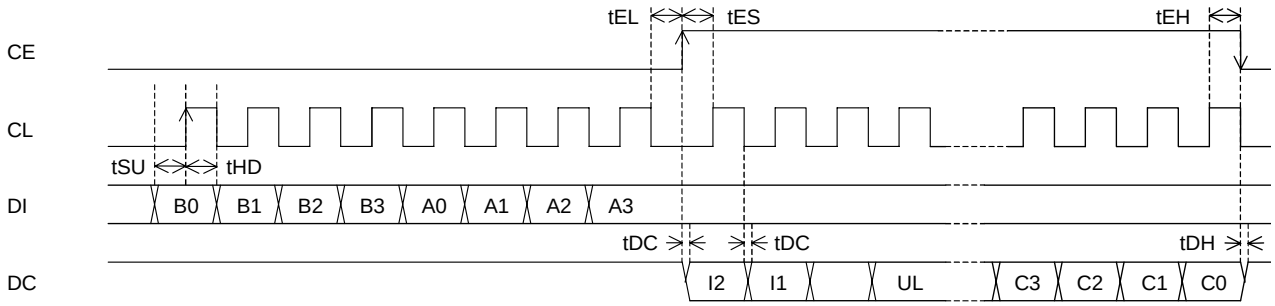


Serial data output (OUT) tSU, tHD, tEL, tES, tEH≥0.75μs tDC, tDH<0.35μs

CL : Normally Hi

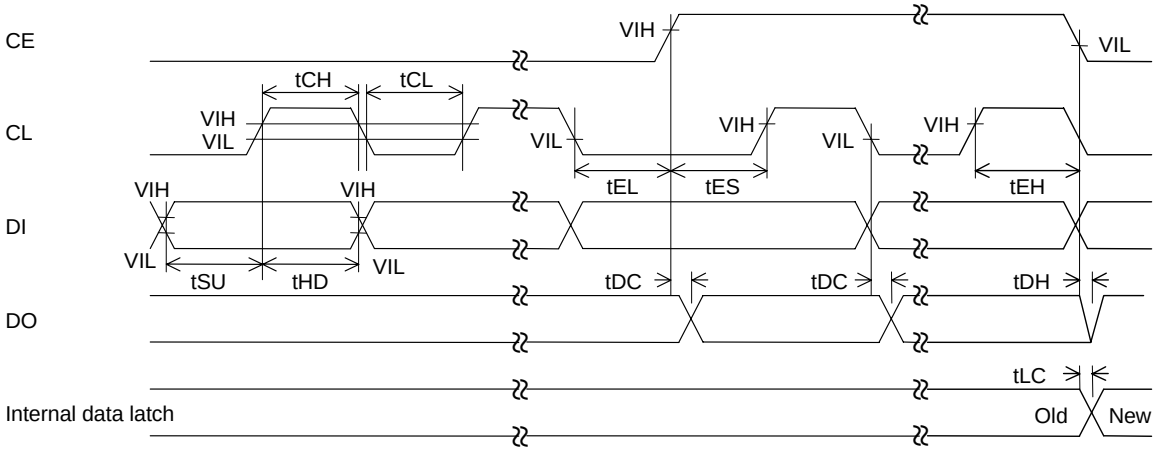


CL : Normally Hi

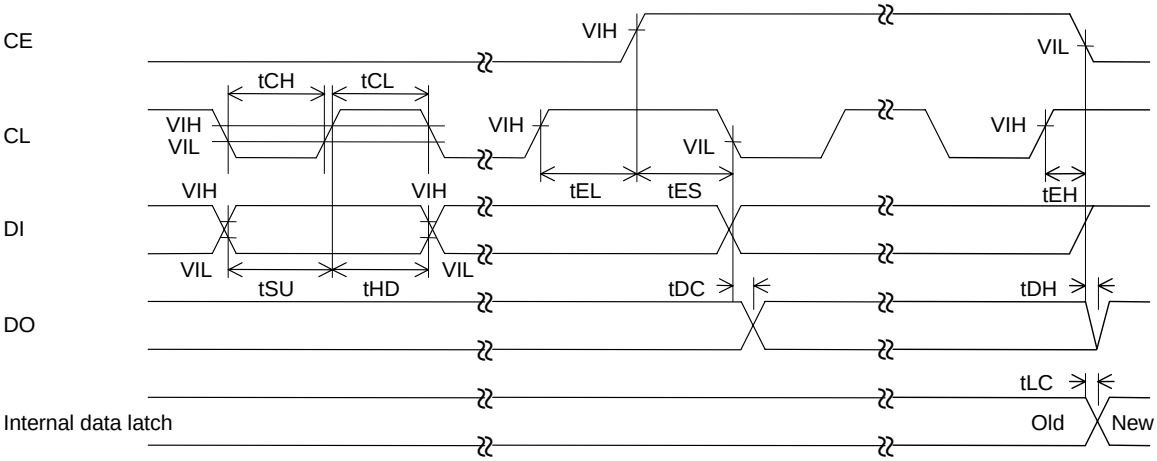


(Note) DO pin is an Nch open drain pin, so that the data varying time (tDC and tDH) differs depending on the pull-up resistance and substrate capacity.

Serial data timing



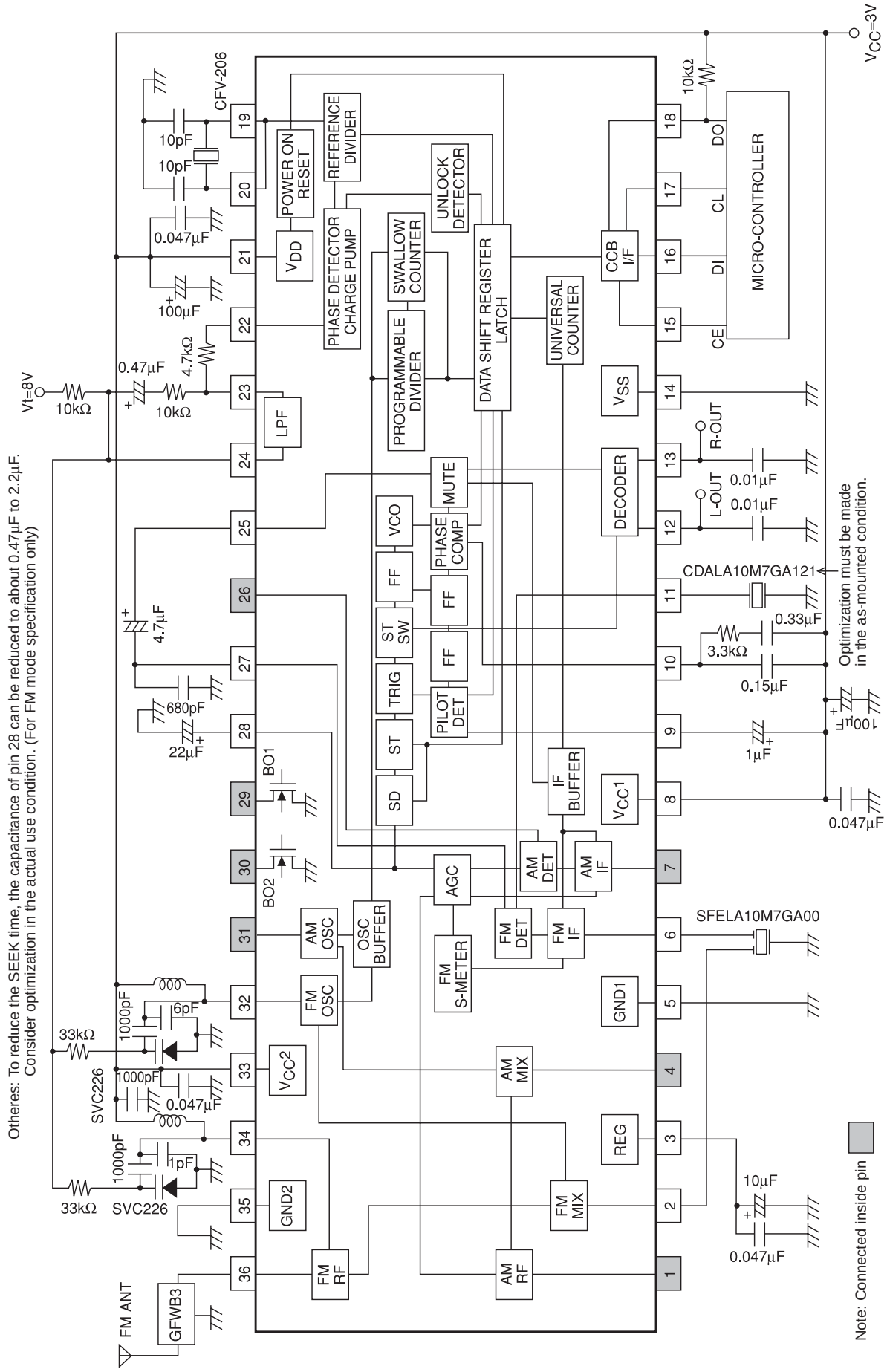
<< When CL stops at the “L” level >>



<< When CL stops at the “H” level >>

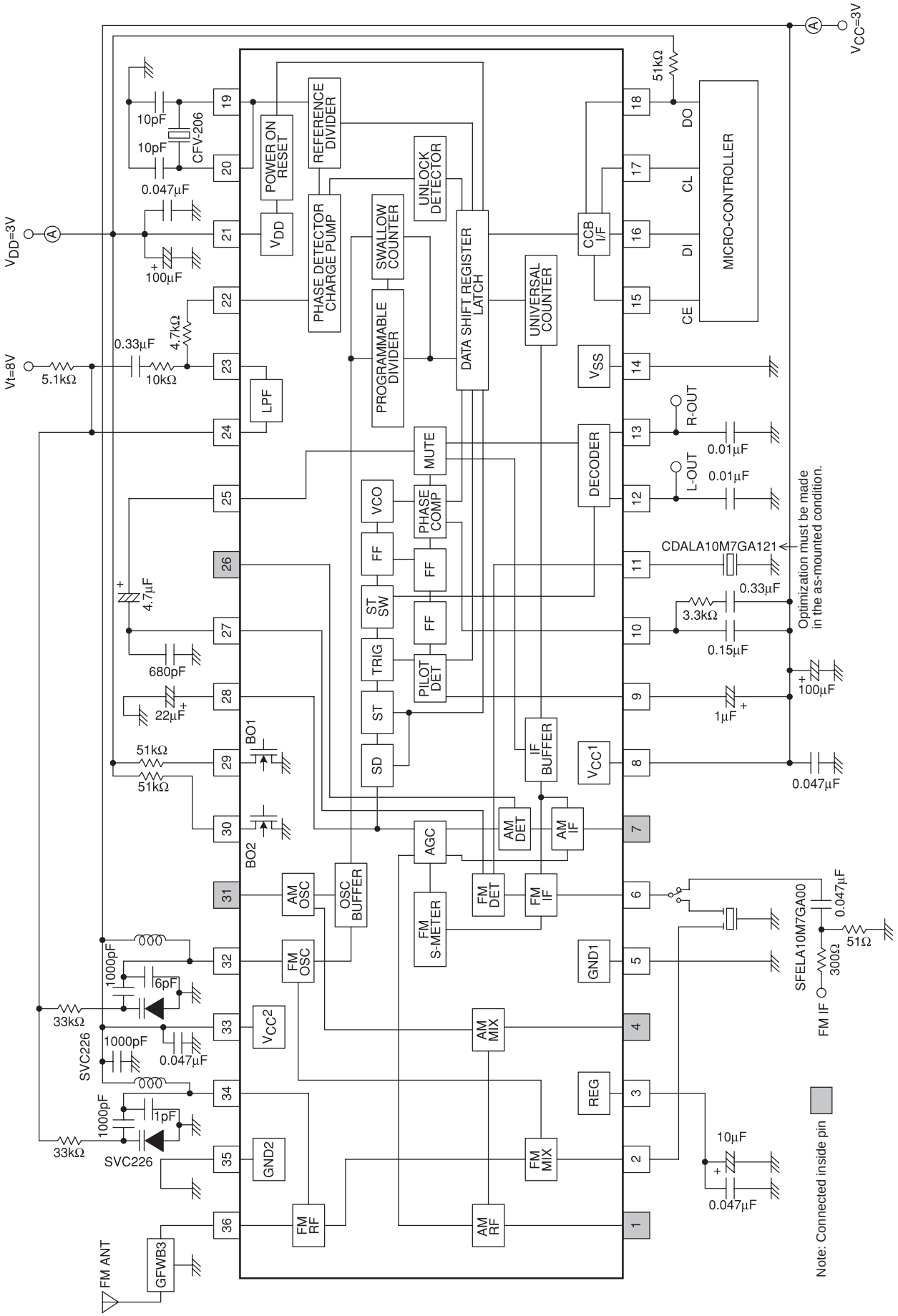
Parameter	Symbol	Pin	Conditions	Min	Typ	Max	Unit
Data setup time	tSU	DI, CL		0.75			μs
Data hold time	tHD	DI, CL		0.75			μs
Clock “L” level time	tCL	CL		0.75			μs
Clock “H” level time	tCH	CL		0.75			μs
CE wait time	tEL	CE, CL		0.75			μs
CE setup time	tES	CE, CL		0.75			μs
CE hold time	the	CE, CL		0.75			μs
Data latch change time	tLC					0.75	μs
Data output time	tDC	DO, CL	Differs depending on the pull-up resistance and substrate capacity			0.35	μs
	tDH	DO, CE					

Block Diagram and Sample Application Circuit



ILV00195

Test Circuit



Coil specifications (Example: Carry out optimization in the as-mounted condition.)

• FM-BPF : GFWB3 (Soshin) 76MHz to 108MHz
• FM-RF : SA-149 (Sumida) 3.6mm diameter, air core, 0.6mm wire, 4.5T
• FM-OSC : SA-151 (Sumida) 3.6mm diameter, air core, 0.6mm wire, 3.5T
• FM-IF Filter : SFELA10M7GA00 (Murata)
• FM-Discriminator : CDALA10M7GA121 (Murata)
• Crystal oscillator : CFV-206 (Citizen)